The TTL Data Book

for

Design Engineers

TEXAS INSTRUMENTS

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Please note: Details of all Texas Instruments AS and ALS Products are contained in TTL Data Book Vol II. Details of all Texas Instruments HC and HCT Products are contained in the High-Speed CMOS Logic Data Book.

THE TTL DATA BOOK

In this data book, Texas Instruments is pleased to present important technical information on the industry's broadest families of TTL integrated circuits.

You will find complete specifications on standard-technology TTL circuits (Series 54/74, Series 54H/74H) and on TI's high-technology TTL circuits such as the Schottky-clamped* Series 54LS/74LS and Series 54S/74S. Information on Advanced Low Power Schottky and Advanced Schottky devices (54ALS/74ALS, 54AS/74AS) is contained in volume II.

The indexes are designed for ease of circuit selection with margin tabs to guide you quickly to general circuit categories, and the alphanumeric and functional indexes will let you locate specific circuit types quickly. In addition, a section showing pin assignments, package availability, and a brief description of the circuit type arranged in type-number order is included for quick reference. Whenever practical, the MSI functions are arranged in sequence by type number to further simplify the task of locating a particular function.

A section is devoted to JAN IC's and provides a table of recommended usage and cross reference from TI part number to 38510 slash sheet, and 38510 slash sheet to TI part number.

Another handy reference for the design engineer is the section on IC sockets and interconnection panels from TI.

Although this volume offers design and specification data only for TTL integrated circuits, complete technical data for any TI semiconductor/component products are available from your nearest TI sales office, or local authorised TI distributor.

We sincerely hope you will find the new TTL Data Book for Design Engineers a meaningful addition to your technical library.

* Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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Please note: Details of all Texas Instruments HC and HCT products are contained in the High-Speed CMOS Logic Data Book.

The following pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. The electrical specifications are referenced by page number.

GATES AND BUFFERS

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

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Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

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Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

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Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

Interchangeability Guide

Please note: Details of all Texas Instruments AS and ALS Products are contained in TTL Data Book Vol II.

TTL INTERCHANGEABILITY GUIDE

Direct Replacements were selected as pin-for-pin equivalent circuits based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangability in any particular application is not necessarily guaranteed. Before using a substitute, the user should compare the specifications of the substitute device with the detailed specifications of the original device.

TI makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

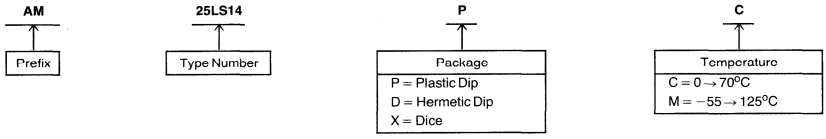
Recommendation for New Designs lists devices performing a similar (sometimes identical) function. Most are pin-for-pin equivalents for the competitor's part. However, the recommended part may have different pin-outs or organizations, as later technologies are listed in some cases to ensure that current high-performance components are recommended.

Only the basic circuit numbers are cross referenced. As the pin-out sometimes varies between a flat-package part and the equivalent DIP part, it is recommended that the manufacturer's specifications be consulted prior to specifying a direct replacement. Other than parts offered only in a flat package, the dual-in-line pin-outs were used as a guide in preparing the following cross references.

The list is intended to give TI replacements for competitors' parts not using the 54/74 numberinge system. For a complete listing of parts in the 54 and 74 families, see the functional index, pages 1 - 11 through 1 - 17.

ADVANCED MICRO DEVICES

Example of AMD ordering code:

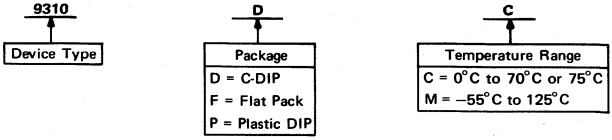


AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS	AMD TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
2501		SN74ALS192/SN74LS192	25LS2513	SN74LS348	SN74LS348
2505		SN74284/SN74285	25LS2517	SN74LS382	SN74LS382
2506		SN74AS881/SN74AS181	25LS2521	SN74LS682	SN74LS682/SN74ALS682
25LS07	SN74LS378	SN74LS378	25LS2568	SN74ALS568	SN74ALS568
25LS08	SN74LS379	SN74LS279	25LS2569	SN74ALS569	SN74ALS569
25LS09	SN74LS399	SN74LS399	2600		SN74121
25LS14	SN74LS384	SN74LS384	2602		SN74123
25LS15	SN74LS385	SN74LS385	26123		SN74123
25LS22	SN74LS322A	SN74LS322A	8224	SN74LS424	SN74LS424
25LS23	SN74LS323	SN74LS323	9304		SN74LS245
25LS240	SN74LS240	SN74ALS240	9300	SN743195	SN74LS245
25LS241	SN74LS241	SN74ALS241	9301	SN29301	SN7442A
25LS242	SN74LS242	SN74ALS242	9308	SN29308	SN74116
25LS243	SN74LS243	SN74ALS243	9309	SN29309	SN174153
25LS244	SN74LS244	SN74ALS244	9310	SN74160	SN74ALS160
25LS273	SN74LS273	SN74ALS273	9311	SN74154	SN74154
25LS299	SN74LS299	SN74ALS299	9312	SN29312	SN74ALS151
25LS373	SN74LS373	SN74ALS573	9316	SN74161	SN74ALS161
25LS374	SN74LS374	SN74ALS574	9318	SN74148	SN74LS148
25LS377	SN74LS377	SN74LS377	9322	SN74157	SN74ALS157
25LS381	SN74LS381	SN74LS381	9334	SN74259	SN74ALS259
25LS533	SN74ALS533	SN74ALS533	9341	SN74181	SN74AS181/AS881
25LS534	SN74ALS534	SN74ALS534	9342	SN74182	SN74AS882

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

FAIRCHILD

Example of order code:



FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
9601	SN29601	
9000	SN29000	SN54276/SN74276
9H00	SN54H00/SN74H00	SN74ALS1000
9L00	SN54LS00/SN74LS00	SN74ALS00A
9N00	SN5400/SN7400	SN74ALS00A
9S00	SN54S00/SN74S00	SN74ALS1000
9001		SN54276/SN74276
	SN29001	SN54376/SN74376
9H01	SN54H01/SN74H01	SN74ALS1003
9N01	SN5401/SN7401	SN74ALS03A
9002	SN7400, SN5400	SN74ALS00A
9N02	SN5402/SN7402	SN74ALS02
9S02	SN54S02/SN74S02	SN74ALS1002
9003	SN29003/SN7410, SN5410	SN74ALS10
9N03	SN5403/SN7403	SN74ALS03
9S03	SN54S03/SN74S03	SN74'ALS1003
9004	SN29004/SN7420, SN5420	SN74ALS20
9H04	SN54H04/SN74H04	SN74ALS1004
9L04	SN54LS04/SN74LS04	SN79ALS04
9N04	SN5404/SN7404	SN74ALS04
9S04	SN54S04/SN74S04	SN74ALS1004
9005	SN29005/SN7450, SN5450	SN5450/SN7450
9H05	SN54S05/SN74S05	SN74ALS1005
9S05	SN54S05/SN74S05	SN74ALS1005
9006	SN5460/SN7460	SN5460/SN7460
9N06	SN5406/SN7406	SN5406/SN7406
9007	SN29007	SN74ALS133
9N07	SN5407/SN7407	SN5407/SN7407
9008	SN29008	SN54S65/74S65
9N08	SN5408/SN7408	SN74ALS08
9S08	SN54S08/SN74S08	SN74ALS1008
9009	SN29009/SN7440, SN5440	SN54S140/SN74S140
9N09	SN5409/SN7409	SN74ALS09
9S09	SN54S09/SN74S09	SN74ALS09
9H10	SN54H10/SN74H10	SN74ALS1010
9N10	SN5410/SN7410	SN74ALS10
9S10	SN54S10/SN74S10	SN74ALS1010
9H11	SN54H11/SN74H11	SN74ALS1011
9S11	SN54S11/SN74S11	SN74ALS1011
9012	SN2901/SN7403, SN5403	SN74ALS03A
9N12	SN5412/SN7412	SN74ALS12
9N13	SN5413/SN7413	SN74LS13
9014		SN54S135/SN74S135
9N14	SN5414/SN7414	SN74LS14
9015		SN74ALS02
9S15	SN54S15/SN74S15	SN74ALS15
9016	SN29016/SN7404, SN5404	SN74ALS240
9N16	SN5416/SN7416	SN5416/SN7416
9017	SN5405/SN7405	SN74ALS241
9N17	SN5417/SN7417	SN5417/SN7417
9020		SN74276
9H20	SN54H20/SN74H20	SN74ALS1020
9N20	SN5420/SN7420	SN74ALS20
9S20	SN54S20/SN74S20	SN74ALS1020
9H21	SN54H21/SN74H21	SN74ALS15
9022		SN74376
9H22	SN54H22/SN74H22	SN74ALS22A
9S22	SN54S22/SN74S22	SN74ALS22A
9N23	SN5423/SN7423	SN5423/SN7423
9024	SN29024/SN74109A,SN54109A	SN54276/SN74276 SN54376/SN74376
9L24	SN54LS109A/SN74LS109A	SN74ALS109
9N25	SN5425/SN7425	SN5425/SN7425
9N26	SN5426/SN7426	SN74LS26
9N27	SN5427/SN7427	SN74ALS27
9H30	SN54H30/SN74H30	SN74ALS30
9N30	SN5430/SN7430	SN74ALS30
9S30	SN54S30/SN74S30	SN74ALS30
9N32	SN5432/SN7432	SN74ALS32
9S32	SN54S32/SN74S32	SN74ALS1032
9N37	SN5437/SN7437	SN74ALS37
9N38	SN5438/SN7438	SN74ALS38
9H40	SN54H40/SN74H40	SN74ALS40
9N40	SN5440/SN7440	SN74ALS40
9S40	SN54S40/SN74S40	SN74ALS40
9H50	SN54H50/SN74H50	SN54S51/SN74S51
9N50	SN5450/SN7450	SN5450/SN7450
9H51	SN54H51/SN74H51	SN54S51/SN74S51
9N51	SN5451/SN7451	SN5451/SN7451
9S51	SN54S51/SN74S51	SN54S51/SN74S51
9H52	SN54H52/SN74H52	SN54S51/SN74S51
9LS168	SN54LS668/SN74LS668	SN54ALS168/SN74ALS168
9LS169	SN54LS169B/SN74LS169B	SN54ALS169/SN74ALS169

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II

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FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
9N53	SN5453/SN7453	SN5453/SN7453
9H54	SN54H54/SN74H54	SN74LS54
9L54		SN54LS54/SN74LS54
9N54	SN5454/SN7454	SN74LS54
9H55	SN54H55/SN74H55	SN54S65/SN74S65
9H60	SN54H60/SN74H60	SN74ALS1011
9N60	SN5460/SN7460	SN5460/SN7460
9H61	SN54H61/SN74H61	SN74ALS1011
9H62	SN54H62/SN74H62	SN54H62/SN74H62
9S64	SN54S64/SN74S64	SN54S64/SN74S64
9S65	SN54S65/SN74S65	SN54S65/SN74S65
9N70	SN5470/SN7470	SN5470/SN7470
9H71	SN54H71/SN74H71	SN74ALS112
9H72	SN54H72/SN74H72	SN74ALS112
9N72	SN5472/SN7472	SN5472/SN7472
9H73	SN54H73/SN74H73	SN74ALS113
9N73	SN5473/SN7473	SN74LS73A
9H74	SN54H74/SN74H74	SN74ALS74
9N74	SN5474/SN7474	SN74ALS74
9S74	SN54S74/SN74S74	SN74ALS74
9N75	SN5475/SN7475	SN74LS75
9H76	SN54H76/SN74H76	SN74ALS112
9N76	SN5476/SN7476	SN5476/SN7476
9H78	SN54H78/SN74H78	SN74ALS114
9L86	SN5486/SN7486	SN54LS86/SN74LS86
9N86	SN5486/SN7486	SN74LS86
9S86	SN54S86/SN74S86	SN54S86/SN74S86
9H101	SN54H101/SN74H101	SN74ALS112
9H102	SN54H102/SN74H102	SN74ALS112
9H103	SN54H103/SN74H103	SN74ALS113
9H106	SN54H106/SN74H106	SN74ALS112
9H107	SN54107/SN74107	SN54107/SN74107
9N107	SN54107/SN7407	SN54107/SN74107
9H108	SN54H108/SN74H108	SN74ALS114
9S112	SN54S112/SN74S112	SN74ALS112
9S113	SN54S113/SN74S113	SN74ALS113
9S114	SN54S114/SN74S114	SN74ALS114
9N122	SN54122/SN74122	SN54122/SN74122
9N123	SN54123/SN74123	SN54123/SN74123
9N132	SN54132/SN74132	SN74LS132
9S132	SN54S132/SN74S132	SN54S132/SN74S132
9S133	SN54S133/SN74S133	SN74ALS133
9S134	SN54S134/SN74S134	SN54S134/SN74S134
9S135	SN54S135/SN74S135	SN54S135/SN74A135
9S140	SN54S140/SN74S140	SN54S140/SN74S140
9N279	SN54279/SN74279	SN74LS279
9300	SN29300/SN74195	SN74ALS299
93H00	SN54S195/SN74S195	SN54S195/SN74S195
93L00	SN54LS195A/SN74LS195A	SN54LS195A/SN74LS195A
93S00	SN54S195/SN74S195	SN54S195/SN74S195

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
9301	SN39301/SN29301	SN74LS42
93L01		SN74LS42
9302		SN74LS42
9304		SN74LS183
9305		SN54S169/SN74S169
93S05		SN54S169/SN74S169
9307	SN5448A/SN7448A	SN74LS48
9308	SN29308/SN74116	SN54116/SN74116
9309	SN39309/SN29309	SN74LS153
93L09		SN74ALS153
9310	SN29310/SN74160	SN54162/SN74S162
93S10		SN54S162/SN74S162
9311	SN39311/SN54154 SN29311/SN74154	SN54154/SN74154
93L11		SN74154
9312	SN39312/SN29312	SN74LS151
93S12		SN54S151/SN74S151
9313		SN74LS251
9314		SN74LS273
93L14		SN74LS75
9315	SN54141	SN74141
9316	SN29316/SN74161	SN54163/SN74S163
93S16		SN54S163/SN74S163
9317B	SN5446A/SN7446A	SN5446A/SN7446A
9317C	SN5446A/SN7446A	SN5446A/SN7446A
9318	SN29318/SN74148	SN74LS198
93L21	SN54LS139A/SN74LS139A	SN54LS139A/SN74LS139A
9321	SN54S139/SN74S139	SN54S139/SN74S139
9322	SN29322/SN74157	SN74LS157
93L22		SN74LS157
93S22	SN54S157/SN74S157	SN54S157/SN74S157
9324		SN54S85/SN74S85
93L24		SN74LS85
9325	SN74141	SN74141
9328		SN74LS91
93L28		SN74LS91
9334	SN54259/SN74259	SN54LS259/SN74LS259
9338		SN74172
9340		SN54S281/SN74S281
93L40		SN54LS181/SN74LS181
9341	SN54181/SN74181	SN74AS881
93S41	SN54S181/SN74S181	SN74AS881
9342	SN54182/SN74182	SN74AS882
93S42	SN54S182/SN74S182	SN74AS882
93S43		SN74S274
9344		SN74S274
9345	SN5445/SN7445	SN5445/SN7445
93S46		SN54S85/SN74S85
93S47		SN54S85/SN74S85
9348		SN54S280/SN74S280
9349	SN54180/SN74180	SN54180/SN74180

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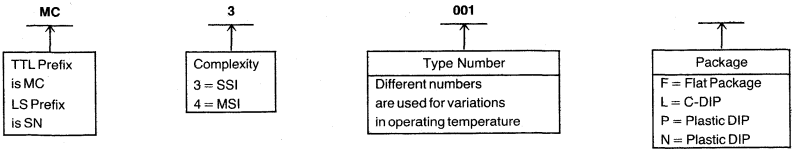
FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
9350	SN54290/SN74290	SN74LS290
9352	SN5442A/SN7442A	SN74LS42
9353	SN5443A/SN7443A	SN5443A/SN7443A
9354	SN5444A/SN7444A	SN5444A/SN7444A
9356	SN54293/SN74293	SN74LS293
9357A	SN5446A/SN7446A	SN5446A/SN7446A
9357B	SN5447A/SN7447A	SN74LS47
9358	SN5448/SN7448	SN74LS48
9359	SN5449/SN7449	SN74LS49
9360	SN54192/SN74192	SN74LS192
93S62		SN54S280/SN74S280
9366	SN54193/SN74193	SN74LS193
9368C		SN54143/SN74143
9370C		SN54144/SN74144
93H72		SN54S194/SN74S194
9374C		SN54143/SN74143
9375	SN5475/SN7475	SN74LS175
9377	SN5477/SN7477	SN74LS175
9380	SN5480/SN7480	SN5480/SN7480
9382	SN5482/SN7482	SN5482/SN7482
9383	SN5483A/SN7483A	SN74S283
9386	SN54LS266/SN74LS266	SN54LS266/SN74LS266
93H87	SN54H87/SN74H87	SN54H87/SN74H87
9390	SN5490A/SN7490A	SN74LS290
9391	SN5491A/SN7491A	SN74LS91
9392	SN5492A/SN7492A	SN74LS92
9393	SN5493A/SN7493A	SN74LS293
9394	SN5494/SN7494	SN5494/SN7494
9395	SN5495A/SN7495A	SN74LS95B
9396	SN5496/SN7496	SN74LS96
93S137		SN54S138/SN74S138
93S138	SN54S138/SN74S138	SN54S138/SN74S138
93S139	SN54S139/SN74S139	SN54S139/SN74S139
93141C	SN74141	SN74141
93145	SN54145/SN74145	SN74LS145
93150	SN54150/SN74150	SN54150/SN74150
93151	SN54151/SN74151	SN74LS151
93S151	SN54S139/SN74S139	SN54S139/SN74S139
93152	SN54152/SN74152	SN74LS151
93153	SN54153/SN74153	SN74LS153
93S153	SN54S153/SN74S153	SN54S153/SN74S153
93155	SN54155/SN74155	SN74LS155

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
93156	SN54156/SN74156	SN74LS156
93157	SN54157/SN74157	SN74LS157
93S157	SN54S157/SN74S157	SN54S157/SN74S157
93S158	SN54S158/SN74S158	SN54S158/SN74S158
93160	SN54160/SN74160	SN74LS160A
93161	SN54161/SN74161	SN74LS161A
93162	SN54162/SN74162	SN74LS162A
93163	SN54163/SN74163	SN74LS163A
93164	SN54164/SN74164	SN74LS164
93165	SN54165/SN74165	SN74LS165
93166	SN54166/SN74166	SN74LS166
93170	SN54170/SN74170	SN74LS170
93174	SN54174/SN74174	SN74LS174
93175	SN54175/SN74175	SN74LS175
93176	SN54176/SN74176	SN54176/SN74176
93177	SN54177/SN74177	SN54177/SN74177
93178	SN54178/SN74178	SN54178/SN74178
93179	SN54179/SN74179	SN54179/SN74179
93180	SN54180/SN74180	SN54180/SN74180
93H183	SN54H183/SN74H183	SN74LS183
93190	SN54190/SN74190	SN74LS190
93191	SN54191/SN74191	SN74LS191
93194	SN54194/SN74194	SN74LS194A
93S194	SN54194/SN74194	SN54S194/SN74S194
93195	SN54195/SN74195	SN74LS195A
93196	SN54196/SN74196	SN74LS196
93197	SN54197/SN74197	SN74LS197
93198	SN54198/SN74198	SN54198/SN74198
93199	SN54199/SN74199	SN54199/SN74199
93S251	SN54S251/SN74S251	SN54S251/SN74S251
93S257	SN54S257/SN74S257	SN54S257/SN74S257
93S258	SN54S258/SN74S258	SN54S258/SN74S258
95137		SN54LS137/SN74LS137
74LS568	SN74ALS568	SN74ALS569
74LS569	SN74ALS569	SN74ALS569
74LS573	SN74ALS573	SN74ALS573
74LS574	SN74ALS574	SN74ALS574
9600		SN54221/SN74221
9601		SN54122/SN74122
9602		SN54123/SN74123
9603	SN54121/SN74121	SN54221/SN74221

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II

MOTOROLA

Example of Motorola order code:



MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3000	SN74H00	SN74500/ALS00/ALS1000
MC3001	SN7408	SN74511/ALS11/ALS1011
MC3002		SN74502/ALS02/ALS1002
MC3003	SN7432	SN74ALS32/ALS1032
MC3004	SN74H01	SN74503/ALS03/ALS1003
MC3005	SN74H10	SN74510/ALS10/ALS1010
MC3006	SN74H11	SN74511/ALS11/ALS1011
MC3007		SN74515/ALS515
MC3008	SN74H04	SN74504/ALS04/ALS1004
MC3009	SN74H05	SN74505/ALS05/ALS1005
MC3010	SN74H20	SN74520/ALS20/ALS1020
MC3011	SN74H21	SN74511/ALS11/ALS1011
MC3012	SN74H22	SN74S22/ALS22A
MC3015		SN74S133/S134/ALS133
MC3016	SN74H30	SN74S133/ALS133
MC3018	SN74H62	SN74S11/ALS11/ALS1011
MC3019	SN74H61	SN74S11/ALS11/ALS1011
MC3020	SN74H50	SN74S51
MC3021	SN74S86	SN74S86/ALS86
MC3022		SN74S135
MC3023	SN74H51	SN74S51
MC3024	SN74H40	SN74S40/ALS40
MC3025	SN74H40	SN74S40/ALS40
MC3026		SN74S140
MC3028		SN74S240/S241/ALS240/ALS241
MC3029		SN74S240/S241/ALS240/ALS241
MC3030	SN74H60	SN74S11/ALS11/ALS1011
MC3031	SN74H52	SN74S64
MC3032	SN74H53	SN74S64
MC3033	SN74H54	SN74S64
MC3034	SN74H55	SN74S64
MC3050		SN74S373/S374/ALS573/ALS574
MC3051		SN74S373/S374/ALS513/ALS514
MC3052		SN74S373/S374/ALS513/ALS514
MC3053		SN74S374/ALS374
MC3054	SN74H71	SN74S112/ALS112
MC3055	SN74H72	SN74S112/ALS112
MC3060	SN74H74	SN74S14/ALS14
MC3061	SN74S114	SN74S114/ALS114
MC3062	SN74S113	SN74S113/ALS113
MC3063	SN74H73	SN74112/ALS112

MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3107		SN54S15/SN74ALS15
MC3108	SN54H04	SN54S04/SN74ALS04/SN74ALS1004
MC3109	SN54H05	SN54S05/SN74ALS05/SN74ALS1005
MC3110	SN54H20	SN54S20/SN74ALS20A/SN74ALS1020
MC3111	SN54H21	SN54S11/SN74ALS11/SN74ALS1011
MC3112	SN54H22	SN54S22/SN74ALS22A
MC3115		SN54S133/SN54S134/SN74ALS133
MC3116	SN54H30	SN54S133/SN74ALS133
MC3118	SN54H62	SN54S11/SN74ALS11/SN74ALS1011
MC3119	SN54H61	SN54S11/SN74ALS11/SN74ALS1011
MC3120	SN54H50	SN54S51
MC3121	SN54S86	SN54S86/SN74ALS86
MC3122		SN54S135
MC3123	SN54H51	SN54S51
MC3124	SN54H40	SN54S40/SN74ALS40
MC3125	SN54H40	SN54S40/SN74ALS40
MC3126		SN54S37/SN54S38/SN74ALS38/SN74ALS37
MC3128		SN54S37/SN54S38/SN74ALS37/SN74ALS38
MC3129		SN54S37/SN54S38/SN74ALS37/SN74ALS38
MC3130	SN54H60	SN54S11/SN74ALS11/SN74ALS1011
MC3131	SN54H52	SN54S64
MC3132	SN54H53	SN54S64
MC3133	SN54H54	SN54S64
MC3134	SN54H55	SN54S64
MC3150		SN54S373/SN54S374/SN74ALS573/574
MC3151		SN54S373/SN54S374/SN74ALS573/574
MC3152		SN54S373/SN54S374/SN74ALS573/574
MC3154	SN54H71	SN54S112/SN74ALS112
MC3155	SN54H72	SN54S112/SN74ALS112
MC3160	SN54H74	SN54S74/SN74ALS74
MC3161	SN54S114	SN54S114/SN74ALS114
MC3162	SN54S113	SN54S113/SN74ALS113
MC3163	SN54H73	SN54S112/SN74ALS112
MC4000		SN74S139/SN74ALS139
MC4001		SN74184/SN74185A
MC4002		SN74S139/SN74ALS139
MC4004	SN7481A	SN7481A
MC4005	SN7481A	SN7481A
MC4006		SN74S138/SN74ALS138
MC4007		SN74S139/SN74ALS139
MC4008		SN74S280

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

MOTOROLA

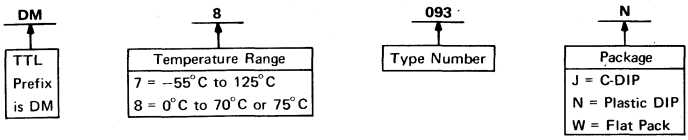
MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3100	SN54H00	SN54S00/ALS00/ALS1000
MC3102	SN5408	SN54S11/ALS11/ALS1011
MC3102		SN54S02/ALS02/ALS1002
MC3103	SN5432	SN5432/ALS32/ALS1032
MC3104	SN54H01	SN54S03/ALS03/ALS1003
MC3105	SN54H10	SN54S10/ALS10/ALS1010
MC3106	SN54H11	SN54S11/ALS11/ALS1011
MC4010		SN74S135
MC4012		SN74S299/ALS299
MC4015		SN74S195
MC4016		SN74S168/ALS168
MC4017		SN74S158/ALS168
MC4018		SN74S169/ALS169
MC4019		SN74S169/ALS169
MC4021		SN74S85
MC4022		SN74S85
MC4023		SN74S260
MC4025		SN74S124
MC4026		SN74S381
MC4027		SN74S381
MC4028		SN74S281
MC4029		SN74S281
MC4030		SN74S281
MC4031		SN74S281
MC4032		SN74S182
MC4035		SN74S373/ALS573, SN74S374/ALS574
MC4037		SN74S373/ALS573, SN74S374/ALS574
MC4038		SN74S138/ALS138
MC4039		SN74S143, SN74S144
MC4040		SN74S139/ALS139
MC4042		SN74S240/ALS240, SN74S241/ALS241
MC4043		SN74S240/ALS240, SN74S241/ALS241
MC4048		SN74S138/ALS138
MC4050		SN74143
MC4051		SN74144

MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC4062		SN74S64
MC4300		SN54S139/ALS139
MC4304	SN5481A	SN5481A
MC4305	SN5481A	SN5481A
MC4306		SN54S138/ALS138
MC4307		SN54S138/ALS138, SN54S139/ALS139
MC4308		SN54S280
MC4310		SN54S280
MC4316		SN54S168/ALS168
MC4317		SN54S168/ALS168
MC4318		SN54S169/ALS169
MC4319		SN54S169/ALS169
MC4324		SN54S124
MC4326		SN54S381
MC4327		SN54S381
MC4328		SN54S281
MC4329		SN54S281, SN54S281
MC4330		SN54S281, SN74S381
MC4331		SN54S281
MC4335		SN54S373/ALS573, SN54S374/ALS574
MC4337		SN54S373/ALS573, SN54S374/ALS574
MC4350		SN54143
MC9310	SN54160	SN74LS160A/ALS160
MC9311	SN54154	SN54154
MC9316	SN54161	SN74LS161A/ALS161
MCM4004	SN7481A	SN7481A
MCM4005	SN7481A	SN7481A
74LS568	74ALS568	74ALS568
74LS569	74ALS569	74ALS569
74LS573	74ALS573	74ALS573
74LS574	74ALS574	74ALS574
SN74LS795	SN74LS465	SN74LS465/ALS465
SN74LS796	SN74LS466	SN74LS466/ALS466
SN74LS797	SN74LS467	SN74LS467/ALS467
SN74LS798	SN74LS468	SN74LS468/ALS468

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II

NATIONAL

Example of Motorola order code:



NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
16149	SN54$436	SN54$436
16179	SN54$437	SN54$437
36149	SN74$436	SN74$436
36179	SN74$437	SN74$437
7091		SN54LS37/SN54ALS37
7093	SN54125	SN54LS125A
7094	SN54126	SN54LS126A
7095	SN54365	SN54LS365A
7096	SN54366	SN54LS366A
7097	SN54367	SN54LS367A
7098	SN54368	SN54LS368A
7121	SN54251	SN54LS251
71L22	SN54L157	SN54LS157
7123	SN54S257	SN54LS257
7130		SN54S85/SN54LS85
7131		SN54S85/SN54LS85
7136		SN54LS85
7160		SN54S85/SN54LS85
7200		SN54S85/SN54LS85
7210		SN54LS151
7211		SN54LS151
7213	SN54154	SN54154
7214	SN54LS253	SN54LS253
7219		SN54150
7220		SN54S280
7223		SN54S139/ALS139
7230		SN54S257
7280	SN54176	SN54176
7281	SN54177	SN54177
7283	SN5483A	SN54LS83A
7288		SN54LS83A
7290	SN54196	SN54LS196
7291	SN54197	SN54LS197
7511		SN54376
7512		SN54376
7520		SN5497
7544		SN54265
7551	SN54173	SN54LS173A
7552		SN54S162/ALS162
8093	SN74125	SN74LS125A
8094	SN74126	SN74LS126A

NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8095	SN74365	SN74LS365
8096	SN74366	SN74LS366
8097	SN74367	SN74LS467
8098	SN74368	SN74LS368
7553		SN54S163/ALS163
7554		SN54S373/SN54S374/ALS573/ALS574
7555		SN54S168/ALS168
7556		SN54S169/ALS169
7560	SN54192	SN54192/SN54LS192
75L60	SN54L192	SN54LS192
7563	SN54193	SN54LS193
75L63	SN54L193	SN54LS193
7570	SN54164	SN54LS164
7590	SN54165	SN54LS165A
7600		SN74LS194
7613		SN54376
76L70	SN54L164	SN54LS164
7810	5426	SN54LS26
7811		SN54LS26
7812	SN5416	SN5416
7819		SN54S240/SN54S241/ALS240/ALS241
7853		SN54LS221
7875A		SN54284
7875B		SN54285
8091		SN74S240/SN74S241/ALS240/ALS241
8551	SN74173	SN74LS173A
8552		SN74S162/ALS162
8553		SN74S163/ALS163
8554		SN74S373/SN74S374/ALS573/ALS574
8555		SN74S168/ALS168
8556		SN74S169/ALS169
8121	SN74251	SN74LS251
81L22		SN74ALS122
8123	SN74S257	SN74S257
8130		SN74S85
8131		SN74S85
8136		SN74LS85
8160		SN74S85
81LS95	SN74LS465	SN74LS465/ALS465
81LS96	SN74LS466	SN74LS466/ALS466
81LS97	SN74LS467	SN74LS467/ALS467

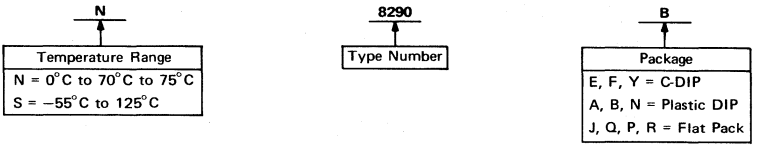
Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

NATIONAL

NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
81LS98	SN74LS468	SN74LS468/ALS468
8200		SN74S85
8210		SN74LS151
8211		SN74LS151
8213	SN74154	SN74154
8214	SN74LS253	SN74LS253
8219		SN74150
8220		SN74S280
8223		SN74S139/ALS139
8224	74LS424	SN74LS424
8230		SN74S257
8280	SN74176	SN74176
8281	SN74177	SN74177
8283	SN7483A	SN74LS83A
8288		SN74LS92
8290	SN74196	SN74LS196
8291	SN74197	SN74LS197
8296	SN74196	SN74LS196
8304		74LS245/74ALS245
8500	SN7476	SN74LS76A
8501	SN7473	SN74LS73A
8510	SN7474	SN74LS74A/ALS74
8511		SN74276
8512		SN74276
8520		SN7497
8530	SN7490A	SN74LS90
8532	SN7492A	SN74LS92
8533	SN7493A	SN74LS93
8544		SN74265
8560	SN74192	SN74LS192/ALS192
85L60	SN74L192	SN74LS192
8563	SN74193	SN74LS193/ALS193
85L63	SN74L193	SN74LS193/ALS193
8570	SN74164	SN74LS164
8579	SN74164	SN74LS164
8580	SN7495A	SN74LS95B
8590	SN74165	SN74LS165A
8640	SN74141	SN74141
86L70	SN74L164	SN74LS164
8810	SN7426	SN74LS26
8811		SN74LS26
8812		SN7416
8819		SN74LS26
8842	SN7442A	SN74LS42
8846	SN7446A	SN7446A
8847	SN7447A	SN74LS47
8848	SN7448	SN74LS48
8853		SN74LS221
8875A		SN74S274
8875B		SN74S274

SIGNETICS

Example of Signetics order code:



NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8H16		SN54S20/SN74S20/ALS20/ALS1020
8H20		SN54S112/SN74S112/ALS112
8H21		SN54S112/SN74S112/ALS112
8H22		SN54S112/SN74S112/ALS112
8H70	SN54H11/SN74H11	SN54S11/SN74S11/ALS11/ALS1011
8201		SN74LS174/ALS174
8202		SN74LS174/ALS174
8203		SN74LS174/ALS174
8204		SN54S471/SN74S471
8205		SN54S472/SN74S472
8H80	SN54H00/SN74H00	SN74S00/ALS00/ALS1000
8H90	SN54H04/SN74H04	SN74S04/ALS04/ALS1004
8T01		SN74141
8T04		SN74LS47
8T05		SN74LS48
8T06		SN74143
8T09		SN74128
8T10	SN54173/SN74173	SN74LS173A
8T13		SN74128
8T18		SN74LS26
8T20		SN74121
8T22	SN54122/SN74122	SN74122
8T23		SN74128
8T26		SN74LS125A
		SN74S240/ALS240

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

SIGNETICS

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8T28		SN74143
		SN74S241/ALS241
8T51		SN74143
		74144
8T54		SN74144
		SN74143
8T59		SN74143
		SN74144
8T71		SN74143
		SN74144
8T74		SN74143
		SN74144
8T75		SN74143
		SN74144
8T79		SN74143
		SN74144
8T80		SN74LS26
8T90		SN7406
		SN74LS125A
8T93		SN74125
		SN764LS125A
8T94		SN74425
		SN74LS125
8T95		SN74LS365
8T96		SN74LS366
8T97		SN74LS367
8T98		SN74LS368
8T245	SN54LS245/SN74LS245	SN74LS245/ALS245
8162		SN74121
8200		SN74LS174/ALS174
8260		SN74S281
8261		SN74S182
8262		SN74180
82S63		SN74S280
8263		SN74LS153
8264		SN74LS153
8266		SN74LS157
82S66		SN74S157
8224	74LS424	74LS424
8230	SN39312/SN29312	SN74LS151
82S30		SN54S151A/SN74S151A
8231		SN54S251/SN74S251
82S31		SN54S151/SN74S151
8232		SN74LS151
82S32		SN54S151/SN74S151
8233		SN74LS157
82S33		SN54S157/SN74S157
8234		SN54S258/SN74S258
82S34		SN54S258/SN74S258
8241		SN74LS86/ALS86
82S41		SN54S86/SN74S86
8242	SN54LS266/SN74LS266	SN54LS266/SN74LS266

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
82S42		SN54S135/SN74S135
8243		SN54198/SN74198
8250		SN74SN74LS42
82S50		SN74LS138/ALS138
8252	SN39301/SN29301	SN74LS42
82S52		SN54S280/SN74S280
8255	SN54S289/SN74S289	SN54S289/SN74S289
82147	SN54147/SN74147	SN74LS147
82148	SN54148/SN74148	SN74LS148
8415		SN74LS20/ALS20A
8416		SN74LS20/ALS20A
8417		SN74LS10/ALS10/ALS1010
8424		SN54111/SN74111
8425		SN54111/SN74111
8440		SN5450/SN7450
8267		SN74LS157
8268	SN5480/SN7480	SN74LS181
8269		SN74LS83
8270	SN54178/SN74178	SN74LS194A
82S70		SN74S299/ALS299
8271	SN54179/SN74179	SN74LS194A
82S71		SN74S299/ALS299
8273		SN74198
8274		SN74198
8275		SN74LS174
8276		SN74LS91
8277		SN74LS91
8280	SN54176/SN74176	SN74176
8281	SN54177/SN74177	SN74177
8283		SN74S69/ALS169
8284		SN74S169/ALS169
8285		SN74S169/ALS169
8288		SN74LS163A/ALS163
8290	SN54196/SN74196	SN74LS196
82S90	SN54S196/SN74S196	SN74S196
8291	SN54197/SN74197	SN74LS197
82S91	SN54S197/SN74S197	SN74S197
8292	SN54LS196/SN74S196	SN74LS196
8293	SN54LS197/SN74LS197	SN74LS197
82S130	SN54170/SN74170	SN74LS170
8455	SN5440/SN7440	SN74LS40
8470	SN5410/SN7410	SN74LS10/ALS10/ALS1010
8471	SN5412/SN7412	SN74LS12/ALS12
8480	SN5400/SN7400	SN74LS00/ALS00/ALS1000
8481	SN5403/SN7403	SN74LS03/ALS03/ALS1003
8490	SN5404/SN7404	SN74LS04/ALS04/ALS1004
8706		SN5460/SN7460
8731		SN5460/SN7460
8806	SN5460/SN7460	SN5460/SN7460
8808	SN5430/AN7430	SN74LS30/ALS30
8815	SN5425/SN7425	SN5425/SN7425
8816	SN5425/SN7425	SN5425/SN7425

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

SIGNETICS

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8821		SN74LS76A
8822		SN74LS107A
8824		SN74LS76A
8825		SN5470/SN7470
8826		SN74LS107A
8827		SN74LS76A
8828	SN5474/SN7474	SN74LS74A/ALS74
8829	SN54110/SN74110	SN54110/SN74110
8840	SN5450/SN7450	SN5450/SN7450
8848	SN54H54/SN74H74	SN54S64/SN74S64
8855		SN74LS40

SIGNETS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8859	SN5450/SN7450	SN5450/SN7450
8870		SN74LS10/ALS10/ALS1010
8875	SN5427/SN7427	SN74LS27
8879	SN5410/SN7410	SN74LS10/ALS10/ALS1010
8880		SN74LS00/ALS00A/ALS1000
8881	SN5401/SN7401	SN74LS01/ALS01
8885		SN74LS02/ALS02ALS1002
8889		SN74LS01/ALS01
8890	SN5404/SN7404	SN74LS04/ALS04/ALS1004
8891	SN5405/SN7405	SN74LS05/ALS05/ALS1005

2

Please note: Details of all Texas Instruments AS and ALS products are contained in TTL Data Book Vol II.

General Information

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I – OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Clock Frequency

Maximum clock frequency, f_{max}
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transistions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

Current

High-level input current, I_{IH}
The current into* an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into* an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state output current, $I_{O(off)}$
The current flowing into* an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current, I_{CC}
The current into* the V_{CC} supply terminal of an integrated circuit.

*Current out of a terminal is given as a negative value.

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})†
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}†
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})†
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}†
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

†On older data sheets, similar symbols without the P subscript were used; i.e. t_{ZH}, t_{ZL}, t_{HZ}, and t_{LZ}.

Pulse Width

Pulse width, t_w
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Recovery Time

Sense recovery time, t_{SR}
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

Release Time

Release time, $t_{release}$
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

Setup Time

Setup time, t_{su}
The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Transition Time

Transition time, low-to-high-level, t_{TLH}
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

Transition time, high-to-low-level, t_{THL}
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

Voltage

High-level input voltage, V_{IH}
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Input clamp voltage, V_{IK}
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

Low-level input voltage, V_{IL}
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}
The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Negative-going threshold voltage, V_{T-}
The voltage level at an input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

Off-state output voltage, $V_{O(off)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

On-state output voltage, $V_{O(on)}$
The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

Positive-going threshold voltage, V_{T+}
The voltage level at an input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

PART II – CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration, LSI

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration, MSI

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Small-Scale Integration, SSI

Integrated circuits of less complexity than medium-scale integration (MSI).

Very-Large-Scale Integration, VLSI

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 1000 or more gates or circuitry of similar complexity.

EXPLANATION OF FUNCTION TABLES

The following symbols are now being used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were establsihed
$\bar{Q}_0$	=	complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each active transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\bar{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Amoung the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register, e.g., type SN74194.

FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the clock remains high or on the high-to-low transition of the clock.

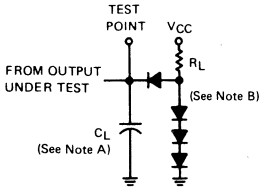
The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A will be at output Q_A, data entered at B will be at Q_B, and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at Q_A is now at Q_B, the previous levels of Q_B and Q_C are now at Q_C and Q_D respectively, and the data previously at Q_D is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

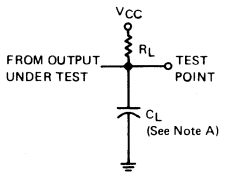
The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at Q_B is now at Q_A, the previous levels of Q_C and Q_D are now at Q_B and Q_C, respectively, and the data previously at Q_A is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both mode inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

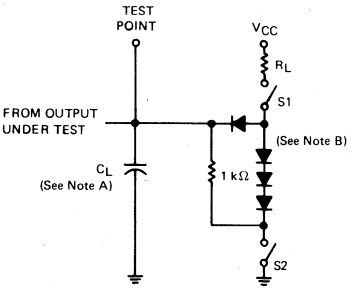
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

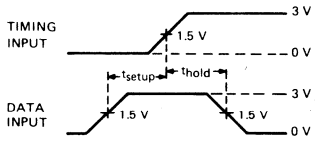


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

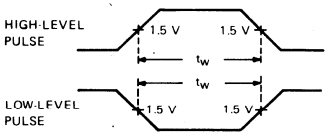


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

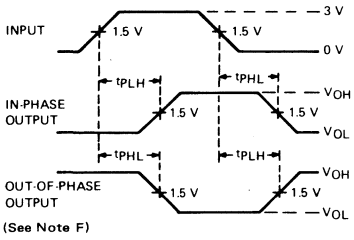
NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



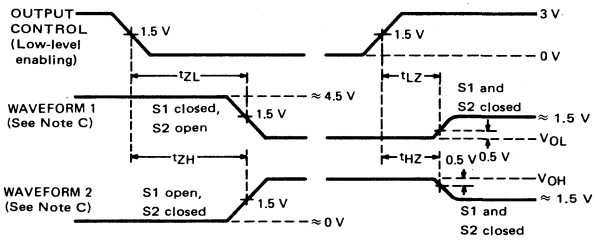
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



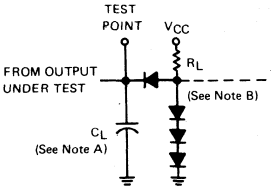
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



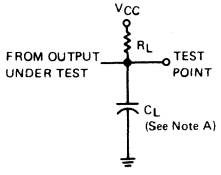
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$ and:
For Series 54/74 and 54H/74H, $t_r \leq 7$ ns, $t_f \leq 7$ ns;
For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

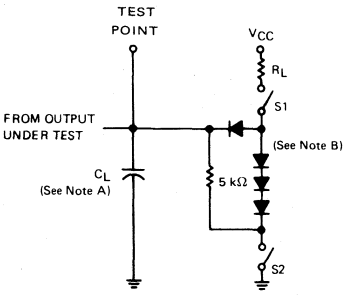
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

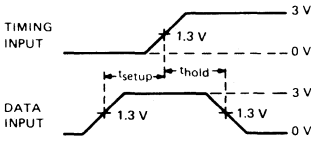


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

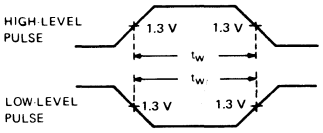


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

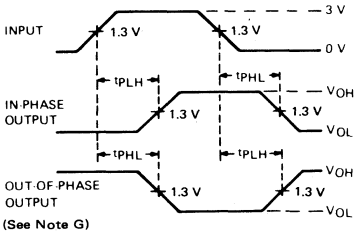
NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



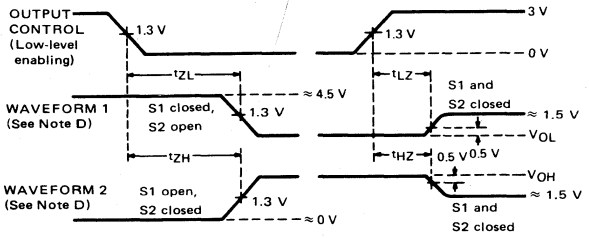
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$ and: For Series 54LS/74LS, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

Explanation of New Logic Symbols

EXPLANATION OF NEW LOGIC SYMBOLS

TABLE OF CONTENTS

LIST OF TABLES

If you have questions on this Explanation of New Logic Symbols, please contact:

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Dallas, Texas 75265
Telephone (214) 995-3746

IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

by F. A. Mann

1 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be explained in Section 4.

The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

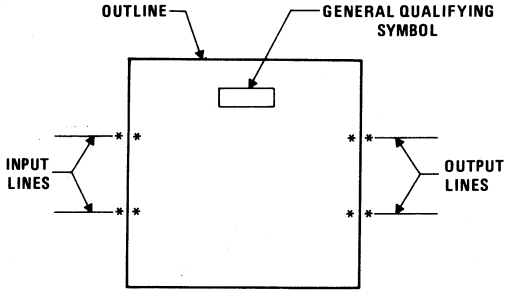
Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this TTL Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions of the TTL Data Book will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book; comparing the symbols with functional block diagrams and/or function tables will further help that understanding.

2 SYMBOL COMPOSITION

A symbol comprises an outline or a combination of outlines together with one or more qualifying symbols. The shape of the symbols is not significant. As shown in Figure 1, general qualifying symbols are used to tell exactly what logical operation is performed by the elements. Table I shows the general qualifying symbols used in this data book. Input lines are placed on the left and output lines are placed on the right. When an exception is made to that convention, the direction of signal flow is indicated by an arrow as shown in Figure 11.

All outputs of a single, unsubdivided element always have identical internal logic states determined by the function of the element except when otherwise indicated by an associated qualifying symbol or label inside the element.



*Possible positions for qualifying symbols relating to inputs and outputs

FIGURE 1 – SYMBOL COMPOSITION

The outlines of elements may be abutted or embedded in which case the following conventions apply. There is no logic connection between the elements when the line common to their outlines is in the direction of signal flow. There is at least one logic connection between the elements when the line common to their outlines is perpendicular to the direction of signal flow. The number of logic connections between elements will be clarified by the use of qualifying symbols and this is discussed further under that topic. If no indications are shown on either side of the common line, it is assumed there is only one connection.

When a circuit has one or more inputs that are common to more than one element of the circuit, the common-control block may be used. This is the only distinctively shaped outline used in the IEC system. Figure 2 shows that unless otherwise qualified by dependency notation, an input to the common-control block is an input to each of the elements below the common-control block.

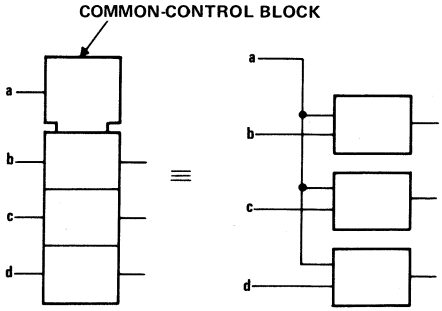


FIGURE 2 – ILLUSTRATION OF COMMON- CONTROL BLOCK

A common output depending on all elements of the array can be shown as the output of a common-output element. Its distinctive visual feature is the double line at its top. In addition the common-output element may have other inputs as shown in Figure 3. The function of the common-output element must be shown by use of a general qualifying symbol.

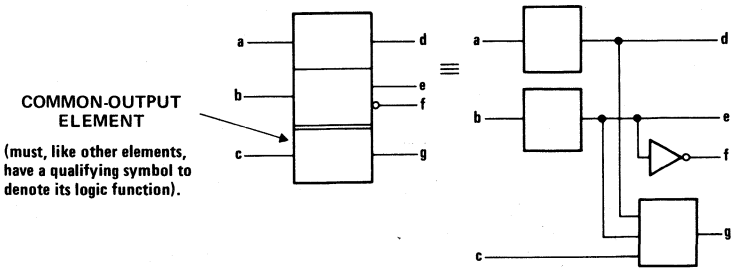


FIGURE 3 – ILLUSTRATION OF COMMON-OUTPUT ELEMENT

3 QUALIFYING SYMBOLS

3.1 General Qualifying Symbols

Table I shows the general qualifying symbols used in this data book. These characters are placed near the top center or the geometric center of a symbol or symbol element to define the basic function of the device represented by the symbol or of the element.

3.2 Qualifying Symbols for Inputs and Outputs

Qualifying symbols for inputs and outputs are shown in Table II and will be familiar to most users with the possible exception of the logic polarity and analog signal indicators. The older logic negation indicator means that the external 0 state produces the internal 1 state. The internal 1 state means the active state. Logic negation may be used in pure logic diagrams; in order to tie the external 1 and 0 logic states to the levels H (high) and L (low), a statement of whether positive logic (1 = H, 0 = L) or negative logic (1 = L, 0 = H) is being used is required or must be assumed. Logic polarity indicators eliminate the need for calling out the logic convention and are used in this data book in the symbology for actual devices. The presence of the triangular polarity indicator indicates that the L logic level will produce the internal 1 state (the active state) or that, in the case of an output, the internal 1 state will produce the external L level. Note how the active direction of transition for a dynamic input is indicated in positive logic, negative logic, and with polarity indication.

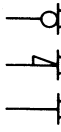
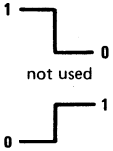
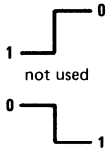
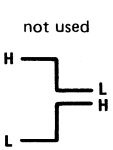
EXPLANATION OF NEW LOGIC SYMBOLS

TABLE I – GENERAL QUALIFYING SYMBOLS

SYMBOL	DESCRIPTION	EXAMPLE
&	AND gate or function.	SN7400
≥1	OR gate or function. The symbol was chosen to indicate that at least one active input is needed to activate the output.	SN7402
=1	Exclusive OR. One and only one input must be active to activate the output.	SN7486
=	Logic identity. All inputs must stand at same state.	SN74180
2k	An even number of inputs must be active.	SN74180
2k+1	An odd number of inputs must be active.	*
1	The one input must be active.	SN7404
▷ or ◁	A buffer or element with more-than usual output capability (symbol is oriented in the direction of signal flow).	SN74S436
⊓	Schmitt trigger; element with hysteresis.	SN74LS18
X/Y	Coder, code converter (DEC/BCD, BIN/OUT, BIN/7-SEG, etc.).	SN74LS347
MUX	Multiplexer/data selector.	SN74150
DMUX or DX	Demultiplexer.	SN74138
Σ	Adder.	SN74LS385
P–Q	Subtracter.	SN74LS385
CPG	Look-ahead carry generator.	SN74182
π	Multiplier.	SN74LS384
COMP	Magnitude comparator.	SN74LS682
ALU	Arithmetic logic unit.	SN74LS381
⎍	Retriggerable monostable.	SN74LS422
1⎍	Non-retriggerable monostable (one-shot).	SN74121
G	Astable element. Showing waveform is optional.	SN74LS320
!G	Synchronously starting astable.	SN74LS624
G!	Astable element that stops with a completed pulse.	
SRGm	Shift register. m = number of bits.	SN74LS595
CTRm	Counter. m = number of bits; cycle length = 2^m.	SN54LS590
CTR DIVm	Counter with cycle length = m.	SN74LS668
ROM	Read-only memory.	*
RAM	Random-access read/write memory.	SN74170
FIFO	First-in, first-out memory.	SN74LS222

*Not all of the general qualifying symbols have been used in this book, but they are included here for the sake of completeness.

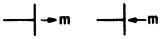
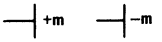
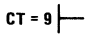
TABLE II – QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to in positive logic.
	Active-low output. Equivalent to in positive logic.
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left. If not otherwise indicated, signal flow is from left to right.
	Bidirectional signal flow.
	Dynamic inputs active on indicated transition POSITIVE LOGIC:  NEGATIVE LOGIC:  POLARITY INDICATION: 
	Nonlogic connection. A label inside the symbol will usually define the nature of this pin.
	Input for analog signals.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. Transition from 0 to 1 on left produces transitory 1 state on right.
	Internal input (virtual input). It always stands at its internal 1 state unless affected by an overriding dependency relationship.
	Internal output (virtual output). Its effect on an internal input to which it is connected is indicated by dependency notation.

The internal connections between logic elements abutted together in a symbol may be indicated by the symbols shown. Each logic connection may be shown by the presence of qualifying symbols at one or both sides of the common line and if confusion can arise about the numbers of connections, use can be made of one of the internal connection symbols.

The internal (virtual) input is an input originating somewhere else in the circuit and is not connected directly to a terminal. The internal (virtual) output is likewise not connected directly to a terminal.

TABLE III – SYMBOLS INSIDE THE OUTLINE

	Postponed output (of a pulse-triggered flip-flop). The output changes when input initiating change (e.g., a C input) returns to its initial external state or level. See § 5.
	Bi-threshold input (input with hysteresis)
	NPN open-collector or similar output that can supply a relatively low-impedance L level when not turned off. Requires external pull-up. Capable of positive-logic wired-AND connection. 
	Passive-pull-up output is similar to NPN open-collector output but is suplemented with a built-in passive pull-up.
	NPN open-emitter or similar output that can supply a relatively low-impedance H level when not turned off. Requires external pull-down. Capable of positive-logic wired-OR connection. 
	Passive-pull-down output is similar to NPN open-emitter output but is supplemented with a built-in passive pull-down.
	3-state output
	Enable input When at its internal 1-state, all outputs are enabled. When at its internal 0-state, open-collector and open-emitter outputs are off, three-state outputs are at normally defined internal logic states and at external high-impedance state, and all other outputs (e.g., totem-poles) are at the internal 0-state.
J, K, R, S, T	Usual meanings associated with flip-flops (e.g., R = reset, T = toggle)
	Data input to a storage element equivalent to: 
	Shift right (left) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Counting up (down) inputs, m = 1, 2, 3 etc. If m = 1, it is usually not shown.
	Binary grouping. m is highest power of 2.
	The contents-setting input, when active, causes the content of a register to take on the indicated value.
	The content output is active if the content of the register is as indicated.
	Input line grouping . . . . indicates two or more terminals used to implement a single logic input. e.g., The paired expander inputs of SN7450. 
	Fixed-state output always stands at its internal 1 state. For example, see SN74185.

The application of internal inputs and outputs requires an understanding of dependency notation, which is explained in Section 4.

In an array of elements, if the same general qualifying symbol and the same qualifying symbols associated with inputs and outputs would appear inside each of the elements of the array, these qualifying symbols are usually shown only in the first element. This is done to reduce clutter and to save time in recognition. Similarly, large identical elements that are subdivided into smaller elements may each be represented by an unsubdivided outline. The SN54LS440 symbol illustrates this principle.

3.3 Symbols Inside the Outline

Table III shows some symbols used inside the outline. Note particularly that open-collector, open-emitter, and three-state outputs have distinctive symbols. Also note that an EN input affects all of the outputs of the circuit and has no effect on inputs. When an enable input affects only certain outputs and/or affects one or more inputs, a form of dependency notation will indicate this (see 4.9). The effects of the EN input on the various types of outputs are shown.

It is particularly important to note that a D input is always the data input of a storage element. At its internal 1 state, the D input sets the storage element to its 1 state, and at its internal 0 state it resets the storage element to its 0 state.

The binary grouping symbol will be explained more fully in Section 8. Binary-weighted inputs are arranged in order and the binary weights of the least-significant and the most-significant lines are indicated by numbers. In this data book weights of input and output lines will be represented by powers of two usually only when the binary grouping symbol is used, otherwise, decimal numbers will be used. The grouped inputs generate an internal number on which a mathematical function can be performed or that can be an identifying number for dependency notation. See Figure 28. A frequent use is in addresses for memories.

Reversed in direction, the binary grouping symbol can be used with outputs. The concept is analogous to that for the inputs and the weighted outputs will indicate the internal number assumed to be developed within the circuit.

Other symbols are used inside the outlines in this data book in accordance with the IEC/IEEE standards but are not shown here. Generally these are associated with arithmetic operations and are self-explanatory.

When nonstandardized information is shown inside an outline, it is usually enclosed in square brackets [like these].

4 DEPENDENCY NOTATION

4.1 General Explanation

Dependency notation is the powerful tool that sets the IEC symbols apart from previous systems and makes compact, meaningful, symbols possible. It provides the means of denoting the relationship between inputs, outputs, or inputs and outputs without actually showing all the elements and interconnections involved. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function.

In the convention for the dependency notation, use will be made of the terms "affecting" and "affected". In cases where it is not evident which inputs must be considered as being the affecting or the affected ones (e.g., if they stand in an AND relationship), the choice may be made in any convenient way.

So far, ten types of dependency have been defined and all of these are used in this data book. They are listed below in the order in which they are presented and are summarized in Table IV following 4.11.

Section	Dependency Type or Other Subject
4.2	G, AND
4.3	General rules for dependency notation
4.4	V, OR
4.5	N, Negate, (Exclusive OR)
4.6	Z, Interconnection
4.7	C, Control
4.8	S, Set and R, Reset
4.9	EN, Enable
4.10	M, Mode
4.11	A, Address

4.2 G (AND) Dependency

A common relationship between two signals is to have them ANDed together. This has traditionally been shown by explicitly drawing an AND gate with the signals connected to the inputs of the gate. The 1972 IEC publication and the 1973 IEEE/ANSI standard showed several ways to show this AND relationship using dependency notation. While nine other forms of dependency have since been defined, the ways to invoke AND dependency are now reduced to one.

In Figure 4 input **b** is ANDed with input **a** and the complement of **b** is ANDed with **c**. The letter G has been chosen to indicate AND relationships and is placed at input **b**, inside the symbol. A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter G and also at each affected input. Note the bar over the 1 at input **c**.

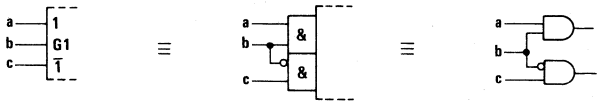


FIGURE 4 – G DEPENDENCY BETWEEN INPUTS

In Figure 5, output **b** affects input **a** with an AND relationship. The lower example shows that it is the internal logic state of **b**, unaffected by the negation sign, that is ANDed. Figure 6 shows input **a** to be ANDed with a dynamic input **b**.

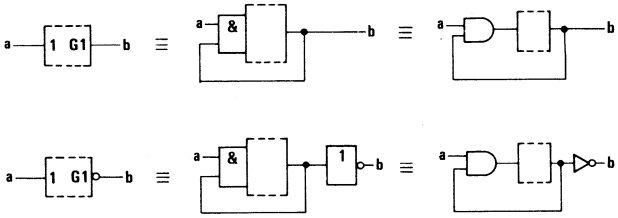


FIGURE 5 – G DEPENDENCY BETWEEN OUTPUTS AND INPUTS

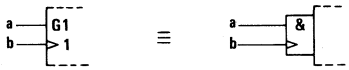


FIGURE 6 – G DEPENDENCY WITH A DYNAMIC INPUT

The rules for G dependency can be summarized thus:

When a G*m* input or output (*m* is a number) stands at its internal 1 state, all inputs and outputs affected by G*m* stand at their normally defined internal logic states. When the G*m* input or output stands at its 0 state, all inputs and outputs affected by G*m* stand at their internal 0 states.

4.3 Conventions for the Application of Dependency Notation in General

The rules for applying dependency relationships in general follow the same pattern as was illustrated for G dependency.

Application of dependency notation is accomplished by:

1) labeling the input (or output) *affecting* other inputs or outputs with the letter symbol indicating the relationship involved (e.g., G for AND) followed by an identifying number, appropriately chosen, and
2) labeling each input or output *affected* by that affecting input (or output) with that same number.

If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. See Figure 4.

If two affecting inputs or outputs have the same letter and same identifying number, they stand in an OR relationship to each other. See Figure 7.

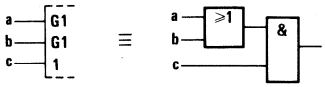


FIGURE 7 – OR'ED AFFECTING INPUTS

If the affected input or output requires a label to denote its function (e.g., "D"), this label will be *prefixed* by the identifying number of the affecting input. See Figure 12.

If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. See Figure 12.

If the labels denoting the functions of affected inputs or outputs must be numbers, (e.g., outputs of a coder), the identifying numbers to be associated with both affecting inputs and affected inputs or outputs will be replaced by another character selected to avoid ambiguity, e.g., Greek letters. See Figure 8.

FIGURE 8 – SUBSTITUTION FOR NUMBERS

4.4 V (OR) Dependency

The symbol denoting OR dependency is the letter V. See Figure 9.

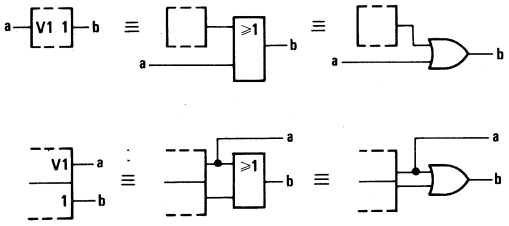
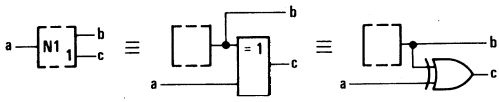


FIGURE 9 – V (OR) DEPENDENCY

When a V*m* input or output stands at its internal 1 state, all inputs and outputs affected by V*m* stand at their internal 1 states. When the V*m* input or output stands at its internal 0 state, all inputs and outputs affected by V*m* stand at their normally defined internal logic states.

4.5 N (Negate) (X-OR) Dependency

The symbol denoting negate dependency is the letter N. See Figure 10. Each input or output affected by an N*m* input or output stands in an exclusive-OR relationship with the N*m* input or output.



If a = 0, then c = b
If a = 1, then c = $\overline{b}$

FIGURE 10 – N (NEGATE) (X-OR) DEPENDENCY

When an N*m* input or output stands at its internal 1 state, the internal logic state of each input and each output affected by N*m* is the complement of what it would otherwise be. When an N*m* input or output stands at its internal 0 state, all inputs and outputs affected by N*m* stand at their normally defined internal logic states.

4.6 Z (Interconnection) Dependency

The symbol denoting interconnection dependency is the letter Z.

Interconnection dependency is used to indicate the existence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

The internal logic state of an input or output affected by a Z*m* input or output will be the same as the internal logic state of the Z*m* input or output, unless modified by additional dependency notation. See Figure 11.

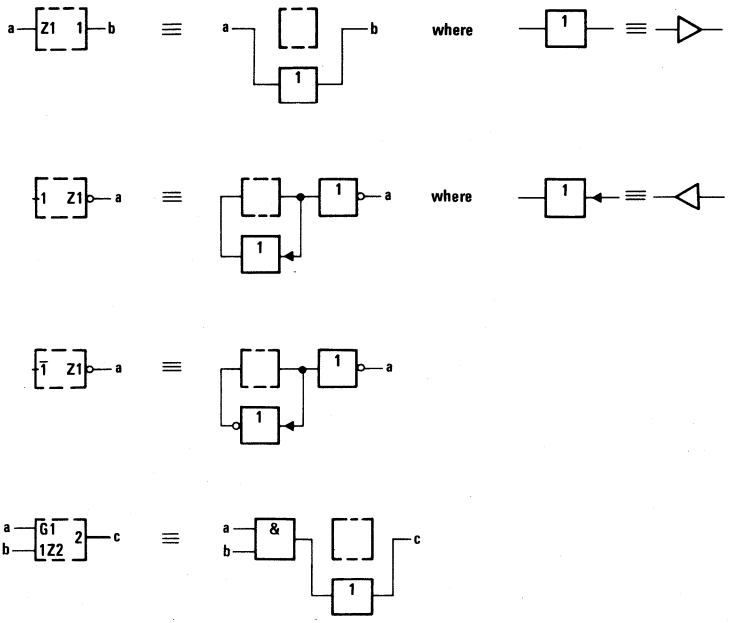


FIGURE 11 – Z (INTERCONNECTION) DEPENDENCY

4.7 C (Control) Dependency

The symbol denoting control dependency is the letter C.

Control inputs are usually used to enable or disable the data (D, J, K, R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically. In the latter case the dynamic input symbol is used as shown in the third example of Figure 12.

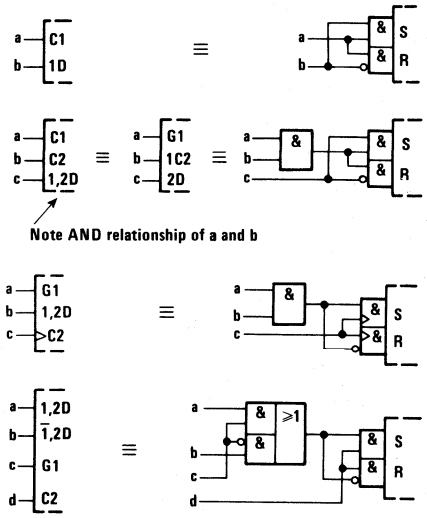


FIGURE 12 – C (CONTROL) DEPENDENCY

When a C*m* input or output stands at its internal 1 state, the inputs affected by C*m* have their normally defined effect on the function of the element, i.e., these inputs are enabled. When a C*m* input or output stands at its internal 0 state, the inputs affected by C*m* are disabled and have no effect on the function of the element.

4.8 S (Set) and R (Reset) Dependencies

The symbol denoting set dependency is the letter S. The symbol denoting reset dependency is the letter R.

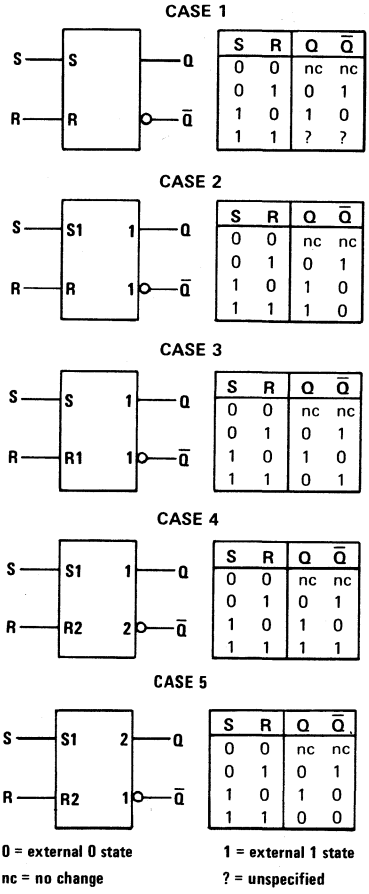
Set and reset dependenies are used if it is necessary to specify the effect of the combination R=S=1 on a bistable element. Case 1 in Figure 13 does not use S or R dependency.

When an S*m* input is at its internal 1 state, outputs affected by the Sm input will react, regardless of the state of an R input, as they normally would react to the combination S=1, R=0. See cases 2, 4, and 5 in Figure 13.

When an R*m* input is at its internal 1 state, outputs affected by the Rm input will react, regardless of the state of an S input, as they normally would react to the combination S=0, R=1. See cases 3, 4, and 5 in Figure 13.

When an S*m* or R*m* input is at its internal 0 state, it has no effect.

Note that the noncomplementary output patterns in cases 4 and 5 are only pseudo stable. The simultaneous return of the inputs to S=R=0 produces an unforeseeable stable and complementary output pattern.



S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	?	?

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	Q̄
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

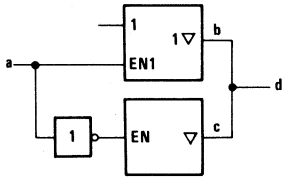
FIGURE 13 – S (SET AND R (RESET) DEPENDENCIES

4.9 EN (Enable) Dependency

The symbol denoting enable dependency is the combination of letters EN.

An EN*m* input has the same effect on outputs as an EN input, see 3.1, but it effects only those outputs labeled with the identifying number *m*. It also affects those inputs labeled with the identifying number *m*. By contrast, an EN input affects all outputs and no inputs. The effect of an EN*m* input on an affected input is identical to that of a C*m* input. See Figure 14.

When an EN*m* input stands at its internal 1 state, the inputs affected by EN*m* have their normally defined effect on the function of the element and the outputs affected by this input stand at their normally defined internal logic states, i.e., these inputs and outputs are enabled.



If a = 0, b is disabled and d = c
If a = 1, c is disabled and d = b

FIGURE 14 – EN (ENABLE) DEPENDENCY

When an EN*m* input stands at its internal 0 state, the inputs affected by EN*m* are disabled and have no effect on the function of the element, and the outputs affected by EN*m* are also disabled. Open-collector outputs are turned off, three-state outputs stand at their normally defined internal logic states but externally exhibit high impedance, and all other outputs (e.g., totem-pole outputs) stand at their internal 0 states.

4.10 M (Mode) Dependency

The symbol denoting mode dependency is the letter M.

Mode dependency is used to indicate that the effects of particular inputs and outputs of an element depend on the mode in which the element is operating.

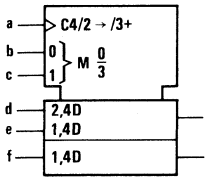
If an input or output has the same effect in different modes of operation, the identifying numbers of the relevant affecting M*m* inputs will appear in the label of that affected input or output between parentheses and separated by solidi. See Figure 19.

4.10.1 M Dependency Affecting Inputs

M dependency affects inputs the same as C dependency. When an M*m* input or M*m* output stands at its internal 1 state, the inputs affected by this M*m* input or M*m* output have their normally defined effect on the function of the element, i.e., the inputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, the inputs affected by this M*m* input or M*m* output have no effect on the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2→/3+), any set in which the identifying number of the M*m* input or M*m* output appears has no effect and is to be ignored. This represents disabling of some of the functions of a multifunction input.

The circuit in Figure 15 has two inputs, **b** and **c**, that control which one of four modes (0, 1, 2, or 3) will exist at any time. Inputs **d**, **e**, and **f** are D inputs subject to dynamic control (clocking) by the **a** input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs **e** and **f** are only enabled in mode 1 (for parallel loading) and input **d** is only enabled in mode 2 (for serial loading). Note that input **a** has three functions. It is the clock for entering data. In mode 2, it causes right shifting of data, which means a shift away from the control block. In mode 3, it causes the contents of the register to be incremented by one count.



Note that all operations are synchronous.

In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place thru inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading thru input d take place.

In MODE 3 (b = c = 1), counting up by increment of 1 per clock pulse takes place.

FIGURE 15 – M (MODE) DEPENDENCY AFFECTING INPUTS

4.10.2 M Dependency Affecting Outputs

When an M*m* input or M*m* output stands at its internal 1 state, the affected outputs stand at their normally defined internal logic states, i.e., the outputs are enabled.

When an M*m* input or M*m* output stands at its internal 0 state, at each affected output any set of labels containing the identifying number of that M*m* input or M*m* output has no effect and is to be ignored. When an output has several different sets of labels separated by solidi (e.g., 2,4/3,5), only those sets in which the identifying number of this M*m* input or M*m* output appears are to be ignored.

In Figure 16, mode 1 exists when the **a** input stands at its internal 1 state. The delayed output symbol is effective only in mode 1 (when input **a** = 1) in which case the device functions as a pulse-triggered flip-flop. See Section 5. When input **a** = 0, the device is not in mode 1 so the delayed output symbol has no effect and the device functions as a transparent latch.

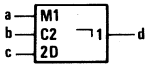


FIGURE 16 – TYPE OF FLIP-FLOP DETERMINED BY MODE

In Figure 17, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 9. Since output **b** is located in the common-control block with no defined function outside of mode 1, this output will stand at its internal 0 state when input **a** stands at its internal 0 state, regardless of the register content.

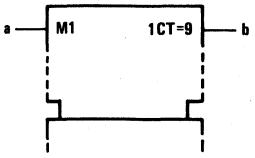


FIGURE 17 – DISABLING AN OUTPUT OF THE COMMON-CONTROL BLOCK

In Figure 18, if input **a** stands at its internal 1 state establishing mode 1, output **b** will stand at its internal 1 state only when the content of the register equals 15. If input **a** stands at its internal 0 state, output **b** will stand at its internal 1 state only when the content of the register equals 0.

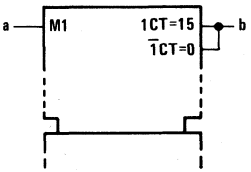


FIGURE 18 – DETERMINING AN OUTPUT'S FUNCTION

In Figure 19 inputs **a** and **b** are binary weighted to generate the numbers 0, 1, 2, or 3. This determines which one of the four modes exists.

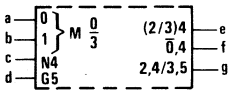


FIGURE 19 – DEPENDENT RELATIONSHIPS AFFECTED BY MODE

At output **e** the label set causing negation (if **c** = 1) is effective only in modes 2 and 3. In modes 0 and 1 this output stands at its normally defined state as if it had no labels. At output **f** the label set has effect when the mode is not 0 so output **e** is negated (if **c** = 1) in modes 1, 2, and 3. In mode 0 the label set has no effect so the output stands at its normally defined state. In this example 0,4 is equivalent to (1/2/3)4. At output **g** there are two label sets. The first set, causing negation (if **c** = 1), is effective only in mode 2. The second set, subjecting **g** to AND dependency on **d**, has effect only in mode 3.

Note that in mode 0 none of the dependency relationships has any effect on the outputs, so **e**, **f**, and **g** will all stand at the same state.

4.11 A (Address) Dependency

The symbol denoting address dependency is the letter A.

Address dependency provides a clear representation of those elements, particularly memories, that use address control inputs to select specified sections of a multidimensional array. Such a section of a memory array is usually called a word. The purpose of address dependency is to allow a symbolic presentation of the entire array. An input of the array shown at a particular element of this general section is common to the corresponding elements of all selected sections of the array. An output of the array shown at a particular element of this general section is the result of the OR function of the outputs of the corresponding elements of selected sections. If the label of an output of the array shown at a particular element of this general section indicates that this output is an open-circuit output or a three-state output, then this indication refers to the output of the array and not to those of the sections of the array.

Inputs that are not affected by any affecting address input have their normally defined effect on all sections of the array, whereas inputs affected by an address input have their normally defined effect only on the section selected by that address input.

An affecting address input is labelled with the letter A followed by an identifying number that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an A*m* input are labelled with the letter A, which stands for the identifying numbers, i.e., the addresses, of the particular sections.

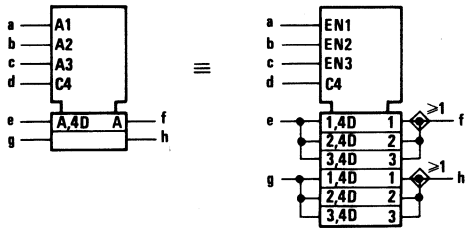


FIGURE 20 – A (ADDRESS) DEPENDENCY

Figure 20 shows a 3-word by 2-bit memory having a separate address line for each word and uses EN dependency to explain the operation. To select word 1, input a is taken to its 1 state, which establishes mode 1. Data can now be clocked into the inputs marked "1,4D". Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked "2,4D" and "3,4D". The outputs will be the OR functions of the selected outputs, i.e., only those enabled by the active EN functions.

The identifying numbers of affecting address inputs correspond with the addresses of the sections selected by these inputs. They need not necessarily differ from those of other affecting dependency-inputs (e.g., G, V, N, . . .), because in the general section presented by the symbol they are replaced by the letter A.

If there are several sets of affecting *Am* inputs for the purpose of independent and possibly simultaneous access to sections of the array, then the letter A is modified to 1A, 2A, . . . Because they have access to the same sections of the array, these sets of A inputs may have the same identifying numbers.

Figure 21 is another illustration of the concept.

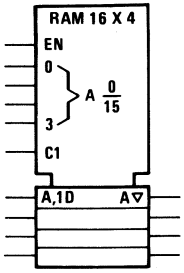


FIGURE 21

FIGURE 21 – ARRAY OF 16 SECTIONS OF FOUR TRANSPARENT LATCHES WITH 3-STATE OUTPUTS COMPRISING A 16-WORD X 4-BIT RANDOM-ACCESS MEMORY

TABLE IV – SUMMARY OF DEPENDENCY NOTATION

TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs. ◇outputs off. ▽outputs at external high impedance, no change in internal logic state. Other outputs at internal 0 state.
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (X-OR)	N	Complements state	No effect
RESET	R	Affected output reacts as it would to S = 0, R = 1	No effect
SET	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Interconnection	Z	Imposes 1 state	Imposes 0 state

*These letter symbols appear at the AFFECTING input (or output) and are followed by a number. Each input (or output) AFFECTED by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described under "Symbols Inside The Outline", see 3.1.

5 BISTABLE ELEMENTS

The dynamic input symbol, the postponed output symbol, and dependency notation provide the tools to differentiate four main types of bistable elements and make synchronous and asynchronous inputs easily recognizable. See Figure 22. The first column shows the essential distinguishing features; the other columns show examples.

Transparent latches have a level-operated control input. The D input is active as long as the C input is at its internal 1 state. The outputs respond immediately. Edge-triggered elements accept data from D, J, K, R, or S inputs on the active transition of C. Pulse-triggered elements require the setup of data before the start of the control pulse; the C input is considered static since the data must be maintained as long as C is at its 1 state. The output is postponed until C returns to its 0 state. The data-lock-out element is similar to the pulse-triggered version except that the C input is considered dynamic in that shortly after C goes through its active transition, the data inputs are disabled and data does not have to be held. However, the output is still postponed until the C input returns to its initial external level.

Notice that synchronous inputs can be readily recognized by their dependency labels (1D, 1J, 1K, 1S, 1R) compared to the asynchronous inputs (S, R), which are not dependent on the C inputs.

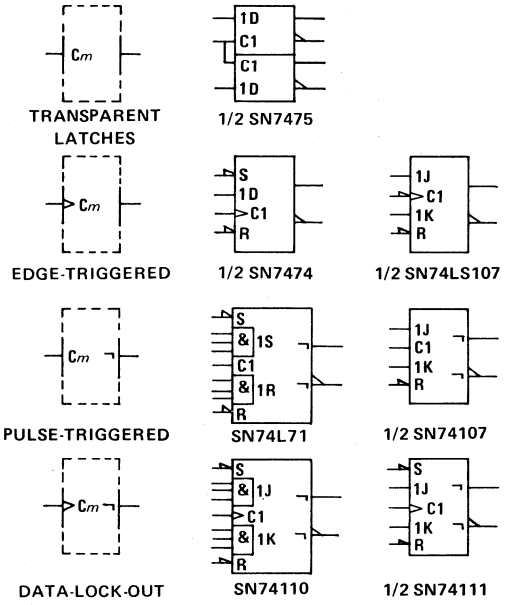


FIGURE 22 – FOUR TYPES OF BISTABLE CIRCUITS

6 CODERS

The general symbol for a coder or code converter is shown in Figure 23. X and Y may be replaced by appropriate indications of the code used to represent the information at the inputs and at the outputs, respectively.

FIGURE 23 – CODER GENERAL SYMBOL

Indication of code conversion is based on the following rule:

> Depending on the input code, the internal logic states of the inputs determine an internal value. This value is reproduced by the internal logic states of the outputs, depending on the output code.

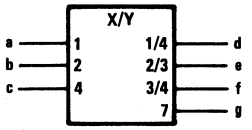
The indication of the relationships between the internal logic states of the inputs and the internal value is accomplished by:

1) labelling the inputs with numbers. In this case the internal value equals the sum of the weights associated with those inputs that stand at their internal 1-state, or by
2) replacing X by an appropriate indication of the input code and labelling the inputs with characters that refer to this code.

The relationships between the internal value and the internal logic states of the outputs are indicated by:

1) labelling each output with a list of numbers representing those internal values that lead to the internal 1-state of that output. These numbers shall be separated by solidi as in Figure 24. This labelling may also be applied when Y is replaced by a letter denoting a type of dependency (see Section 7). If a continuous range of internal values produces the internal 1 state of an output, this can be indicated by two numbers that are inclusively the beginning and the end of the range, with these two numbers separated by three dots, e.g., 4 . . . 9 = 4/5/6/7/8/9, or by
2) replacing Y by an appropriate indication of the output code and labelling the outputs with characters that refer to this code as in Figure 25.

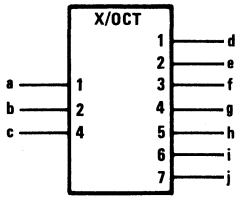
Alternatively, the general symbol may be used together with an appropriate reference to a table in which the relationship between the inputs and outputs is indicated. This is a recommended way to symbolize a PROM after it has been programmed.



TRUTH TABLE

INPUTS			OUTPUTS			
c	b	a	g	f	e	d
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0

FIGURE 24 – AN X/Y CODE CONVERTER



TRUTH TABLE

INPUTS			OUTPUTS						
c	b	a	j	i	h	g	f	e	d
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	0
0	1	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0	0
1	1	0	0	1	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0

FIGURE 25 – AN X/OCTAL CODE CONVERTER

7 USE OF A CODER TO PRODUCE AFFECTING INPUTS

It often occurs that a set of affecting inputs for dependency notation is produced by decoding the signals on certain inputs to an element. In such a case use can be made of the symbol for a coder as an embedded symbol. See Figure 26.

If all affecting inputs produced by a coder are of the same type and their identifying numbers correspond with the numbers shown at the outputs of the coder, Y (in the qualifying symbol X/Y) may be replaced by the letter denoting the type of dependency. The indications of the affecting inputs should then be omitted. See Figure 27.

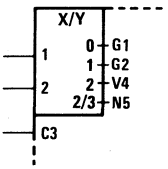


FIGURE 26 – PRODUCING VARIOUS TYPES OF DEPENDENCIES

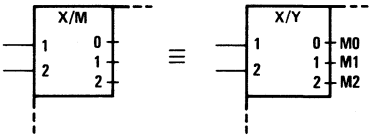


FIGURE 27 – PRODUCING ONE TYPE OF DEPENDENCY

8 USE OF BINARY GROUPING TO PRODUCE AFFECTING INPUTS

If all affecting inputs produced by a coder are of the same type and have consecutive identifying numbers not necessarily corresponding with the numbers that would have been shown at the outputs of the coder, use can be made of the binary grouping symbol (see 3.1). k external lines effectively generate 2^k internal inputs. The bracket is followed by the letter denoting the type of dependency followed by $\frac{m1}{m2}$. The m1 is to be replaced by the smallest identifying number and the m2 by the largest one, as shown in Figure 28.

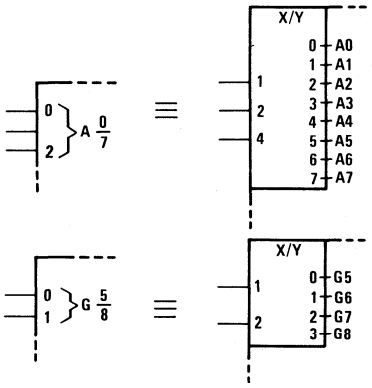


FIGURE 28 – USE OF THE BINARY GROUPING SYMBOL

9 SEQUENCE OF INPUT LABELS

If an input having a single functional effect is affected by other inputs, the qualifying symbol (if there is any) for that functional effect is preceded by the labels corresponding to the affecting inputs. The left-to-right order of these preceding labels is the order in which the effects or modifications must be applied. The affected input has no functional effect on the element if the logic state of any one of the affecting inputs, considered separately, would cause the affected input to have no effect, regardless of the logic states of other affecting inputs.

If an input has several different functional effects or has several different sets of affecting inputs, depending on the mode of action, the input may be shown as often as required. However, there are cases in which this method of presentation is not advantageous. In those cases the input may be shown once with the different sets of labels separated by solidi. See Figure 29. No meaning is attached to the order of these sets of labels. If one of the functional effects of an input is that of an unlabelled input of the element, a solidus will precede the first set of labels shown.

If all inputs of a combinational element are disabled (caused to have no effect on the function of the element), the internal logic states of the outputs of the element are not specified by the symbol. If all inputs of a sequential element are disabled, the content of this element is not changed and the outputs remain at their existing internal logic states.

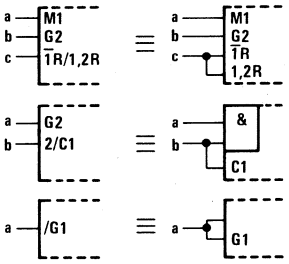


FIGURE 29 – INPUT LABELS

Labels may be factored using algebraic techniques.

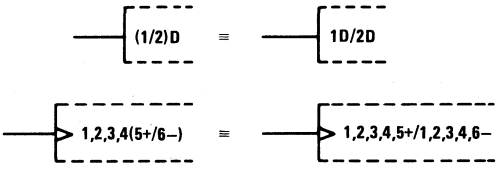


FIGURE 30 – FACTORING INPUT LABELS

10 SEQUENCE OF OUTPUT LABELS

If an output has a number of different labels, regardless of whether they are identifying number of affecting inputs or outputs or not, these labels are shown in the following order:

1) if the postponed output symbol has to be shown, this comes first, if necessary preceded by the indications of the inputs to which it must be applied;

2) followed by the labels indicating modifications of the internal logic state of the output, such that the left-to-right order of these labels corresponds with the order in which their effects must be applied;

3) followed by the label indicating the effect of the output on inputs and other outputs of the element.

Symbols for open-circuit or three-state outputs, where applicable, are placed just inside the outside boundary of the symbol adjacent to the output line. See Figure 31.

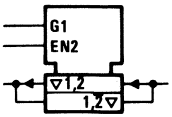


FIGURE 31 – PLACEMENT OF 3-STATE SYMBOLS

If an output needs several different sets of labels that represent alternative functions (e.g., depending on the mode of action), these sets may be shown on different output lines that must be connected outside the outline. However, there are cases in which this method of presentation is not advantageous. In those cases the output may be shown once with the different sets of labels separated by solidi. See Figure 32.

Two adjacent identifying numbers of affecting inputs in a set of labels that are not already separated by a nonnumeric character should be separated by a comma.

If a set of labels of an output not containing a solidus contains the identifying number of an affecting M*m* input standing at its internal 0 state, this set of labels has no effect on that output.

Labels may be factored using algebraic techniques.

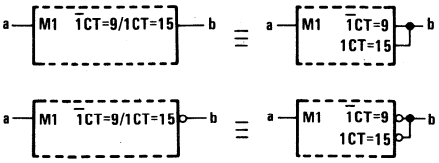


FIGURE 32 – OUTPUT LABELS

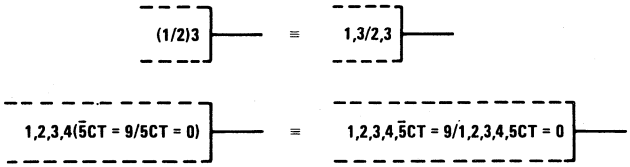


FIGURE 33 – FACTORING OUTPUT LABELS

If you have questions on this Explanation of New Logic Symbols, please contact:

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Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 995-3746

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Ordering Instructions and Mechanical Data

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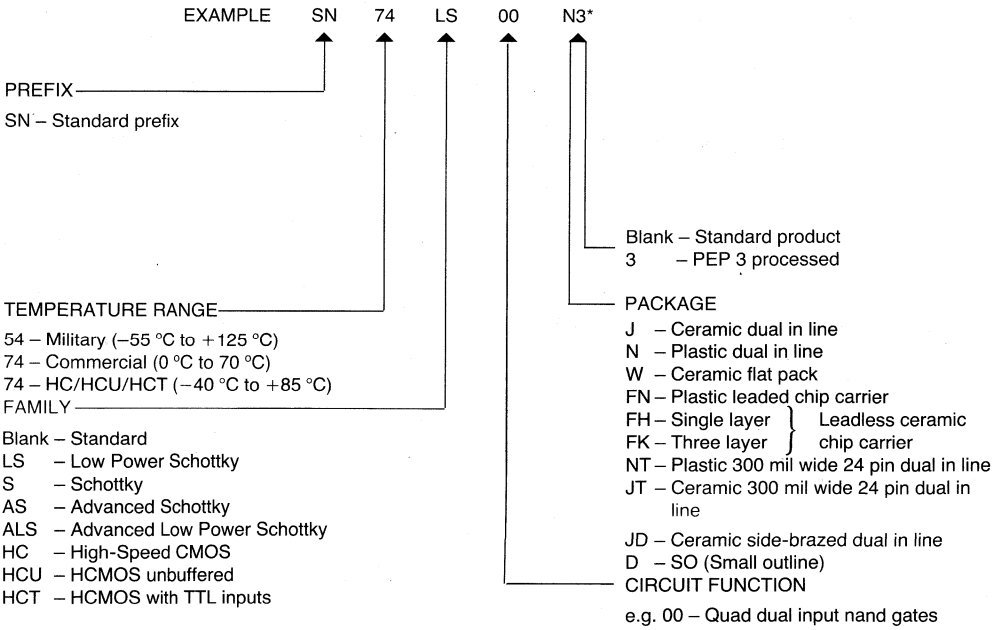
Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference with the pin connection diagram(s). These alphabetic references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this catalogue should include a type number as explained below.



* Only applies to N packaged product.

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Barnes Carrier

SOJC (D)
Slide Magazines
(Tubes)

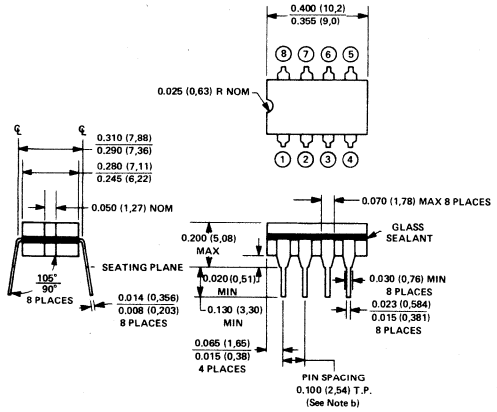
DUAL IN LINE (J,JD, N, NT, JT)
Slide Magazines
A channel Plastic Tubing
Sectional Cardboard Box
Individual Plastic Box

CHIP CARRIER (FK,FH, FN)
Slide Magazines
Sectional Cardboard Box
Individual Cardboard Box

J ceramic dual-in-line package

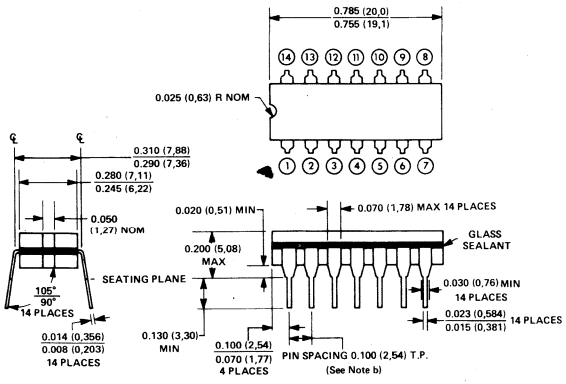
These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, 20-, or 24-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

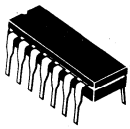
8-PIN JG CERAMIC



NOTES: a. All dimensions are inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

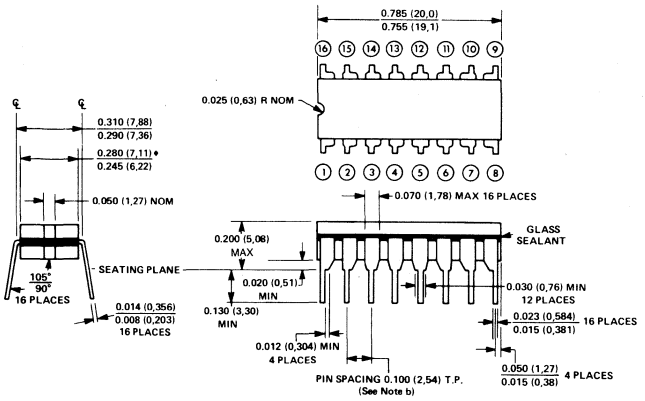
14-PIN J CERAMIC

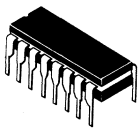




Falls within JEDEC TO-116 and MO-001AA dimensions

16-PIN J CERAMIC

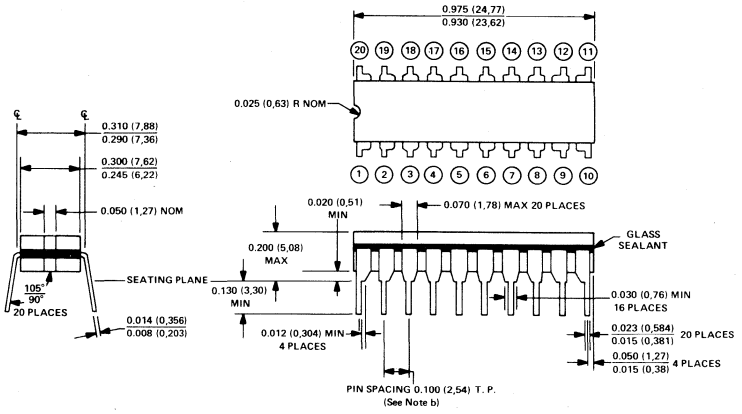


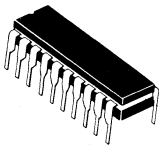


♦For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 0.300 (7,62). All other dimensions apply without modification.

J ceramic dual-in-line packages (continued)

20-PIN J CERAMIC

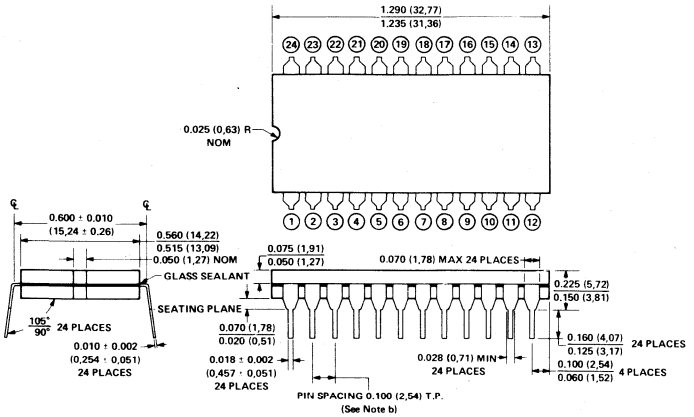


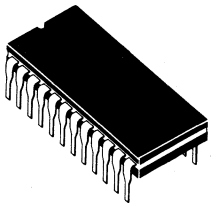


J and JT ceramic dual-in-line package

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 24- or 28-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

24-PIN J CERAMIC

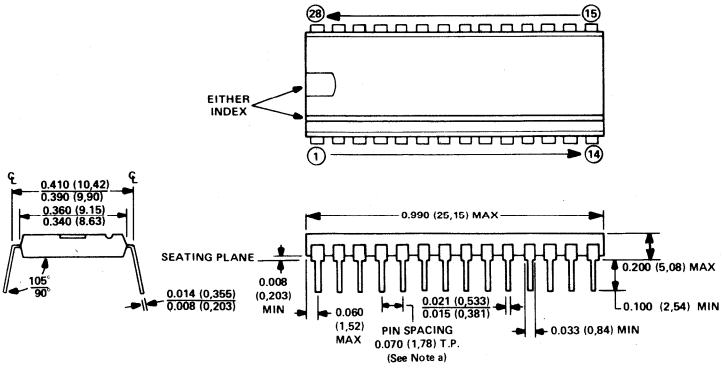




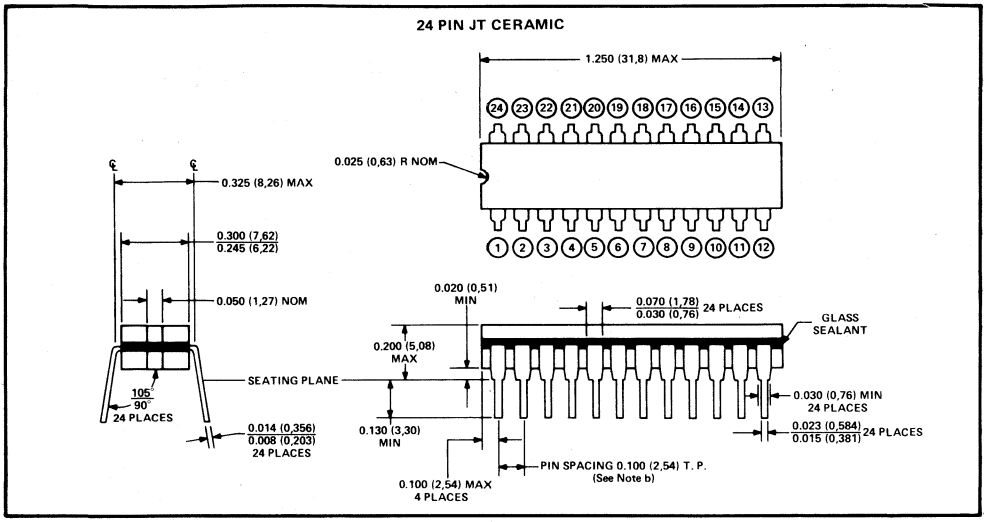
Falls within JEDEC MO-015AA dimensions

NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

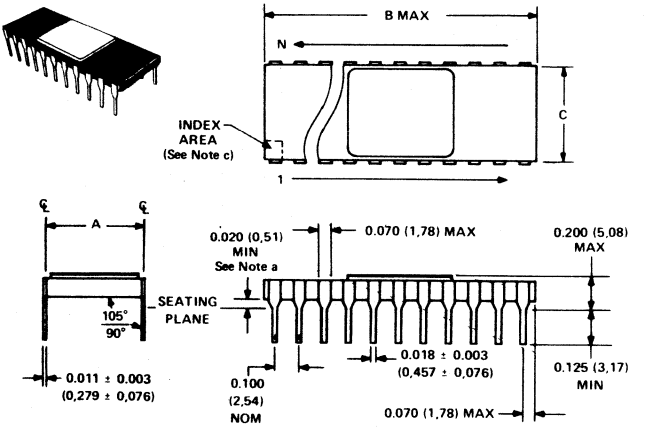
28 PIN J CERAMIC



TTL INTEGRATED CIRCUITS MECHANICAL DATA



40 pin JD ceramic dual in line package
ceramic packages with side-brazed leads and metal or epoxy or glass lid seal



NOTES: a. This minimum spacing is valid for printed circuit board mounting with 0.033 (0,84) diameter holes for the leads.
b. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
c. The index is placed in this area to identify pin 1 and to provide other information as follows:

1	Pin 1 connected to chip-mounting pad.
ΔXX	Pin XX connected to chip-mounting pad.
●	No connetion to chip-mounting pad.

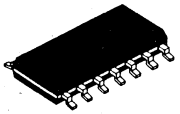
Other symbols may indicate any combination of up-to 4 pins connected to the chip-mounting pad.

DIM \ PINS	16	18	20	22	24	28	40
A ± 0.010 (0,26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (15,24)
B MAX	0.840 (21,4)	0.910 (23,1)	1.020 (25,9)	1.100 (28,0)	1.290 (32,8)	1.415 (36,0)	2.020 (51,3)
C NOM	0.290 (7,4)	0.290 (7,4)	0.290 (7,4)	0.390 (9,9)	0.590 (15,0)	0.590 (15,0)	0.590 (15,0)

D plastic dual-in-line packages (SO package)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

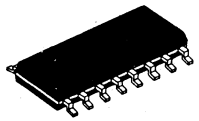
14-PIN
D PACKAGE



NOTES:
1. Body dimensions do not include mold flash.
2. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

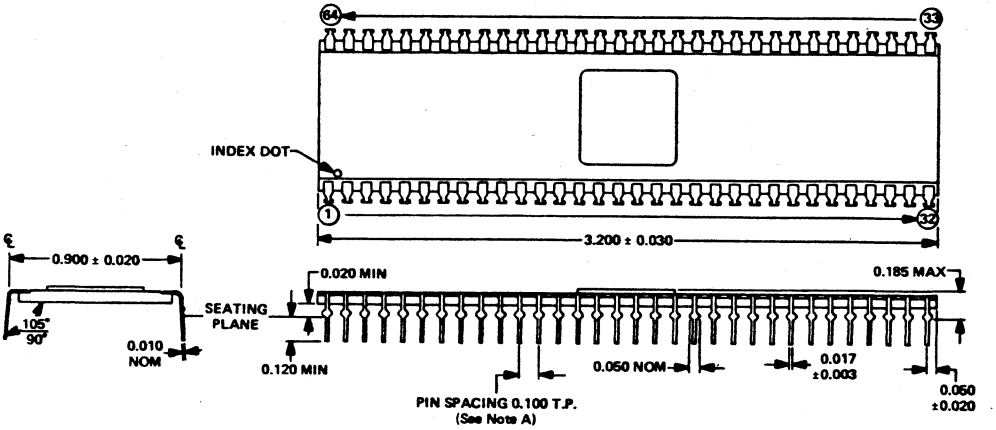
16-PIN
D PACKAGE



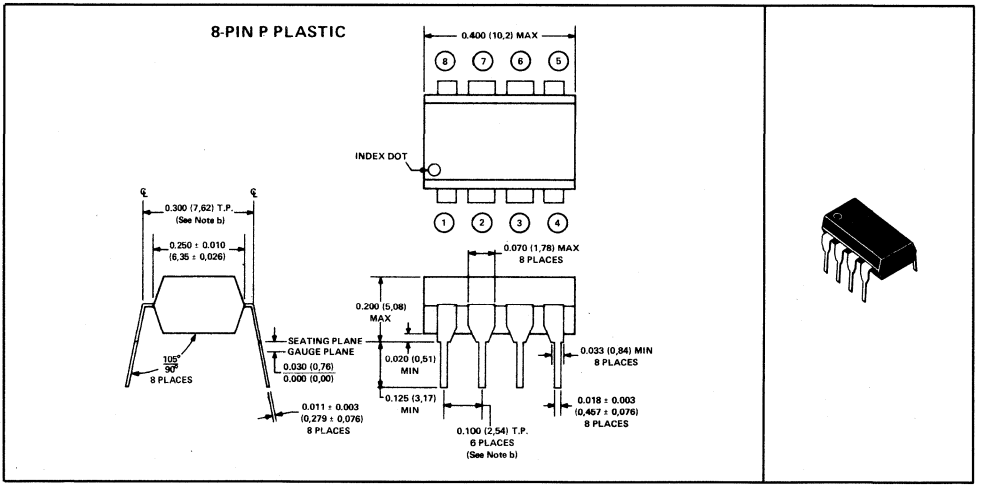
NOTES:
1. Body dimensions do not include mold flash.
2. Leads are within 0,25 (0.010) radius of true position at maximum material condition.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

64 pin ceramic dual in line package



NOTE A. Each pin centerline is located within 0.010 of its true longitudinal position.

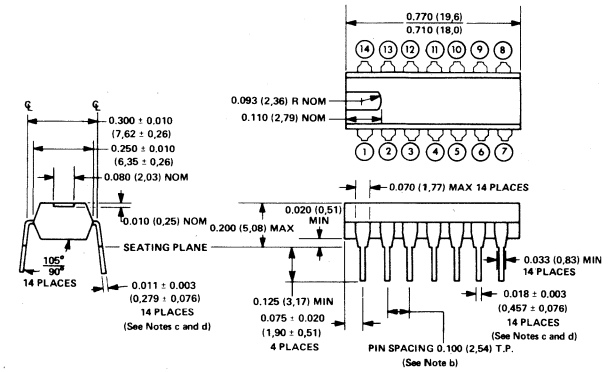


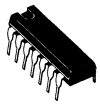
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin is within 0.005 (0,127) radius of true position (TP) at the gauge plane with maximum material condition and unit installed.

N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 28-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

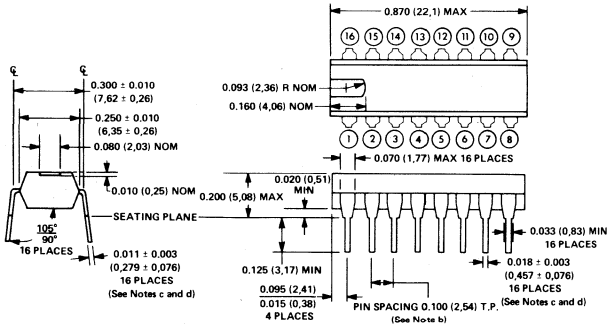
14-PIN N PLASTIC

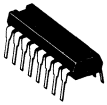




Falls Within JEDEC TO-116 and MO-001AA Dimensions

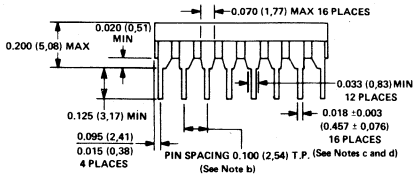
16-PIN N PLASTIC





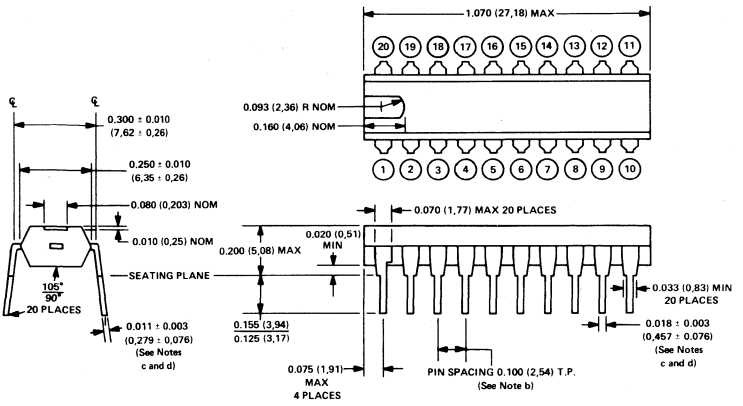
Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.

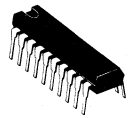
ALTERNATE SIDE VIEW



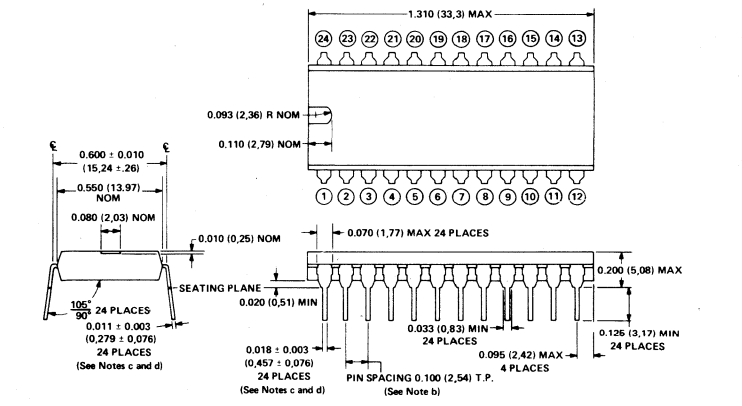
N plastic dual-in-line packages (continued)

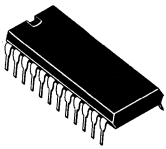
20-PIN N PLASTIC





24-PIN N PLASTIC

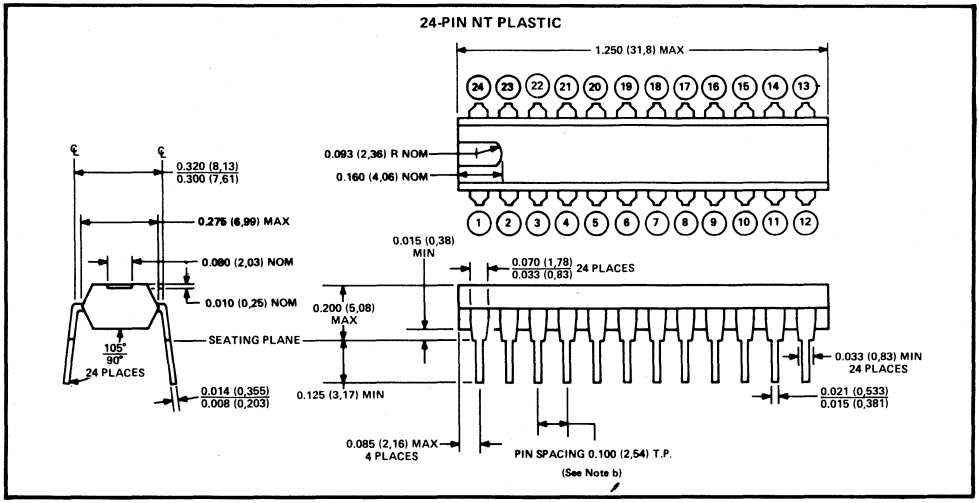




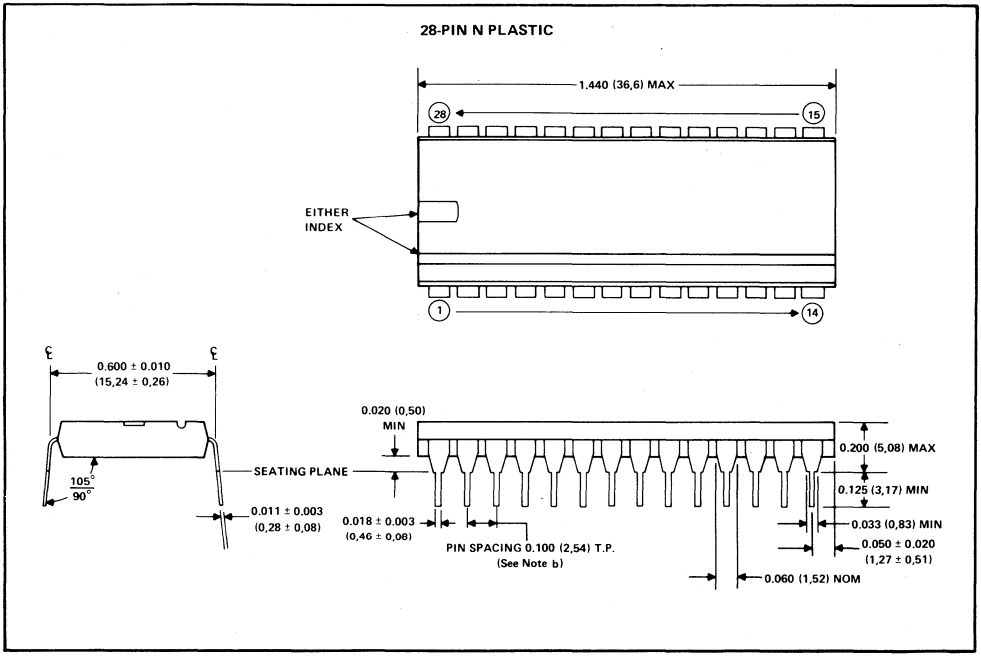
NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,50) above the seating plane.

NT plastic dual-in-line packages

This dual-in-line package consists of a circuit mounted on a 24-lead frame and encapsulated within an electrically non-conductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting hole rows on 0.300 (7,62) or 0.600 (15,24) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.



N plastic dual-in-line packages (continued)

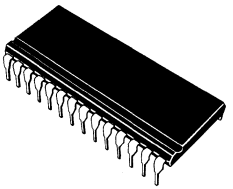


NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

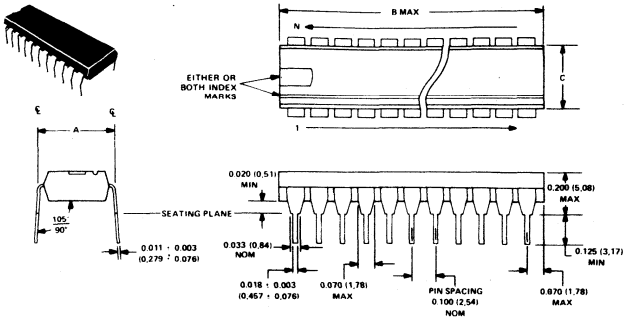
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 (0,50) above the seating plane.



40 pin N plastic dual in line package
plastic packages



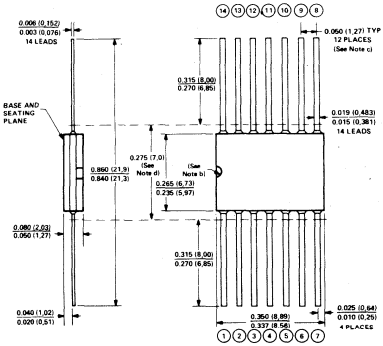
All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

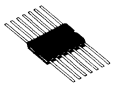
DIM \ PINS	8	16	18	20	22	24	28	40
A ± 0.010 (0,26)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.400 (10,16)	0.600 (15,24)	0.600 (15,24)	0.600 (10,24)
B MAX	0.390 (9,9)	0.870 (22,1)	0.920 (23,4)	1.070 (27,2)	1.100 (28,0)	1.290 (32,8)	1.440 (36,6)	2.090 (53,1)
C NOM	0.250 (6,4)	0.250 (6,4)	0.250 (6,4)	0.265 (6,7)	0.350 (8,9)	0.550 (14,0)	0.550 (14,0)	0.550 (14,0)

W ceramic flat package

These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

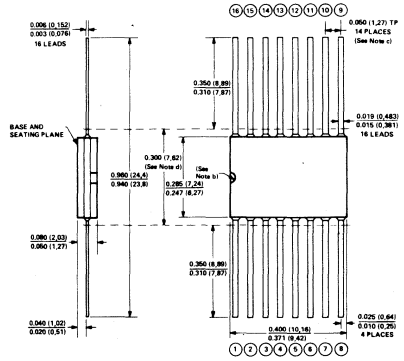
14 PIN W CERAMIC

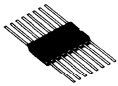




Falls within JEDEC MO-004AA Dimensions

16 PIN W CERAMIC

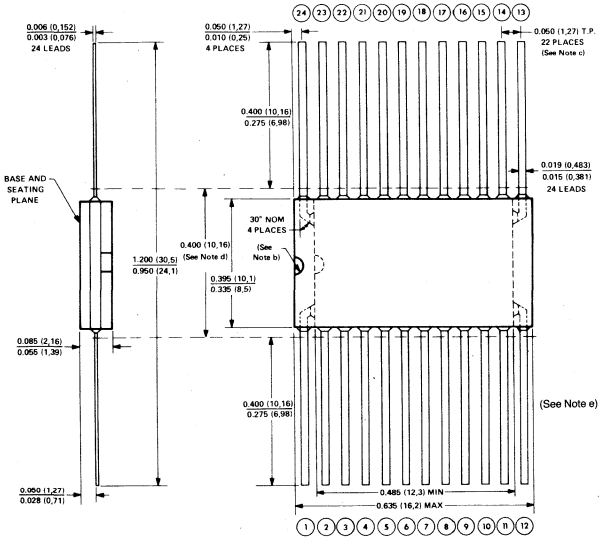




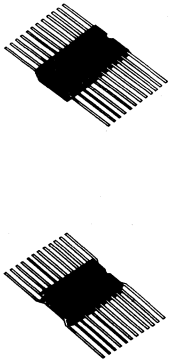
Falls within JEDEC MO-004AG Dimensions

W ceramic flat package (continued)

24 PIN W CERAMIC



Falls within JEDEC MO-019AA Dimensions



NOTES: a. All dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 (0,13) radius of true position (T.P.) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. End configuration of 24-pin package is at the option of TI.

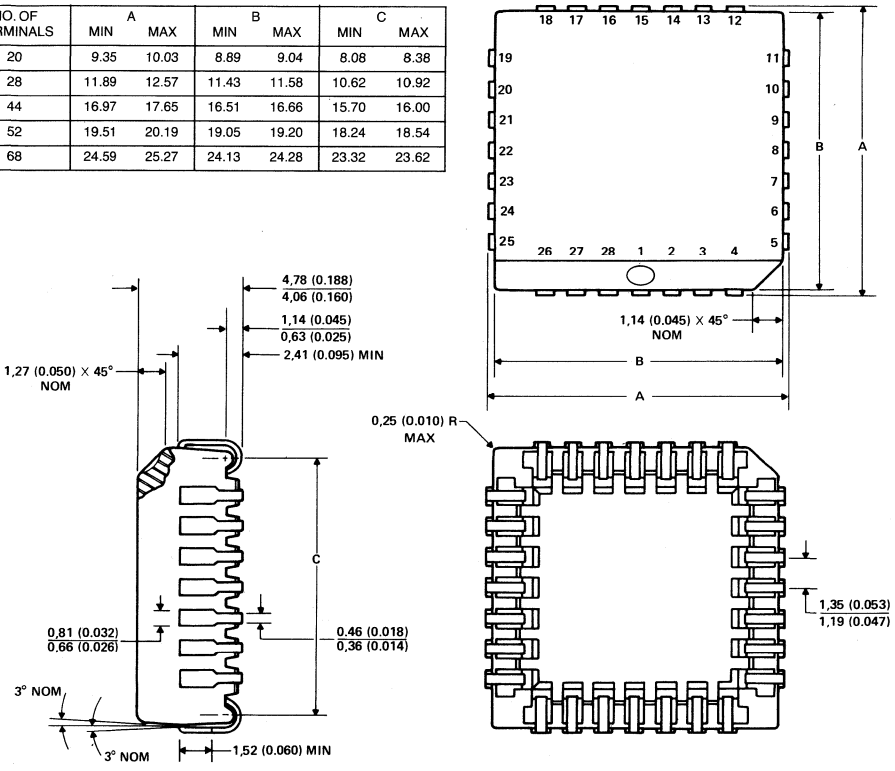
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 0.050-inch centers. Leads require no additional cleaning or processing when used in soldered assembly.

The following bipolar digital device families will be offered in these plastic chip carrier packages: Advanced Schottky and Advanced Low-Power Schottky, all bipolar PROMS, Schottky and Low-Power Schottky.

FN PLASTIC CHIP CARRIER PACKAGE
(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9.35	10.03	8.89	9.04	8.08	8.38
28	11.89	12.57	11.43	11.58	10.62	10.92
44	16.97	17.65	16.51	16.66	15.70	16.00
52	19.51	20.19	19.05	19.20	18.24	18.54
68	24.59	25.27	24.13	24.28	23.32	23.62



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

FH and FK ceramic chip carrier packages

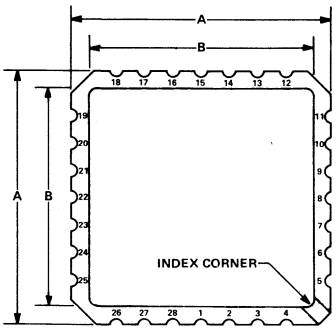
Both versions of these hermetically sealed chip carrier packages have ceramic bases. The FH package has a single-layer base with a ceramic lid and glass seal. The FK package has a three-layer base with either a metal lid and braze seal or a ceramic lid and glass seal, at the option of Texas Instruments.

The packages are intended for surface mounting on solder lands on 0.050-inch centers. Terminals require no additional cleaning or processing when used in soldered assembly.

The full-military-temperature-range versions of the following bipolar digital device families, will be offered in these or similar ceramic chip carrier packages: Advanced Low-Power Schottky, PROMs and RAMs, and certain memory support functions (i.e., 'S225, 184A, 185, 284, 285 and 'LS630).

Products in design will be offered in 44-terminal (MS004CD), 52-terminal (MS004CE), 68-terminal (MS004CF), and 84-terminal (MS004CG) packages.

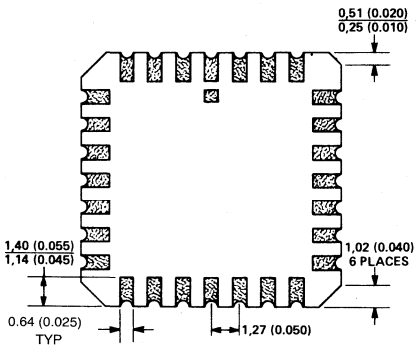
FH AND FK CERAMIC CHIP CARRIER PACKAGE
(28-terminal package shown)

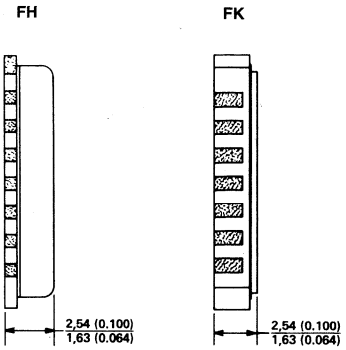


CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NUMBER OF TERMINALS	A		B	
		MIN	MAX	MIN	MAX
MS004CB	20	8,687 (0.342)	9,093 (0.358)	7,798 (0.307)	9,093 (0.358)
MS004CC	28	11,227 (0.442)	11,633 (0.458)	10,312 (0.406)	11,633 (0.458)

*All dimensions and notes for the specified JEDEC outline apply.





All dimensions are in millimeters and parenthetically in inches.

JEDEC Standard for Digital Bipolar Logic Circuit Pin-outs of Chip Carriers

The following information details the JEDEC approved standards for chip carriers that are being supplied by Texas Instruments. This is in accordance with the JEDEC JC-40.1 Committee recommended pin-out connections for Bipolar logic devices.

1. The standard chip carrier packages for Bipolar Digital Logic will be:
   A. Twenty (20) Lead:
      For devices up to 20 external connections, the standard chip carrier package will be the .350 x .350 inch square format with 20 pads on .050 inch centres, as defined in JEDEC Standard MS004, Variation CB*.
   B. Twenty-eight (28 Lead:
      For devices up to 28 external connections, the standard chip carrier package will be the .450 x .450 inch square format with 28 pads on .050 inch centres, as defined in JEDEC Standard MS004, Variation CC*.
   C. Forty-four (44) Lead:
      For devices up to 44 external connections, the standard chip carrier package will be the .650 x .650 inch square format with 44 pads on .050 inch centres, as defined in JEDEC Standard MS004, Variation CD*.
   D. Sixty-eight (68) Lead:
      For devices up to 68 external connections, the standard chip carrier package will be the .950 x .950 inch square format with 68 pads on .050 inch centres, as defined in JEDEC Standard MS004, Variation CF*.
2. The pin-out definitions for Bipolar Digital Logic Integrated Circuits in the Dual-in-Line package configuration is universally accepted and documented in the industry's array of component catalogues. All pin-outs in chip carriers will be by reference to the de facto Dual-in-Line standards as follows:
   A. Twenty (20) Lead:
      1. Devices requiring 14 connections in a 20 pad chip carrier, see Figure 1.
      2. Devices requiring 16 connections in a a 20 pad chip carrier, see Figure 2.
      3. Devices requiring 20 connections in a 20 pad chip carrier, see Figure 3.
   B. Twenty-eight (28) Lead:
      1. Devices requiring f24 connections in a 28 pad chip carrier, see Figure 4.
      2. Devices requiring 28 connections in a 28 pad chip carrier, see Figure 5.
   C. Bias Voltages for chip carriers will be designated by the following standard convention:
      The most positive bias voltage required by the device will be assigned to the highest numbered terminal. The most negative bias voltage required by the device will be assigned to the terminal number which is half the highest terminal number. Other required bias voltages will be assigned terminal numbers in accordance with the appropriate mapping figure.

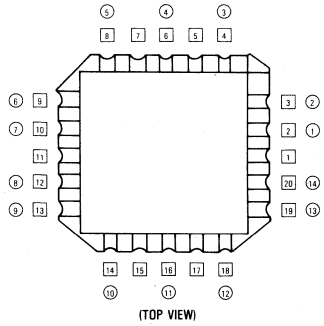


Figure 1: 14-Lead Pin-out for 20 Terminal Chip Carrier

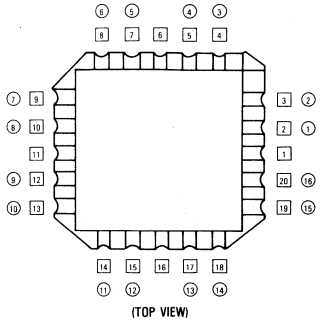


Figure 2: 16-Lead Pin-out for 20 Terminal Chip Carrier

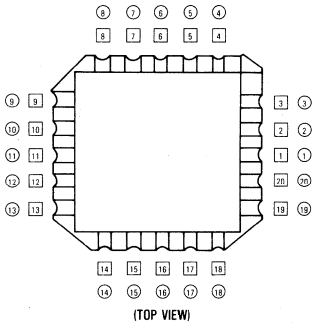


Figure 3: 20-Lead Pin-out for 20 Terminal Chip Carrier

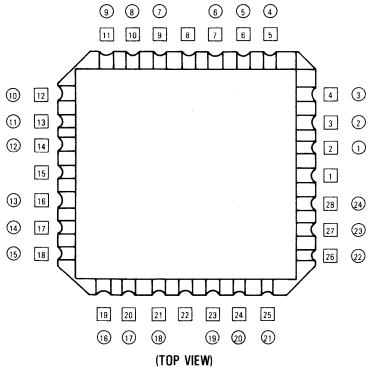


Figure 4: 24-Lead Pin-out for 28 Terminal Chip Carrier

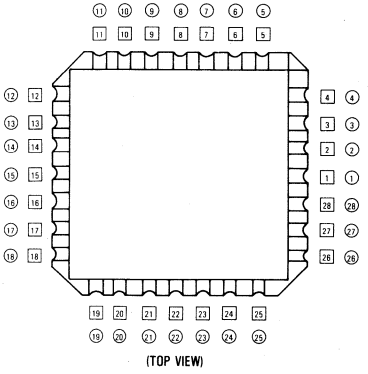


Figure 5: 28-Lead Pin-out for 28 Terminal Chip Carrier

THERMAL RESISTANCE OF INTEGRATED CIRCUIT PACKAGES

Typical thermal resistance values of standard integrated circuit packages are shown in the table below. The values shown do not imply any guarantee, but represent the latest and best available data. Steady-state thermal conditions are implied in the resistance measurements. Also, the following definitions apply:

RΦJC – thermal resistance from junction to case using freon as heat sink. This parameter offers good repeatability and a high degree (±5%) of correlation.

RΦJX – thermal resistance from junction to still air (25 °C ambient) with packagef in a specified socket. This parameter is highly dependent on test conditions which are difficult to reproduce accurately.

BIPOLAR PRODUCTS
TYPICAL THERMAL RESISTANCES

PACKAGE DESCRIPTION	PACKAGE DESIGNATION	°C/WATT		SOCKET USED FOR RΦJX MEASUREMENT	POWER (mW)
		RΦJC ±5%	RΦJX ±15%		
8-Pin Plastic DIP	P	52	95	Augat	300
14- or 16-Pin Plastic DIP	N	45	90	Augat	300
24-Pin Plastic DIP	N	35	65	Barnes	500
14- or 16-Pin Ceramic DIP	J	20	70	Augat	300
14- or 16-Pin Ceramic Flat Pak (Alloy Mounted)	W, U	45	160	Barnes Carrier/ Contactor	500

Special test chips were used to obtain the above information.

54/74 Families of Compatible TTL Circuits

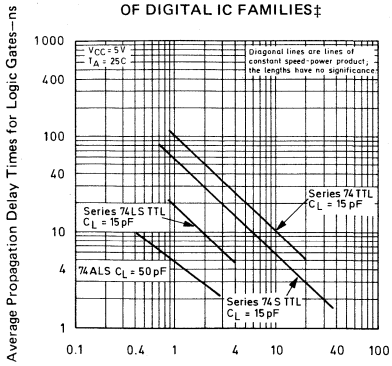
Please note: Details of all Texas Instruments AS and ALS Products are contained in TTL Data Book Vol II.

description

Texas Instruments transistor-transistor-logic (TTL) family of high-performance bipolar digital integrated circuits comprises five distinct series of compatible product lines. These product lines offer the digital systems designer a full spectrum of performance ranges in order to optimize system cost and performance. The available choices range from the very high performance of the Schottky-clamped† functions for systems operating typically up to 200 megahertz to low-power functions with power consumption of only one milliwatt per gate.

Typical characteristics of the five TTL series offered are shown in Table I and their respective speed/power relationships are illustrated in Figure A.

SPEED-POWER RELATIONSHIPS
OF DIGITAL IC FAMILIES‡



‡Typical saturated logic gate from the indicated families.

FIGURE A

TABLE 1 – 54/74 FAMILY TYPICAL SSI PERFORMANCE CHARACTERISTICS

SERIES	GATES			FLIP-FLOPS
	Speed-Power Product	Propagation Delay Time	Power Dissipation	Clock Input Frequency Range
54LS/74LS	19 pJ	9.5 ns	2 mW	dc to 45 MHz
54S/74S	57 pJ	3 ns	19 mW	dc to 125 MHz
54/74	57 pJ	10 ns	10 mW	dc to 35 MHz
54AS/74AS	30 pJ	1.5 ns	20 mW	dc to 200 MHz
54ALS/74ALS	4 pJ	4 ns	1 mW	dc to 50 MHz
54ALS/74ALS (buffer output)	6 pJ	3 ns	2 mW	dc to 50 MHz

features

EASE OF SYSTEM DESIGN

- **Full compatibility provides choice from five distinct performance ranges**
- **Broad range of functions are offered in each series**
- **Diode-clamped inputs are provided on all high-performance functions**
- **Terminated,controlled-impedance lines are not normally required with TTL**
- **Low output impedance:**
  Provides low a-c noise susceptibility
  Drives high-capacity loads

FULL COMPATIBILITY IS DESIGNED INTO TI TTL

- **All series are designed for single 5-volt power supply**
- **All series provide one-volt or greater typical d-c noise margins**
- **Power dissipation relatively insensitive to operating frequency**
- **Switching times are guaranteed at full d-c loading**
- **Compatible with most logic families such as DTL, MOS, CMOS**

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74	SERIES 54ALS / SERIES 74ALS	SERIES 54AS / SERIES 74AS	SERIES 54LS / SERIES 74LS WITH DIODE INPUTS	SERIES 54LS / SERIES 74LS WITH EMITTER INPUTS	SERIES 54S / SERIES 74S	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	7	7	V
Input voltage		5,5	7	7	7	5,5	5,5	V
Interemitter voltage (see Note 2)		5,5				5,5	5,5	V
Off-state (high-level) voltage applied to open-collector outputs of SSI circuits (see Note 3)	'06, '07	30						V
	'16, '17, '26	15						
	Others		7	7	7	7	7	
High-level voltage applied to a disabled 3-state output		5,5	5,5	5,5	5,5	5,5	5,5	V
Operating free-air temperature range	54 Family	−55 to 125						°C
	74 Family	0 to 70						
Storage temperature range		−65 to 150						°C

NOTES: 1. Voltage values, unless otherwise noted, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.
3. Ratings for MSI parts are given on the individual date sheets.

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than V_{OH} min (see tables of electrical characteristics), but not to exceed the absolute maximum rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between V_{OH} min and 4.5 V. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

b. Connect unused inputs to a used input if maximum drive capability of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient that exceeds the input maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

d. Connect unused inputs to any fixed-high-level compatible output such as the output of an inverter or NAND gate that has its input(s) grounded. Maximum high-level drive capability of the output should not be exceeded.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. The table below shows maximum input current requirements and nominal base resistor values for standard loads in each TTL series. A standard load is defined as an input connected to a single emitter or diode that is associated with a pull-up resistor having the value indicated in the table. However, some inputs are tied to more than one input transistor (or diode), or the base-resistor values of some inputs have been changed either to reduce input-current requirements or to improve performance. Therefore, the input-current requirements may vary. Consult the electrical characteristics table for the particular device type to determine the input-current requirements of each input.

STANDARD INPUTS (ONE LOAD)

SERIES	MINIMAL VALUE OF INPUT PULL-UP RESISTOR	MAXIMUM HIGH-LEVEL INPUT CURRENT	MAXIMUM LOW-LEVEL INPUT CURRENT
54/74	4 kΩ	40 μA	− 1.6 mA
54LS/74LS	18 kΩ	20 μA	− 0.4 mA
54S/74S	2.8 kΩ	50 μA	− 2 mA
54ALS/74ALS		20 μA	− 0.2 mA
54AS/74AS		0.2 mA	− 2.4 mA

Since low-level input current is primarily a function of the input base resistor, two or more inputs of the same NAND or AND gate may be tied together and still be considered one load at a low logic level, but at a high logic level, each input is an additional load.

Currents into input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

drive capability

The maximum value of I_{OL} given under "recommended operating conditions" reflects the ability of an output to sink current from a number of loads at a low voltage level and maximum I_{OH} reflects the ability to supply current at a high voltage level. Each standard output at a low level is capable of sinking current from 10 standard loads of its own series (20 standard loads for Series 74LS/74ALS), and at a high level is capable of supplying current to either 10 or 20 loads of its own series. The fan-out of 20 at a high logic level makes it possible to tie as many as 10 unused inputs of NAND or AND gates to used inputs of the same gates (as mentioned under input-current requirements) without exceeding the fan-out capability of the output driving 10 used inputs. Certain outputs are designed for special applications and have greater or lesser drive capability. See the recommended operating conditions for each type.

The loads may be intermixed in any desired combination so long as the load totals for I_{IH} and I_{IL} are less than the maximum recommended values of I_{OH} and I_{OL}, respectively, for the driving circuit.

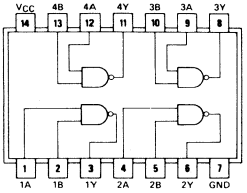
PIN ASSIGNMENTS (TOP VIEWS)

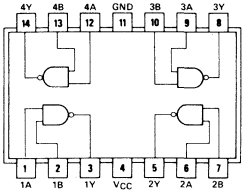
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$

See page 6-2





SN5400 (J)
SN54ALS00A (J)
SN54AS00 (J)
SN54HC00 (J)
SN54LS00 (J, W)
SN54S00 (J, W)

SN7400 (J, N)
SN74ALS00A (N)
SN74AS00 (N)
SN74HC00 (N)
SN74LS00 (J, N)
SN74S00 (J, N)

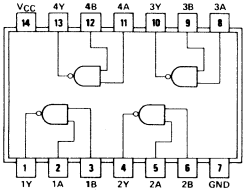
SN5400 (W)

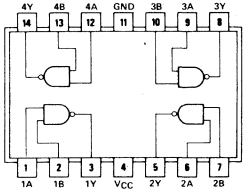
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

01

positive logic:
$Y = \overline{AB}$

See page 6-4





SN5401 (J)
SN54ALS01 (J)
SN54HC01 (J)
SN54LS01 (J, W)

SN7401 (J, N)
SN74ALS01 (N)
SN74HC01 (N)
SN74LS01 (J, N)

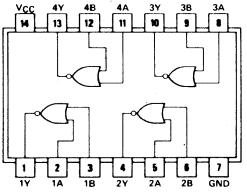
SN5401 (W)

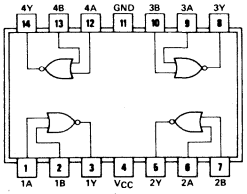
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

02

positive logic:
$Y = \overline{A+B}$

See page 6-8





SN5402 (J)
SN54ALS02 (J)
SN54AS02 (J)
SN54HC02 (J)
SN54LS02 (J, W)
SN54S02 (J, W)

SN7402 (J, N)
SN74ALS02 (N)
SN74AS02 (N)
SN74HC02 (N)
SN74LS02 (J, N)
SN74S02 (J, N)

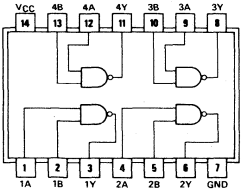
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

03

positive logic:
$Y = \overline{AB}$

See page 6-4



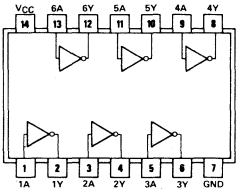
SN5403 (J) SN7403 (J, N)
SN54ALS03A (J) SN74ALS03A (N)
SN54HC03 (J) SN74HC03 (N)
SN54LS03 (J, W) SN74LS03 (J, N)
SN54S03 (J, W) SN74S03 (J, N)

HEX INVERTERS

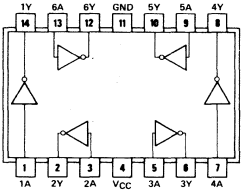
04

positive logic:
$Y = \overline{A}$

See page 6-2



SN5404 (J) SN7404 (J, N)
SN54ALS04 (J) SN74ALS04 (N)
SN54AS04 (J) SN74AS04 (N)
SN54HC04 (J) SN74HC04 (N)
SN54LS04 (J, W) SN74LS04 (J, N)
SN54S04 (J, W) SN74S04 (J, N)



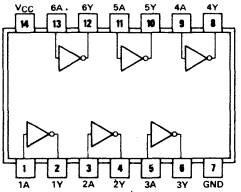
SN5404 (W)

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

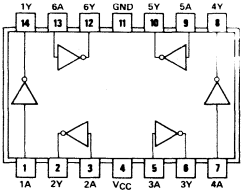
05

positive logic:
$Y = \overline{A}$

See page 6-4



SN5405 (J) SN7405 (J, N)
SN54ALS05 (J) SN74ALS05 (N)
SN54HC05 (J) SN74HC05 (N)
SN54LS05 (J, W) SN74LS05 (J, N)
SN54S05 (J, W) SN74S05 (J, N)



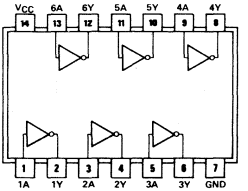
SN5405 (W)

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

06

positive logic:
$Y = \overline{A}$

See page 6-24



SN5406 (J, W) SN7406 (J, N)
SN54LS06 (J, W) SN74LS06 (J, N)

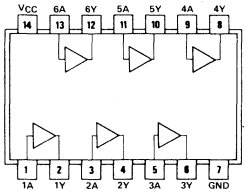
PIN ASSIGNMENTS (TOP VIEWS)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

07

positive logic:
Y = A

See page 6-24



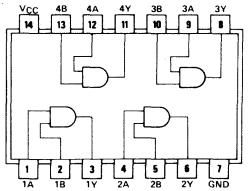
SN5407 (J, W)
SN54LS07 (J, W)
SN7407 (J, N)
SN74LS07 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
Y = AB

See page 6-10



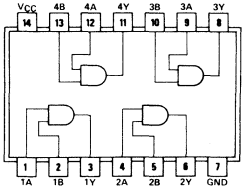
SN5408 (J, W)
SN54ALS08 (J)
SN54AS08 (J)
SN54HC08 (J)
SN54LS08 (J, W)
SN54S08 (J, W)
SN7408 (J, N)
SN74ALS08 (N)
SN74AS08 (N)
SN74HC08 (N)
SN74LS08 (J, N)
SN74S08 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

09

positive logic:
Y = AB

See page 6-12



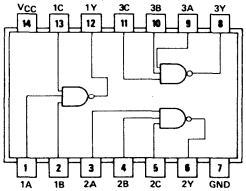
SN5409 (J, W)
SN54ALS09 (J)
SN54HC09 (J)
SN54LS09 (J, W)
SN54S09 (J, W)
SN7409 (J, N)
SN74ALS09 (N)
SN74HC09 (N)
SN74LS09 (J, N)
SN74S09 (J, N)

TRIPLE 3-INPUT
POSITIVE-NAND GATES

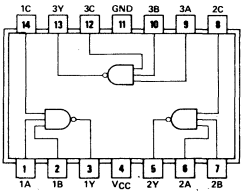
10

positive logic:
$Y = \overline{ABC}$

See page 6-2



SN5410 (J)
SN54ALS10 (J)
SN54AS10 (J)
SN54HC10 (J)
SN54LS10 (J, W)
SN54S10 (J, W)
SN7410 (J, N)
SN74ALS10 (N)
SN74AS10 (N)
SN74HC10 (N)
SN74LS10 (J, N)
SN74S10 (J, N)



SN5410 (W)

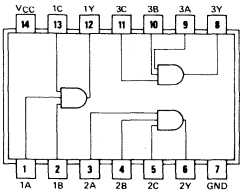
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT POSITIVE-AND GATES

11

positive logic:
Y = ABC

See page 6-10



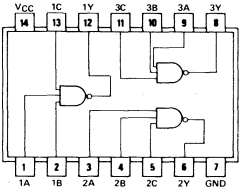
SN54ALS11 (J) **SN74ALS11 (N)**
SN54AS11 (J) **SN74AS11 (N)**
SN54HC11 (J) **SN74HC11 (N)**
SN54LS11 (J, W) **SN74LS11 (J, N)**
SN54S11 (J, W) **SN74S11 (J, N)**

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

12

positive logic:
$Y = \overline{ABC}$

See page 6-4



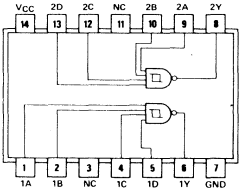
SN5412 (J, W) **SN7412 (J, N)**
SN54LS12 (J, W) **SN74LS12 (J, N)**
SN54ALS12 (J) **SN74ALS12 (N)**

DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

13

positive logic:
$Y = \overline{ABCD}$

See page 6-14



SN5413 (J, W) **SN7413 (J, N)**
SN54LS13 (J, W) **SN74LS13 (J, N)**

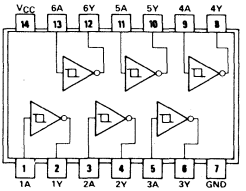
NC—No internal connection

HEX SCHMITT-TRIGGER INVERTERS

14

positive logic:
$Y = \overline{A}$

See page 6-14



SN5414 (J, W) **SN7414 (J, N)**
SN54HC14 (J) **SN74HC14 (N)**
SN54LS14 (J, W) **SN74LS14 (J, N)**

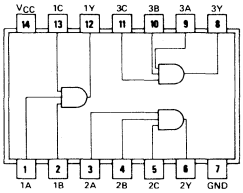
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

15

positive logic:
$Y = ABC$

See page 6-12



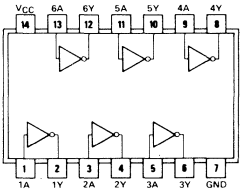
SN54ALS15 (J) SN74ALS15 (N)
SN54LS15 (J, W) SN74LS15 (J, N)
SN54S15 (J, W) SN74S15 (J, N)

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

16

positive logic:
$Y = \overline{A}$

See page 6-24



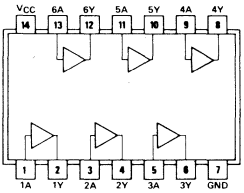
SN5416 (J, W) SN7416 (J, N)
SN54LS16 (J, W) SN74LS16 (J, N)

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

17

positive logic:
$Y = A$

See page 6-24



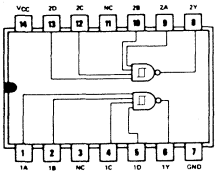
SN5417 (J, W) SN7417 (J, N)
SN54LS17 (J, W) SN74LS17 (J, N)

SCHMITT TRIGGER POSITIVE NAND GATE
WITH TOTEM POLE OUTPUT

18

positive logic:
$Y = \overline{ABCD}$

See page 6-60



SN54LS18 (J or W) SN74LS18 (J or N)

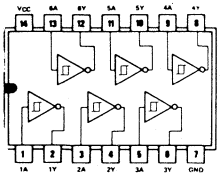
PIN ASSIGNMENTS (TOP VIEW)

SCHMITT TRIGGER INVERTER WITH TOTEM POLE OUTPUT

19

positive logic:
$Y = \overline{A}$

See page 6-60



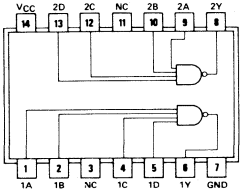
SN54LS19 (J or W) SN74LS19 (J or N)

DUAL 4-INPUT POSITIVE-NAND GATES

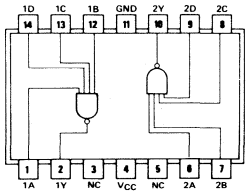
20

positive logic:
$Y = \overline{ABCD}$

See page 6-2



SN5420 (J) **SN7420 (J, N)**
SN54ALS20A (J) **SN74ALS20A (N)**
SN54AS20 (J) **SN74AS20 (N)**
SN54HC20 (J) **SN74HC20 (N)**
SN54LS20 (J, W) **SN74LS20 (J, N)**
SN54S20 (J, W) **SN74S20 (J, N)**



SN5420 (W)

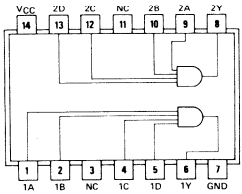
NC—No internal connection

DUAL 4-INPUT POSITIVE-AND GATES

21

positive logic:
$Y = ABCD$

See page 6-10



SN54ALS21 (J) **SN74ALS21 (N)**
SN54AS21 (J) **SN74AS21 (N)**
SN54HC21 (J) **SN74HC21 (N)**
SN54LS21 (J, W) **SN74LS21 (J, N)**

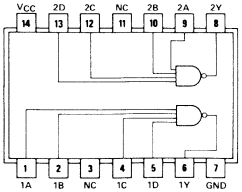
NC—No internal connection

DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

22

positive logic:
$Y = \overline{ABCD}$

See page 6-4



SN5422 (J, W) **SN7422 (J, N)**
SN54ALS22A (J) **SN74ALS22A (N)**
SN54LS22 (J, W) **SN74LS22 (J, N)**
SN54S22 (J, W) **SN74S22 (J, N)**

NC—No internal connection

PIN ASSIGNMENTS (TOP VIEWS)

EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

23

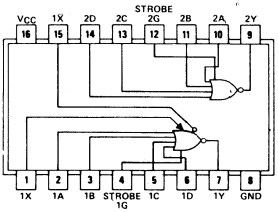
positive logic:

$1Y = \overline{1G(1A+1B+1C+1D)+X}$

$2Y = \overline{2G(2A+2B+2C+2D)}$

X = output of SN5460/SN7460

See page 6-39



SN5423 (J, W) SN7423 (J, N)

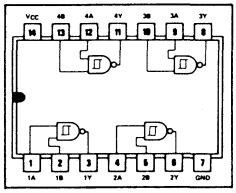
SCHMITT TRIGGER POSITIVE NAND GATE WITH TOTEM POLE OUTPUT

24

positive logic:

$Y = \overline{A \cdot B}$

See page 6-60



SN54LS24 (J or W) SN74LS24 (J or N)

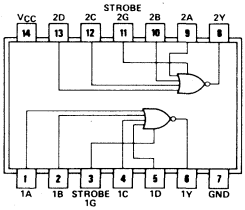
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

25

positive logic:

$Y = \overline{G(A+B+C+D)}$

See page 6-8



SN5425 (J, W) SN7425 (J, N)

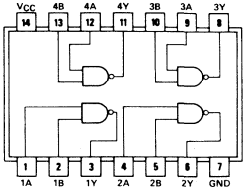
QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

26

positive logic:

$Y = \overline{AB}$

See pages 6-24 and 6-26



SN5426 (J) SN7426 (J, N)
SN54LS26 (J, W) SN74LS26 (J, N)

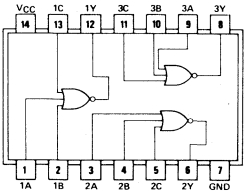
PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 3-INPUT POSITIVE-NOR GATES

27

positive logic:
$Y = \overline{A+B+C}$

See page 6-8



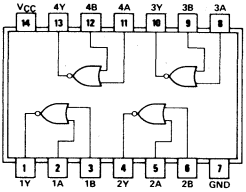
SN5427 (J, W) SN7427 (J, N)
SN54ALS27 (J) SN74ALS27 (N)
SN54AS27 (J) SN74AS27 (N)
SN54HC27 (J) SN74HC27 (N)
SN54LS27 (J, W) SN74LS27 (J, N)

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS

28 (equivalent to 1002)

positive logic:
$Y = \overline{A+B}$

See page 6-20



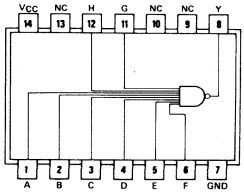
SN5428 (J, W) SN7428 (J, N)
SN54LS28 (J, W) SN74LS28 (J, N)
SN54ALS28 (J) SN74ALS28 (N)

8-INPUT POSITIVE-NAND GATES

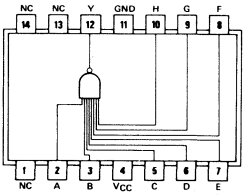
30

positive logic:
$Y = \overline{ABCDEFGH}$

See page 6-2



SN5430 (J) SN7430 (J, N)
SN54ALS30 (J) SN74ALS30 (N)
SN54AS30 (J) SN74AS30 (N)
SN54HC30 (J) SN74HC30 (N)
SN54LS30 (J, W) SN74LS30 (J, N)
SN54S30 (J, W) SN74S30 (J, N)



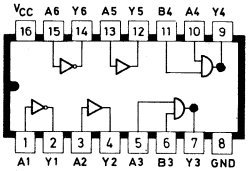
SN5430 (W)

NC – No internal connection

DELAY ELEMENTS

31

See page 6-62



SN74LS31 (J, N)

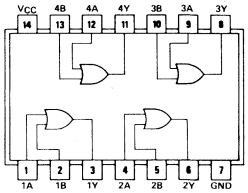
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
$Y = A+B$

See page 6-28



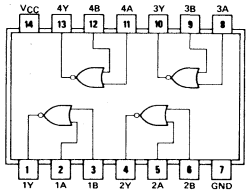
SN5432 (J, W) SN7432 (J, N)
SN54ALS32 (J) SN74ALS32 (N)
SN54AS32 (J) SN74AS32 (N)
SN54HC32 (J) SN74HC32 (N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

33

positive logic:
$Y = \overline{A+B}$

See pages 6-24 and 6-26



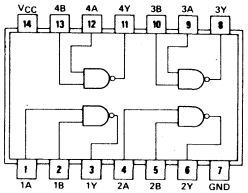
SN5433 (J, W) SN7433 (J, N)
SN54LS33 (J, W) SN74LS33 (J, N)
SN54ALS33 (J) SN74ALS33 (N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

37 (equivalent to 1000)

positive logic:
$Y = \overline{AB}$

See page 6-20



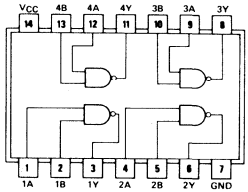
SN5437 (J, W) SN7437 (J, N)
SN54LS37 (J, W) SN74LS37 (J, N)
SN54S37 (J, W) SN74S37 (J, N)
SN54ALS37 (J) SN74ALS37 (N)

QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

38 (equivalent to 1003)

positive logic:
$Y = \overline{AB}$

See pages 6-24 and 6-26



SN5438 (J, W) SN7438 (J, N)
SN54LS38 (J, W) SN74LS38 (J, N)
SN54S38 (J, W) SN74S38 (J, N)
SN54ALS38 (J) SN74ALS38 (N)

PIN ASSIGNMENTS (TOP VIEWS)

QUAD 2-INPUT
POSITIVE-NAND BUFFERS

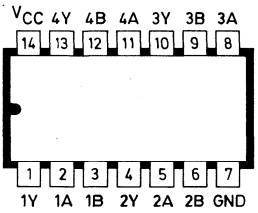
39 OPEN COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A \cdot B}$ or $Y = \overline{A + B}$

See page: **6-64**

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H



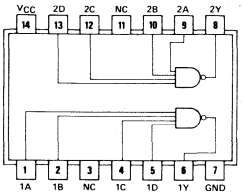
SN5439 (J) **SN7439 (J, N)**

DUAL 4-INPUT
POSITIVE-NAND BUFFERS

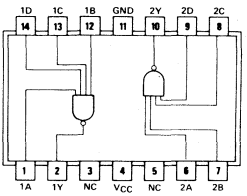
40 (equivalent to 1020)

positive logic:
$Y = \overline{ABCD}$

See page **6-20**



SN5440 (J) **SN7440 (J, N)**
SN54ALS40 (J) **SN74ALS40 (N)**
SN54LS40 (J, W) **SN74LS40 (J, W)**
SN54S40 (J, W) **SN74S40 (J, N)**



SN5440 (W)

NC – No internal connection

---

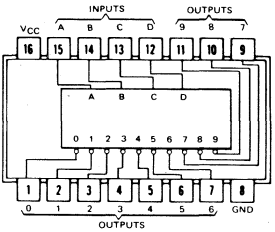
4 LINE-TO-10-LINE DECODERS

42 BCD-TO-DECIMAL

43 EXCESS-3-TO-DECIMAL

44 EXCESS-3-GRAY-TO-DECIMAL

See page **7-2**

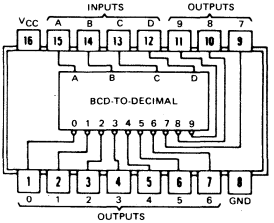


SN5442A (J, W) **SN7442A (J, N)**
SN54HC42 (J) **SN74HC42 (N)**
SN54LS42 (J, W) **SN74LS42 (J, N)**
SN5443A (J, W) **SN7443A (J, N)**
SN5444A (J, W) **SN7444A (J, N)**

BCD-TO-DECIMAL DECODER/DRIVER

45 LAMP, RELAY, OR MOS DRIVER
80-mA CURRENT SINK
OUTPUTS OFF FOR INVALID CODES

See page **7-6**



SN5445 (J, W) **SN7445 (J, N)**

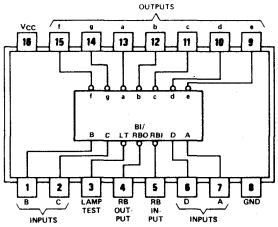
PIN ASSIGNMENTS (TOP VIEWS)

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

46 ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

47 ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS

See page 7-8

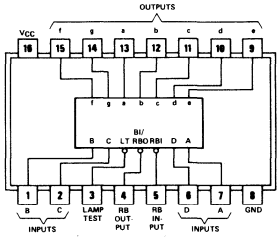


SN5446A (J, W) **SN7446A (J, N)**
SN5447A (J, W) **SN7447A (J, N)**
SN54LS47 (J, W) **SN74LS47 (J, N)**

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

48 INTERNAL PULL-UP OUTPUTS

See page 7-8

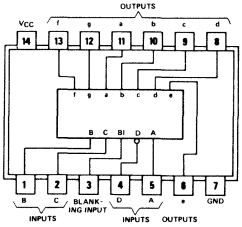


SN5448 (J, W) **SN7448 (J, N)**
SN54LS48 (J, W) **SN74LS48 (J, N)**

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

49 OPEN-COLLECTOR OUTPUTS

See page 7-8



SN5449 (W)
SN54LS49 (J, W) **SN74LS49 (J, N)**

PIN ASSIGNMENTS (TOP VIEWS)

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

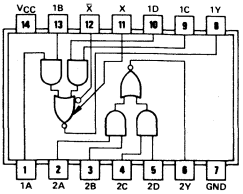
50

positive logic:

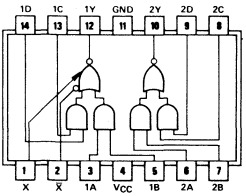
$Y = \overline{AB+CD+X}$

'50: X = output of SN5460/SN7460

See page 6-39



SN5450 (J) SN7450 (J, N)



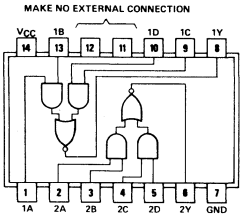
SN5450 (W)

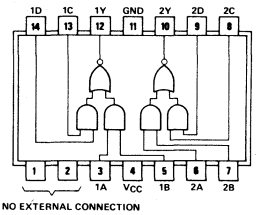
AND-OR-INVERT GATES

51

'51, 'S51
DUAL 2-WIDE 2-INPUT
positive logic:

$Y = \overline{AB+CD}$





SN5451 (J) SN7451 (J, N)
SN54HC51 (J) SN74HC51 (N)
SN54S51 (J, W) SN74S51 (J, N)

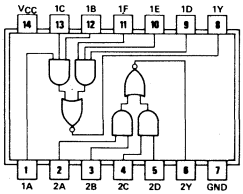
SN5451 (W)

'LS51
2-WIDE 3-INPUT, 2-WIDE 2-INPUT
positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

See page 6-30



SN54LS51 (J, W) SN74LS51 (J, N)

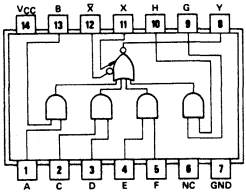
PIN ASSIGNMENTS (TOP VIEWS)

EXPANDABLE 4-WIDE AND-OR-INVERT GATES

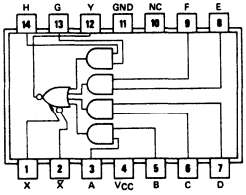
53

'53
positive logic:
$Y = \overline{AB+CD+EF+GH+X}$
X = output of SN5460/SN7460

See page 6-39



SN5453 (J) **SN7453 (J, N)**



SN5453 (W)

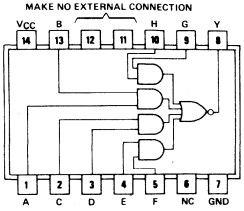
NC—No internal connection

PIN ASSIGNMENTS (TOP VIEWS)

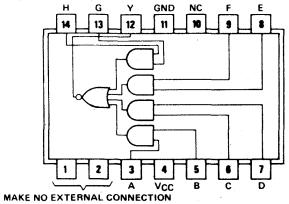
4-WIDE AND-OR-INVERT GATES

54

'54
positive logic:
$Y = \overline{AB+CD+EF+GH}$

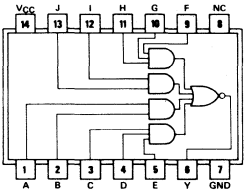


SN5454 (J) SN7454 (J, N)



SN5454 (W)

'LS54
positive logic:
$Y = \overline{AB+CDE+FGH+IJ}$



SN54LS54 (J, W) SN74LS54 (J, N)

See page 6-30

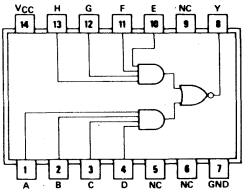
NC—No internal connection

PIN ASSIGNMENTS (TOP VIEWS)

2-WIDE 4-INPUT AND-OR-INVERT GATES

55

'LS55
positive logic:
$Y = \overline{ABCD+EFGH}$



SN54LS55 (J, W) SN74LS55 (J, N)

See pages 6-30 and 6-39

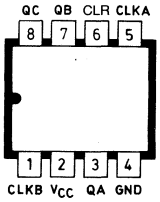
NC—No internal connection

FREQUENCY DIVIDERS

56 50-TO-1

57 60-TO-1

See page 7-20

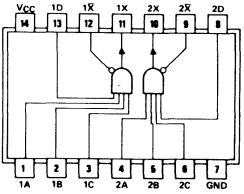


SN54LS56 (JG) SN74LS56 (JG, P)
SN54LS57 (JG) SN74LS57 (JG, P)

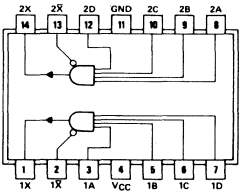
DUAL 4-INPUT EXPANDERS

60

positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453



SN5460 (J) SN7460 (J, N)



SN5460 (W)

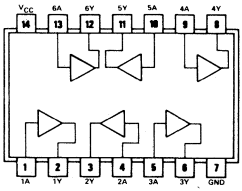
NC—No internal connection

See pages 6-43 and 6-44

PIN ASSIGNMENTS (TOP VIEWS)

HEX CURRENT-SENSING INTERFACE GATES

63 TRANSLATES LOW-LEVEL INPUT CURRENT TO LOW-LEVEL VOLTAGE
AND
HIGH-LEVEL CURRENT TO HIGH-LEVEL VOLTAGE



SN54LS63(J,W) SN74LS63(J,N)

See page 6-66

PIN ASSIGNMENTS (TOP VIEWS)

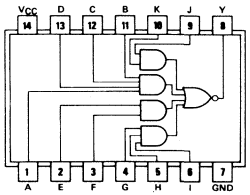
4-2-3-2 INPUT AND-OR-INVERT GATES

64 TOTEM-POLE OUTPUT

65 OPEN-COLLECTOR OUTPUT

positive logic: $\overline{Y = ABCD+EF+GHI+JK}$

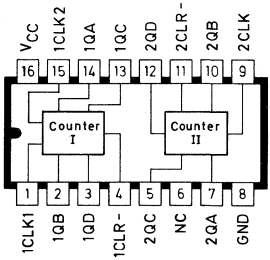
See pages 6-30 and 6-32



SN54S64 (J, W) **SN74S64 (J, N)**
SN54S65 (J, W) **SN74S65 (J, N)**

DUAL 40 MHz DECADE COUNTER

68

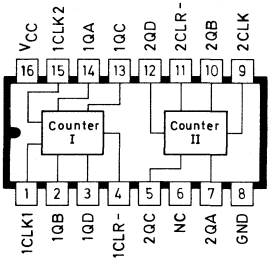


See page: **7-24**

SN54LS68 (J) **SN74LS68 (J, N)**

DUAL 40 MHz 4 BIT BINARY COUNTER

69



See page: **7-27**

SN54LS69 (J) **SN74LS69 (J, N)**

See explanation of function tables on page 3-8.

PIN ASSIGNMENTS (TOP VIEWS)

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

70 FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↑	L	L	Q_0	$\overline{Q}_0$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q_0	$\overline{Q}_0$

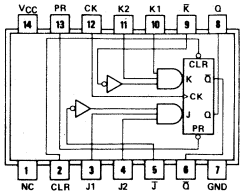
positive logic: $J = J1 \cdot J2 \cdot \overline{J}$

$K = K1 \cdot K2 \cdot \overline{K}$

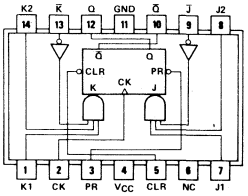
If inputs $\overline{J}$ and $\overline{K}$ are not used, they must be grounded.

Preset or clear function can occur only when the clock input is low.

See page 6-46



SN5470 (J) SN7470 (J, N)



SN5470 (W)

NC—No internal connection

See explanation of function tables on page 3-8.

5

PIN ASSIGNMENTS (TOP VIEWS)

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

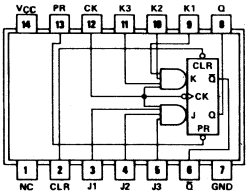
72

FUNCTION TABLE

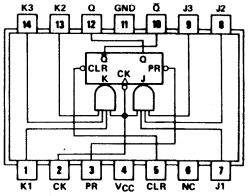
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

positive logic: J = J1·J2·J3; K1·K2·K3

See pages 6-46 and 6-50



SN5472 (J) SN7472 (J, N)



SN5472 (W)

NC—No internal connection

DUAL J-K FLIP-FLOPS WITH CLEAR

73

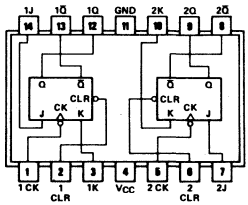
'73,
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

'LS73A, 'HC73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50 and 6-54



SN5473 (J, W) SN7473 (J, N)
SN54HC73 (J) SN74HC73 (N)
SN54LS73A (J, W) SN74LS73A (J, N)

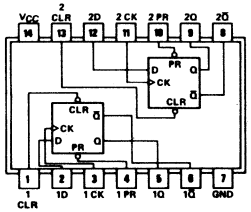
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

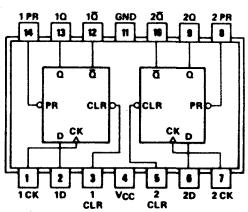
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54 and 6-56



SN5474 (J) SN7474 (J, N)
SN54ALS74 (J) SN74ALS74 (N)
SN54AS74 (J) SN74AS74 (N)
SN54HC74 (J) SN74HC74 (N)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)



SN5474 (W)

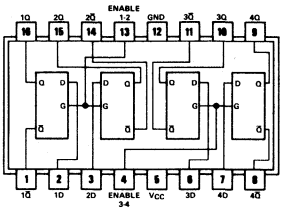
See explanation of function tables on page 3-8.

* This configuration is non-stable, that is, it will not persist when preset or clear input returns to its inactive (high) level. Furthermore, in this configuration the output levels of the 'LS74A are not guaranteed to meet the minimum limits for VOH if the low level voltages a preset and clear are near VIL maximum.

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT BISTABLE LATCHES

75



SN5475 (J, W) SN7475 (J, N)
SN54HC75 (J) SN74HC75 (N)
SN54LS75 (J, W) SN74LS75 (J, N)

FUNCTION TABLE
(Each Latch)

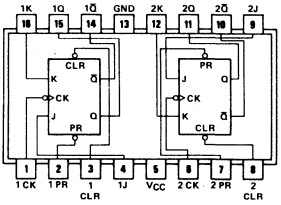
INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transistion of G

See page 7-30

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR

76



SN5476 (J, W) SN7476 (J, N)
SN54HC76 (J) SN74HC76 (N)
SN54LS76A (J, W) SN74LS76A (J, N)

'76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

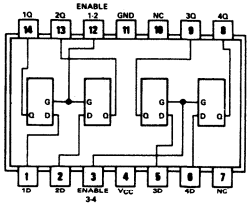
'LS76A, 'HC76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50 and 6-54

4-BIT BISTABLE LATCHES

77



SN5477 (W)
SN54HC77 (J) SN74HC77 (N)
SN54LS77 (W)

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transistion of G

See page 7-30

See explanation of function tables on page 3-8.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN ASSIGNMENTS (TOP VIEWS)

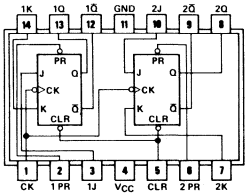
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

78

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-50 and 6-54



SN54HC78 (J) SN74HC78 (N)
SN54LS78A (J, W) SN74LS78A (J, N)

GATED FULL ADDERS

80 GATED COMPLEMENTARY INPUTS
COMPLEMENTARY SUM OUTPUTS

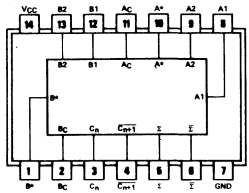
FUNCTION TABLE
(See Notes 1, 2, and 3)

INPUTS			OUTPUTS		
C_n	B	A	$\bar{C}_{n+1}$	$\bar{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

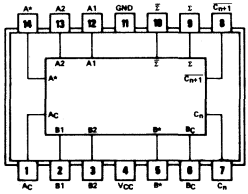
H = high level, L = low level

NOTES: 1. $A = \bar{A}_c + \bar{A}\star + A1 \cdot A2$, $B = \bar{B}_c + B\star + B1 \cdot B2$.
2. When A☆ is used as an input, A1 or A2 must be low. When B☆ is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A☆ or B☆, respectively, must be open or used to perform dot-AND logic.

See page 7-35



SN5480(J) SN7480 (J, N)



SN5480(W)

See explanation of function tables on page 3-8.

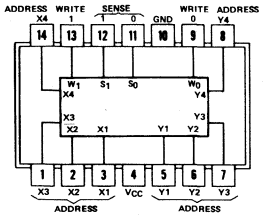
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN ASSIGNMENTS (TOP VIEWS)

16-BIT RANDOM-ACCESS MEMORIES

81

See page 7-38

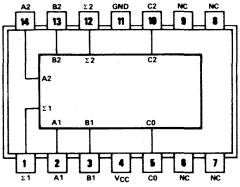


SN5481A (J, W) SN7481A (J, N)

2-BIT BINARY FULL ADDERS

82

See page 7-43



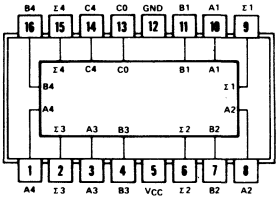
SN5482 (J, W) SN7482 (J, N)

NC—No internal connection

4-BIT BINARY FULL ADDERS WITH FAST CARRY

83

See page 7-46

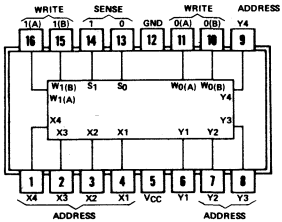


SN5483A (J, W) SN74 83A (J, N)
SN54LS83A (J, W) SN74LS83A (J, N)

16-BIT RANDOM-ACCESS MEMORIES

84

See page 7-38

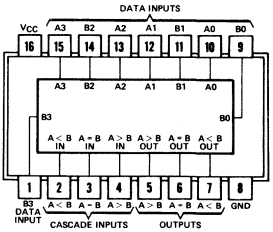


SN5484A (J, W) SN7484A (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT MAGNITUDE COMPARATORS

85

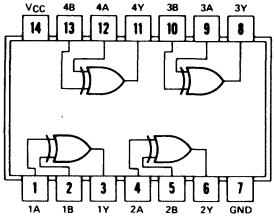


SN5485 (J, W) **SN7485 (J, N)**
SN54HC85 (J) **SN74HC85 (N)**
SN54LS85 (J, W) **SN74LS85 (J, N)**
SN54S85 (J, W) **SN74S85 (J, N)**

See page 7-50

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \overline{A}B + A\overline{B}$



SN5486 (J, W) **SN7486 (J, N)**
SN54ALS86 (J) **SN74ALS86 (N)**
SN54HC86 (J) **SN74HC86 (N)**
SN54LS86A (J, W) **SN74LS86A (J, N)**
SN54S86 (J, W) **SN74S86 (J, N)**

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

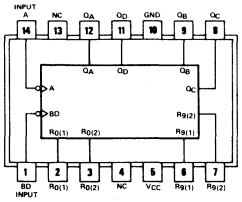
H = high level, L = low level

See page 7-57

PIN ASSIGNMENTS (TOP VIEWS)

DECADE COUNTERS

90 DIVIDE-BY-TWO AND DIVIDE-BY FIVE



SN5490A (J, W) **SN7490A (J, N)**
SN54LS90 (J, W) **SN74LS90 (J, N)**

NC – No internal connection

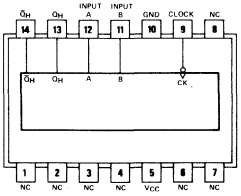
See page 7-63

5

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT SHIFT REGISTERS

91 SERIAL-IN, SERIAL-OUT
GATED INPUT

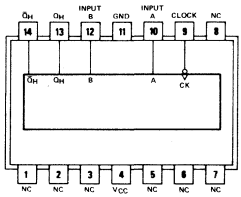


SN5491A (J) **SN7491A (J,N)**
SN54LS91 (J) **SN74LS91 (J, N)**

FUNCTION TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = high, L = low
X = irrelevant
t_n = Reference bit time, clock low
t_{n+8} = Bit time after 8 low-to-high clock transitions



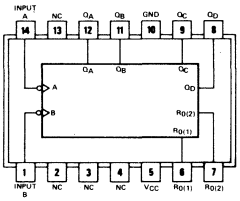
SN5491A (W)
SN54LS91 (W)

NC — No internal connections

See page 7-71

DIVIDE-BY-TWELVE COUNTERS

92 DIVIDE-BY-TWO AND DIVIDE-BY-SIX



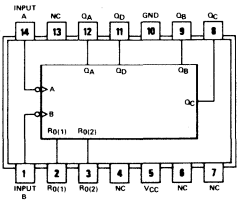
SN5492A (J, W) **SN7492A (J, N)**
SN54LS92 (J, W) **SN74LS92 (J, N)**

NC—No internal connection

See page 7-63

4-BIT BINARY COUNTERS

93 DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT



SN5493A (J, W) **SN7493A (J, N)**
SN54LS93 (J, W) **SN74LS93 (J, N)**

NC—No internal connection

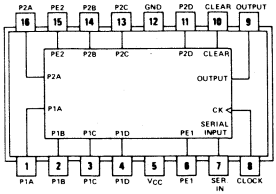
See page 7-63

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT SHIFT REGISTERS

94 DUAL ASYNCHRONOUS PRESETS

See page 7-75

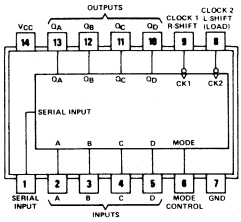


SN5494 (J, W) SN7494 (J, N)

4-BIT SHIFT REGISTERS

95 PARALLEL IN/PARALLEL OUT
SHIFT RIGHT, SHIFT LEFT
SERIAL INPUT

See page 7-79

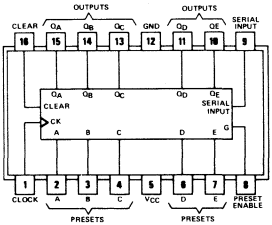


SN5495A (J, W) SN7495A (J, N)
SN54AS95 (J) SN74AS95 (N)
SN54LS95B (J, W) SN74LS95B (J, N)

5-BIT SHIFT REGISTERS

96 ASYNCHRONOUS PRESET

See page 7-83

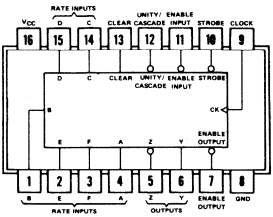


SN5496 (J, W) SN7496 (J, N)
SN54LS96 (J, W) SN74LS96 (J, N)

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

97

See page 7-89



SN5497 (J, W) SN7497 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT BISTABLE LATCHES

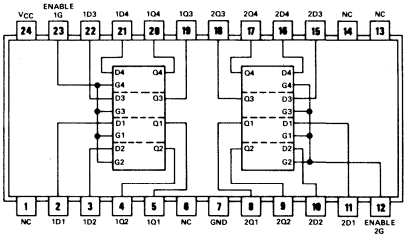
100

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

See page 7-94



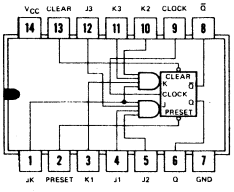
SN54100 (J, W) **SN74100 (J, N, NT)**

NC – No internal connection

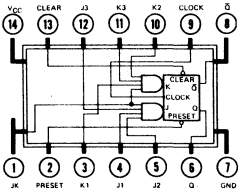
PIN ASSIGNMENTS (TOP VIEWS)

GATED J-K MASTER-SLAVE FLIP FLOP

104



SN54104 (J) SN74104 (J or N)

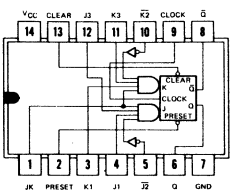


SN54104 (W)

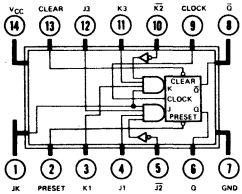
See page: **6-68**

GATED J-K MASTER-SLAVE FLIP FLOP

105



SN54105 (J) SN74105 (J or N)



SN54105 (W)

See page: **6-68**

PIN ASSIGNMENTS (TOP VIEWS)

DUAL J-K FLIP-FLOPS WITH CLEAR

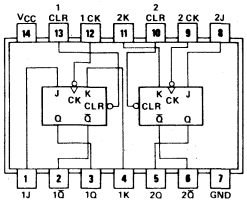
107

'107
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

'LS107A, 'HC107
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54107 (J) SN74107 (J, N)
SN54HC107 (J) SN74HC107 (N)
SN54LS107A (J) SN74LS107A (J, N)

See pages 6-46 and 6-54

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN ASSIGNMENTS (TOP VIEWS)

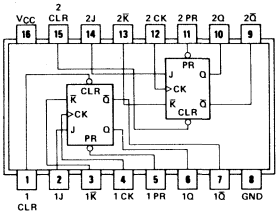
DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

109

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

See pages 6-46 and 6-54



SN54109 (J, W) SN74109 (J, N)
SN54ALS109 (J) SN74ALS109 (N)
SN54AS109 (J) SN74AS109 (N)
SN54HC109 (J) SN74HC109 (N)
SN54LS109A (J, W) SN74ALS109A (J, N)

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

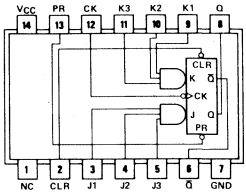
110

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1•J2•J3
K = K1•K2•K3

See page 6-46



SN54110 (J, W) SN74110 (J, N)

NC—No internal connection

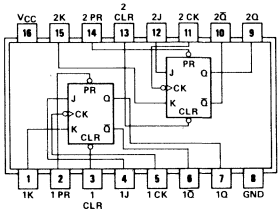
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

111

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

See page 6-46



SN54111 (J, W) SN74111 (J, N)

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

PIN ASSIGNMENTS (TOP VIEWS)

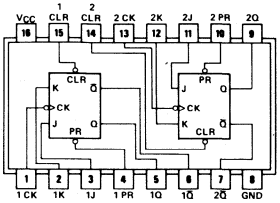
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

112

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-54 and 6-56



SN54ALS112 (J) SN74ALS112 (N)
SN54AS112 (J) SN74AS112 (N)
SN54HC112 (J) SN74HC112 (N)
SN54LS112A (J, W) SN74LS112A (J, N)
SN54S112 (J, W) SN74S112 (J, N)

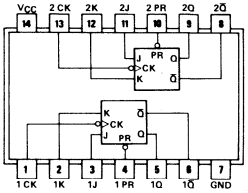
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

113

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-54 and 6-56



SN54ALS113 (J) SN74ALS113 (N)
SN54AS113 (J) SN74AS113 (N)
SN54HC113 (J) SN74HC113 (N)
SN54LS113A (J, W) SN74LS113A (J, N)
SN54S113 (J, W) SN74S113 (J, N)

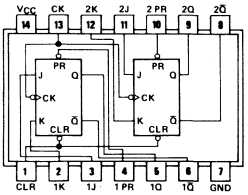
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

114

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See pages 6-54 and 6-56



SN54ALS114 (J) SN74ALS114 (N)
SN54AS114 (J) SN74AS114 (N)
SN54HC114 (J) SN74HC114 (N)
SN54LS114A (J, W) SN74LS114A (J, N)
SN54S114 (J, W) SN74S114 (J, N)

See explanation of function tables on page 3-8.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

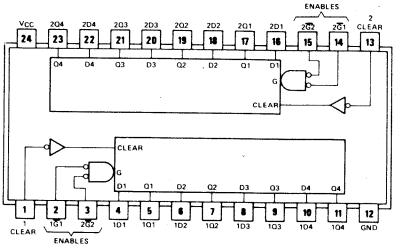
PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-BIT LATCHES

116

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
CLEAR	ENABLE		DATA	Q
	$\overline{G}1$	$\overline{G}2$		
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

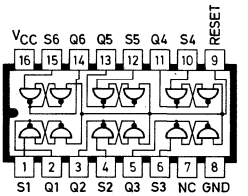


See page **7-96**

SN54116 (J, W) **SN74116 (J, N, NT)**

HEX SET-RESET LATCH

118

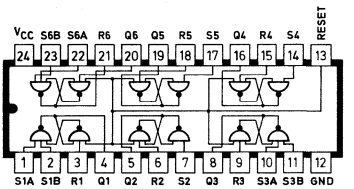


See page: **7-99**

SN54118 (J, W) **SN54118 (J or N)**

HEX SET-RESET LATCH

119



See page: **7-102**

SN54119 (J, W) **SN74119 (J, N)**

See explanation of function tables on page 3-8

PIN ASSIGNMENTS (TOP VIEWS)

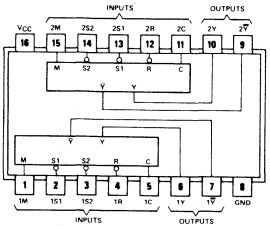
DUAL PULSE SYNCHRONIZERS/DRIVERS

120

FUNCTION TABLE

INPUTS			FUNCTION
R	S1	S2	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

†Operation initiated by last ↓ transition continues.



See page 7-105

SN54120 (J, W) SN74120 (J, N)

MONOSTABLE MULTIVIBRATORS

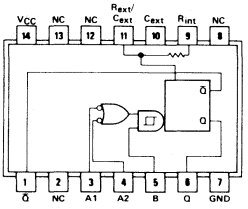
121

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H*
X	X	L	L	H*
H	H	X	L	H*
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.

2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.



SN54121 (J, W) SN74121 (J, N)

'121 . . . R_{int} = 2 kΩ NOM

NC—No internal connection

See page 6-73

See explanation of function tables on page 3-8.

* "These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough for any pulse started before the setup to have been completed."

PIN ASSIGNMENTS (TOP VIEWS)

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

122

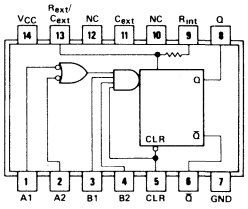
FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H*
X	X	X	L	X	L	H*
X	X	X	X	L	L	H*
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

See page 6-85

*



SN54122 (J, W) **SN74122 (J, N)**
SN54LS122 (J, W) **SN74LS122 (J, N)**
'122 . . . R_{int} = 10 kΩ NOM
'LS122 . . . R_{int} = 10 kΩ NOM

NC—No internal connection

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

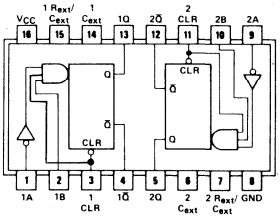
123

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H*
X	X	L	L	H*
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See page 6-85

*



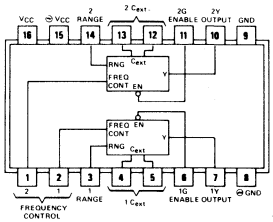
SN54123 (J, W) **SN74123 (J, N)**
SN54HC123 (J) **SN74HC123 (N)**
SN54LS123 (J, W) **SN74LS123 (J, N)**

DUAL VOLTAGE-CONTROLLED OSCILLATORS

124

See page 7-110

*



SN54S124 (J, W) **SN74S124 (J, N)**

NC—No internal connection

† See explanation of function tables on page 3.8.

* "These lines of the function table assume that the indicated steady-state conditions at the A and B inputs have been setup long enough for any pulse started before the setup to have been completed."

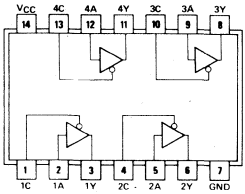
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

125

positive logic:
Y = A
Output is off (disabled) when C is high.

See page 6-33



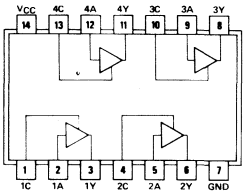
SN54125 (J, W) SN74125 (J, N)
SN54HC125 (J) SN74HC125 (N)
SN54LS125A (J, W) SN74LS125A (J, N)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

126

positive logic:
Y = A
Output is off (disabled) when C is low.

See page 6-33



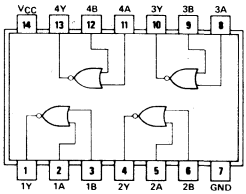
SN54126 (J, W) SN74126 (J, N)
SN54HC126 (J) SN74HC126 (N)
SN54LS126A (J, W) SN74LS126A (J, N)

SN54128 . . . 75-OHM LINE DRIVER
SN74128 . . . 50-OHM LINE DRIVER

128

positive logic:
$Y = \overline{A+B}$

See page 6-22

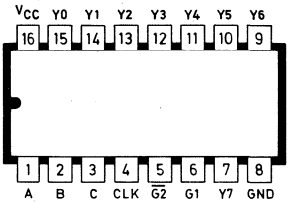


SN54128 (J, W) SN74128 (J, N)

3 LINE TO 8 LINE DECODER/DEMULTIPLEXER EDGE TRIGGERED ADDRESS REGISTERS

131

See Volume II



SN54ALS131 (J) SN74ALS131 (N)
SN54AS131 (J) SN74AS131 (N)

5

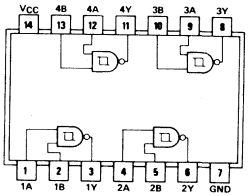
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

132

positive logic:
$Y = \overline{AB}$

See page 6-14



SN54132 (J, W) **SN74132 (J, N)**
SN54HC132 (J) **SN74HC132 (N)**
SN54LS132 (J, W) **SN74LS132 (J, N)**
SN54S132 (J, W) **SN74S132 (J, N)**

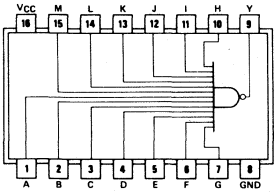
PIN ASSIGNMENTS (TOP VIEWS)

13-INPUT POSITIVE-NAND GATES

133

positive logic:
$Y = \overline{ABCDEFGHIJKLM}$

See page 6-2



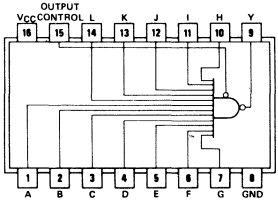
SN54ALS133 (J) SN74ALS133 (N)
SN54HC133 (J) SN74HC133 (N)
SN54S133 (J, W) SN74S133 (J, N)

12-INPUT POSITIVE-NAND GATES WITH THREE-STATE OUTPUTS

134

positive logic:
$Y = \overline{ABCDEFGHIJKL}$
Output is off (disabled) when output control is high.

See page 6-33



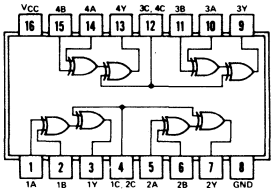
SN54S134 (J, W) SN74S134 (J, N)

QUAD EXCLUSIVE-OR GATES

135

positive logic: $Y = (A \oplus B) \oplus C = A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$

See page 7-115



SN54AS135 (J, W) SN74S135 (J, N)

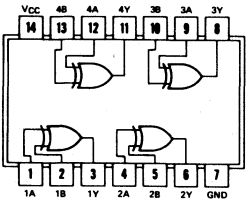
NC—No internal connection

QUAD EXCLUSIVE-OR GATES

136

positive logic: $Y = A \oplus B = A\overline{B} + \overline{A}B$

See page 7-117

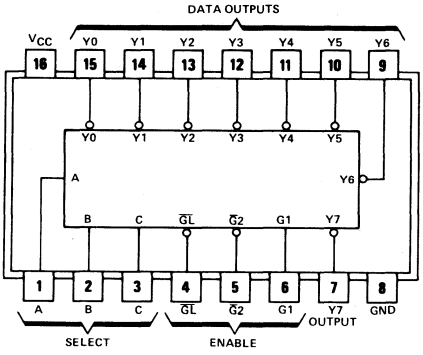


SN54136 (J, W) SN74136 (J, N)
SN54ALS136 (J) SN74ALS136 (N)
SN54LS136 (J, W) SN74LS136 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCHES

137

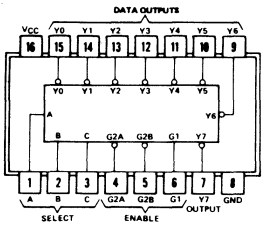


SN54ALS137 (J) **SN74ALS137 (J or N)**
SN54HC137 (J) **SN74HC137 (N)**
SN54LS137 (J) **SN74LS137 (J or N)**

See page 7-120

3-TO-8 LINE DECODERS/MULTIPLEXERS

138

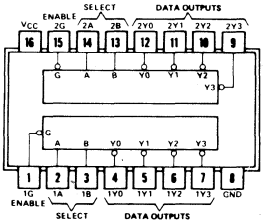


See page 7-124

SN54ALS138 (J, W) **SN74ALS138 (N)**
SN54HC138 (J) **SN74HC138 (N)**
SN54LS138 (J, W) **SN74LS138 (J, N)**
SN54S138 (J, W) **SN74S138 (J, N)**

DUAL 2-TO-4 LINE DECODERS/MULTIPLEXERS

139



See page 7-124

SN54HC139 (J) **SN74HC139 (N)**
SN54LS139A (J, W) **SN74LS139A (J, N)**
SN54S139 (J, W) **SN74S139 (J, N)**

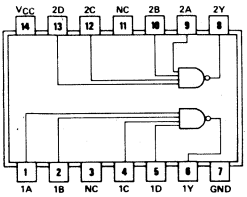
PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-INPUT POSITIVE-NAND 50-OHM LINE DRIVERS

140

positive logic:
$Y = \overline{ABCD}$

See page 6-22



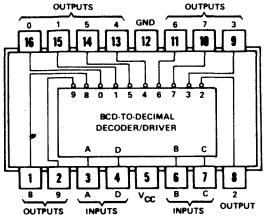
SN54S140 (J, W) SN74S140 (J, N)

NC—No internal connection

BCD-TO-DECIMAL DECODER/DRIVER

141 DRIVES COLD-CATHODE INDICATOR TUBES

See page 7-128

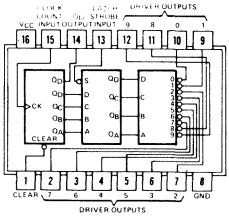


SN74141 (J, N)

COUNTER/LATCH/DECODER/DRIVER

142 DIVIDE-BY-10 COUNTER
4-BIT LATCH
4-BIT TO 7-SEGMENT DECODER
NIXIE ‡ TUBE DRIVER

See page 7-130



SN74142 (J, N)

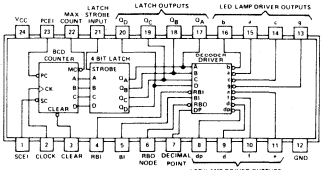
‡Nixie is a registered trademark of the Borroughs Corp.

COUNTERS/LATCHES/DECODERS/DRIVERS

143 15 mA CONSTANT CURRENT
1- TO 5-V OUTPUT RANGE

144 UP TO 15-V INDICATORS
UP TO 25 mA
OPEN-COLLECTOR OUTPUT

See page 7-133



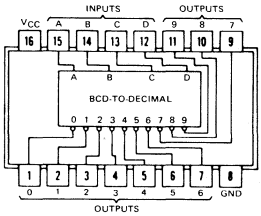
SN54143 (J, W) SN74143 (J, N, NT)
SN54144 (J, W) SN74144 (J, N, NT)

PIN ASSIGNMENTS (TOP VIEWS)

BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

145 BCD-TO-DECIMAL

See page 7-138

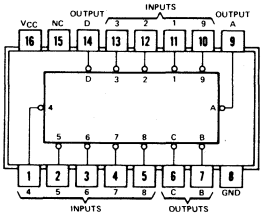


SN54145 (J, W) SN74145 (J, N)
SN54LS145 (J, W) SN74LS145 (J, W)

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODERS

147

See page 7-141



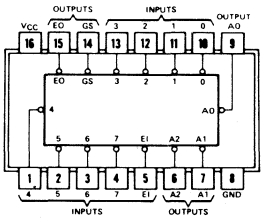
SN54147 (J, W) SN74147 (J, N)
SN54HC147 (J) SN74HC147 (N)
SN54LS147 (J, W) SN74LS147 (J, N)

NC No internal connection

8-LINE-TO-3-LINE OCTAL PRIORITY ENCODERS

148

See page 7-141

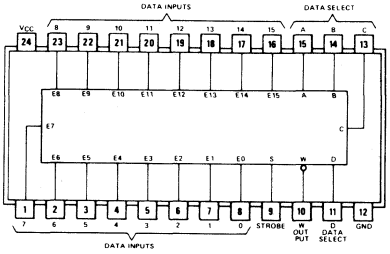


SN54148 (J, W) SN74148 (J, N)
SN54HC148 (J) SN74HC148 (N)
SN54LS148 (J, W) SN74LS148 (J, N)

1-OF-16 DATA SELECTORS/MULTIPLEXERS

150

See page 7-147



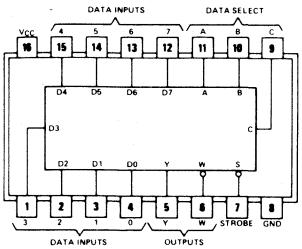
SN54150 (J, W) SN74150 (J, N, NT)
SN54AS150 (J, JT) SN74AS150 (N, NT)

PIN ASSIGNMENTS (TOP VIEWS)

1-OF-8 DATA SELECTORS/MULTIPLEXERS

151

See page 7-147

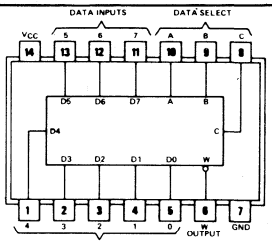


SN54151A (J, W) **SN74151A (J, N)**
SN54ALS151 (J) **SN74ALS151 (N)**
SN54AS151 (J) **SN74AS151 (N)**
SN54HC151 (J) **SN74HC151 (N)**
SN54LS151 (J, W) **SN74LS151 (J, N)**
SN54S151 (J, W) **SN74S151 (J, N)**

1-OF-8 DATA SELECTORS/MULTIPLEXERS

152

See page 7-147

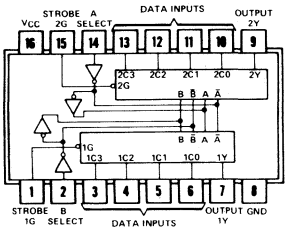


SN54152A (W) **SN74HC152 (N)**
SN54HC152 (J)
SN54LS152 (W)

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

153

See page 7-155

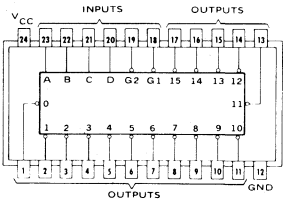


SN54153 (J, W) **SN74153 (J, N)**
SN54ALS153 (J, W) **SN74ALS153 (N)**
SN54AS153 (J, W) **SN74AS153 (N)**
SN54HC153 (J) **SN74HC153 (N)**
SN54LS153 (J, W) **SN74LS153 (J, N)**
SN54S153 (J, W) **SN74S153 (J, N)**

PIN ASSIGNMENTS (TOP VIEWS)

4-LINE TO 16-LINE DECODERS/DEMULTIPLEXERS

154



SN54154 (J, W) **SN74154 (J, N, NT)**
SN54HC154 (JT) **SN74HC154 (NT)**

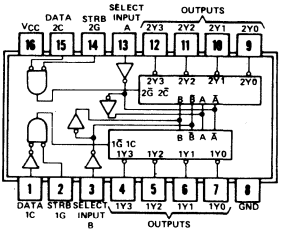
See page 7-160

DECODERS/DEMULTIPLEXERS

DUAL 2- TO 4-LINE DECODER
DUAL 1- TO 4-LINE DEMULTIPLEXER
3- TO 8-LINE DECODER
1- TO 8-LINE DEMULTIPLEXER

155 TOTEM-POLE OUTPUTS

156 OPEN-COLLECTOR OUTPUTS



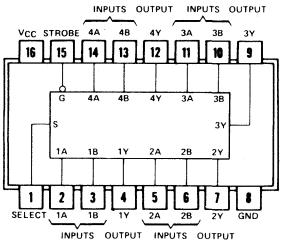
SN54155 (J, W) **SN74155 (J, N)**
SN54LS155A (J, W) **SN74LS155A (J, N)**
SN54156 (J, W) **SN74156 (J, N)**
SN54LS156 (J, W) **SN74LS156 (J, N)**

See page 7-163

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

157 NONINVERTED DATA OUTPUTS

158 INVERTED DATA OUTPUTS



SN54157 (J) **SN74157 (N)**
SN54AS157 (J) **SN74AS157 (N)**
SN54HC157 (J) **SN74HC157 (N)**
SN54LS157 (J) **SN74LS157 (N)**
SN54S157 (J) **SN74S157 (N)**
SN54AS158 (J) **SN74AS158 (N)**
SN54HC158 (J) **SN74HC158 (N)**
SN54LS158 (J, W) **SN74LS158 (J, N)**
SN54S158 (J, W) **SN74S158 (J, N)**

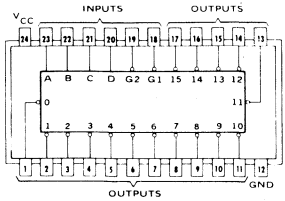
See page 7-169

PIN ASSIGNMENTS (TOP VIEWS)

4- TO 16-LINE DECODERS/DEMULTIPLEXERS

159 OPEN-COLLECTOR OUTPUTS

See page 7-175



SN54159 (J, W) SN74159 (J, N, NT)

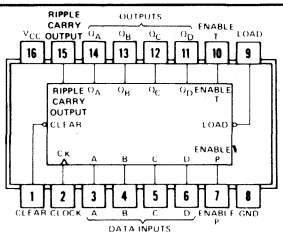
SYNCHRONOUS 4-BIT COUNTERS

160 DECADE, DIRECT CLEAR

161 BINARY, DIRECT CLEAR

162 DECADE, SYNCHRONOUS CLEAR

163 BINARY, SYNCHRONOUS CLEAR

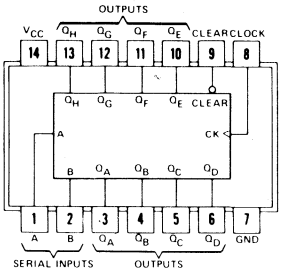


SN54160 (J, W)	SN74160 (J, N)	SN54ALS162B (J)	SN74ALS162B (N)
SN54ALS160B (J)	SN74ALS160B (N)	SN54AS162 (J)	SN74AS162 (N)
SN54AS160 (J)	SN74AS160 (N)	SN54HC162 (J)	SN74HC162 (N)
SN54HC160 (J)	SN74HC160 (N)	SN54LS162A (J, W)	SN74LS162A (J, N)
SN54LS160A (J, W)	SN74LS160A (J, N)	SN54S162 (J, W)	SN74S162 (J, N)
SN54161 (J, W)	SN74161 (J, N)	SN54163 (J, W)	SN74163 (J, N)
SN54ALS161B (J)	SN74ALS161B (N)	SN54ALS163B (J)	SN74ALS163B (N)
SN54AS161 (J)	SN74AS161 (N)	SN54AS163 (J)	SN74AS163 (N)
SN54HC161 (J)	SN74HC161 (N)	SN54HC163 (J)	SN74HC163 (N)
SN54LS161A (J, W)	SN74LS161A (J, N)	SN54LS163A (J, W)	SN74LS163A (J, N)
SN54162 (J, W)	SN74162 (J, N)	SN54S163 (J, W)	SN74S163 (J, N)

See page 7-177

8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS

164 ASYNCHRONOUS CLEAR



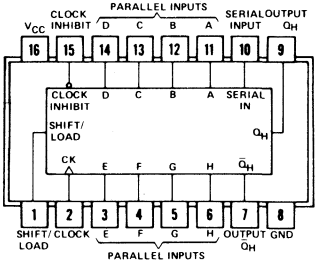
SN54164 (J, W) SN74164 (J, N)
SN54HC164 (J) SN74HC164 (N)
SN54LS164 (J, W) SN74LS164 (J, N)

See page 7-193

PIN ASSIGNMENTS (TOP VIEWS)

PARALLEL-LOAD 8-BIT SHIFT REGISTERS WITH COMPLEMENTARY OUTPUTS

165

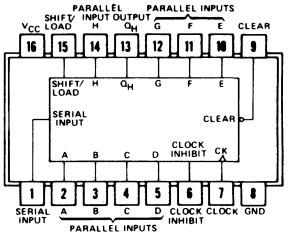


See page 7-198

SN54165 (J, W) **SN74165 (J, N)**
SN54HC165 (J) **SN74HC165 (N)**
SN54LS165A (J, W) **SN74LS165A (J, N)**

8-BIT SHIFT REGISTERS

166 PARALLEL/SERIAL INPUT
SERIAL OUTPUT

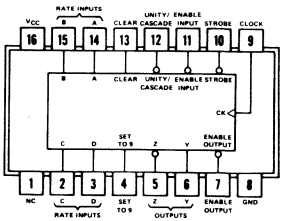


See page 7-203

SN54166 (J, W) **SN74166 (J, N)**
SN54HC166 (J) **SN74HC166 (N)**
SN54LS166A (J, W) **SN74LS166A (J, N)**

SYNCHRONOUS DECADE RATE MULTIPLIERS

167



SN54167 (J, W) **SN74167 (J, N)**

See page 7-208

NC – No internal connection

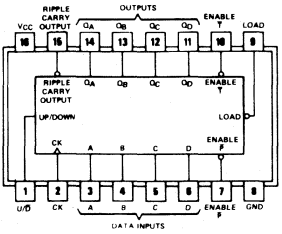
PIN ASSIGNMENTS (TOP VIEW)

4-BIT UP/DOWN SYNCHRONOUS COUNTERS

168 DECADE

169 BINARY

See page 7-212



SN54S168 (J, W)
SN54LS169B (J, W)
SN54S169 (J, W)
SN54ALS168A (J)
SN54ALS169A (J)
SN54AS168 (J)
SN54AS169 (J)

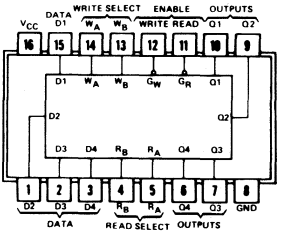
SN74S168 (J, N)
SN74LS169B (J, N)
SN74S169 (J, N)
SN74ALS168A (N)
SN74ALS169A (N)
SN74AS168 (N)
SN74AS169 (N)

4-BY-4 REGISTER FILES

170

- SEPARATE READ/WRITE ADDRESSING
- SIMULTANEOUS READ AND WRITE
- OPEN-COLLECTOR OUTPUTS
- EXPANDABLE TO 1024 WORDS

See page 7-223



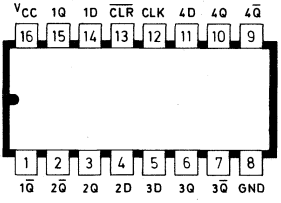
SN54170 (J, N)
SN54LS170 (J, W)

SN74170 (J, N)
SN74LS170 (J, N)

QUAD D-TYPE FLIP-FLOPS WITH CLEAR

171

See page 7-231



SN54LS171 (J, W)

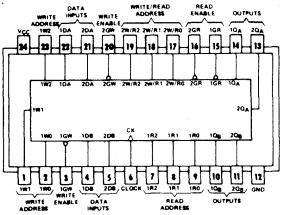
SN74LS171 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

16-BIT REGISTER FILE

172 INDEPENDENT READ/WRITE ADDRESSING
SIMULTANEOUS READ/WRITE
8-WORDS OF TWO BITS EACH
3-STATE OUTPUTS

See page 7-234

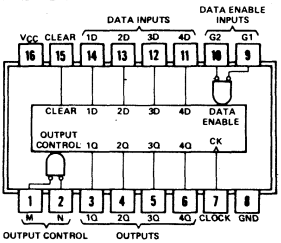


SN74172 (J, N, NT)

4-BIT D-TYPE REGISTERS

173 3-STATE OUTPUTS

See page 7-238

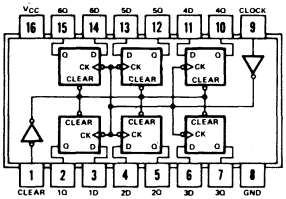


SN54173 (J, W) SN74173 (J, N)
SN54HC173 (J) SN74HC173 (N)
SN54LS173A (J, W) SN74LS173A (J, N)

HEX D-TYPE FLIP-FLOPS

174 SINGLE RAIL OUTPUTS
COMMON DIRECT CLEAR

See page 7-242

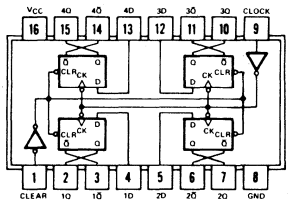


SN54174 (J, W) SN74174 (J, N)
SN54ALS174 (J, W) SN74ALS174 (N)
SN54AS174 (J) SN74AS174 (N)
SN54HC174 (J) SN74HC174 (N)
SN54LS174 (J, W) SN74LS174 (J, N)
SN54S174 (J, W) SN74174 (J, N)

QUAD D-TYPE FLIP-FLOPS

175 COMPLEMENTARY OUTPUTS
COMMON DIRECT CLEAR

See page 7-242



SN54175 (J, W) SN74175 (J, N)
SN54ALS175 (J, W) SN74ALS175 (N)
SN54AS175 (J) SN74AS175 (N)
SN54HC175 (J) SN74HC175 (N)
SN54LS175 (J, W) SN74LS175 (J, N)
SN54S175 (J, W) SN74S175 (J, N)

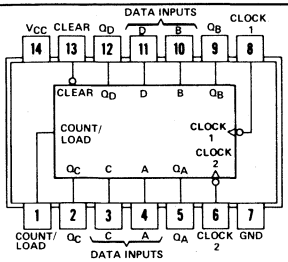
PIN ASSIGNMENTS (TOP VIEWS)

PRESETABLE COUNTERS/LATCHES

176 DECADE (BI-QUINARY)

177 BINARY

See page 7-248

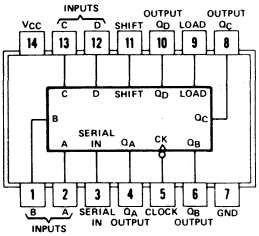


SN54176 (J, W) SN74176 (J, N)
SN54177 (J, W) SN74177 (J, N)

4-BIT UNIVERSAL SHIFT REGISTERS

178

See page 7-254

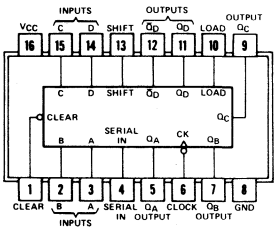


SN54178 (J, W) SN74178 (J, N)

4-BIT UNIVERSAL SHIFT REGISTERS

179 DIRECT CLEAR
Q_D COMPLEMENTARY OUTPUTS

See page 7-254

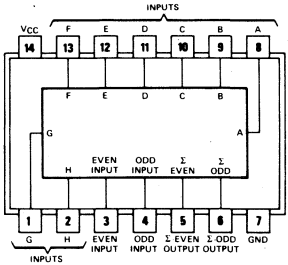


SN54179 (J, W) SN74179 (J, N)

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

180

See page 7-258

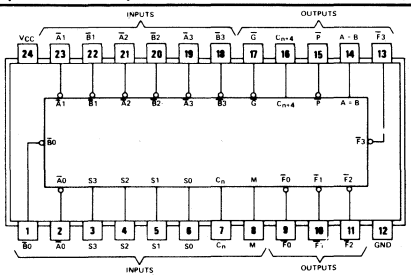


SN54180 (J, W) SN74180 (J, N)
SN54HC180 (J) SN74HC180 (N)

PIN ASSIGNMENTS (TOP VIEWS)

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

181 16 ARITHMETIC OPERATIONS
16 LOGIC FUNCTIONS

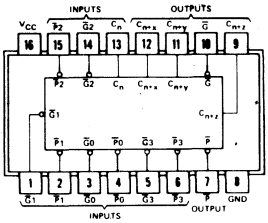


See page 7-260

SN54181 (J, W) SN74181 (J, N, NT)
SN54LS181 (J, W) SN74LS181 (J, N, NT)
SN54S181 (J, W) SN74S181 (J, N, NT)
SN54AS181 (J) SN74AS181 (N, NT)

LOOK-AHEAD CARRY GENERATORS

182

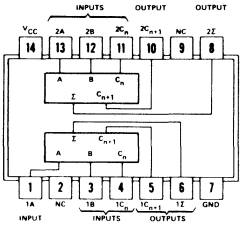


See page 7-271

SN54182 (J, W) SN74182 (J, N)
SN54S182 (J, W) SN74S182 (J, N)

DUAL CARRY-SAVE FULL ADDERS

183



See page 7-276

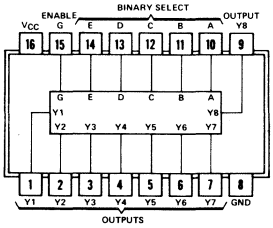
SN54LS183 (J, W) SN74LS183 (J, N)

CODE CONVERTERS

CASCADEABLE TO N-BITS

184 BCD-TO-BINARY

185 BINARY-TO-BCD



See page 7-279

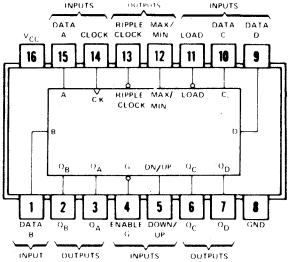
SN54184 (J, W) SN74184 (J, N)
SN54185A (J, W) SN74185A (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

SYNCHRONOUS UP/DOWN COUNTERS

190 BCD

191 BINARY



SN54190 (J, W)
SN54ALS190 (J, W)
SN54HC190 (J)
SN54LS190 (J, W)
SN54191 (J, W)
SN54ALS191 (J, W)
SN54HC191 (J)
SN54LS191 (J, W)

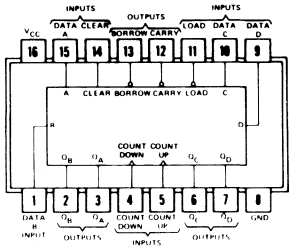
SN74190 (J, N)
SN74ALS190 (N)
SN74HC190 (N)
SN74LS190 (J, N)
SN74191 (J, N)
SN74ALS191 (N)
SN74HC191 (N)
SN74LS191 (J, N)

See page 7-285

SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

192 BCD WITH CLEAR

193 BINARY WITH CLEAR



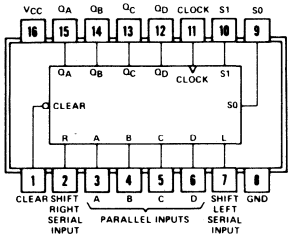
SN54192 (J, W)
SN54ALS192 (J, W)
SN54HC192 (J)
SN54LS192 (J, W)
SN54193 (J, W)
SN54ALS193 (J, W)
SN54HC193 (J)
SN54LS193 (J, W)

SN74192 (J, N)
SN74ALS192 (N)
SN74HC192 (N)
SN74LS192 (J, N)
SN74193 (J, N)
SN74ALS193 (N)
SN74HC193 (N)
SN74LS193 (J, N)

See page 7-295

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

194



SN54194 (J, W)
SN54AS194 (J)
SN54HC194 (J)
SN54LS194A (J, W)
SN54S194 (J, W)

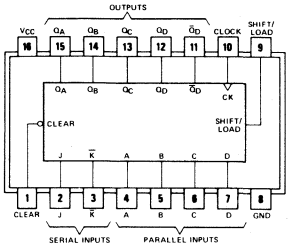
SN74194 (J, N)
SN74AS194 (N)
SN74HC194 (N)
SN74LS194A (J, N)
SN74S194 (J, N)

See page 7-304

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

195



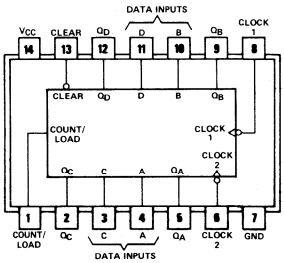
SN54195 (J, W) **SN74195 (J, N)**
SN54HC195 (J) **SN74HC195 (N)**
SN54LS195A (J, W) **SN74LS195A (J, N)**
SN54S195 (J, W) **SN74S195 (J, N)**

See page 7-312

PRESETABLE COUNTERS/LATCHES

196 DECADE/BI-QUINARY

197 BINARY

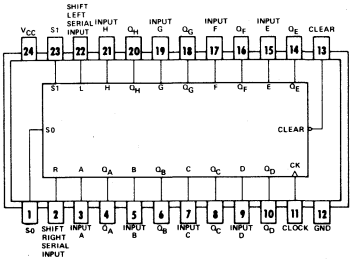


SN54196 (J, W) **SN74196 (J, N)**
SN54LS196 (J, W) **SN74LS196 (J, N)**
SN54S196 (J, W) **SN74S196 (J, N)**
SN54197 (J, W) **SN74197 (J, N)**
SN54LS197 (J, W) **SN74LS197 (J, N)**
SN54S197 (J, W) **SN74S197 (J, N)**

See page 7-319

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

198



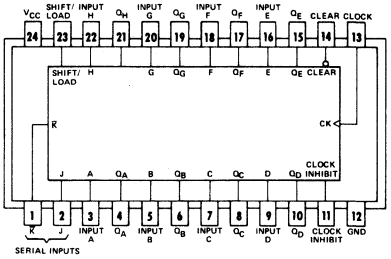
SN54198 (J, W) **SN74198 (J, N, NT)**

See page 7-326

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

199 J-$\overline{K}$ SERIAL INPUTS



SN54199 (J, W) SN74199 (J, N, NT)

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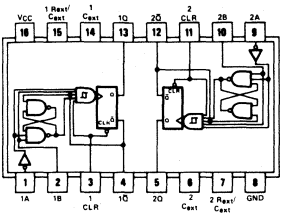
PIN ASSIGNMENTS (TOP VIEWS)

DUAL MONOSTABLE MULTIVIBRATORS

221

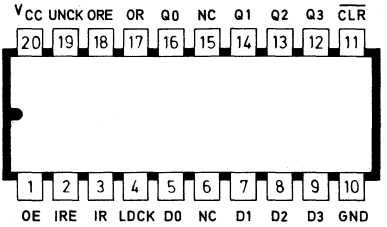


See page 6-77

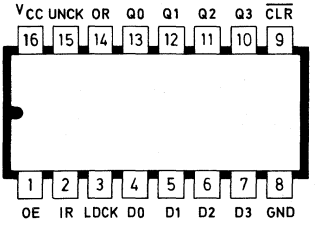
SN54221 (J, W) SN74221 (J, N)
SN54LS221 (J, W) SN74LS221 (J, N)

ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORIES

222
224
227
228



SN54LS222 (J) SN74LS222 (J, N)
SN54LS227 (J) SN74LS227 (J, N)



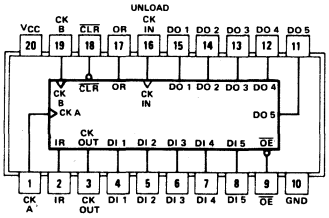
SN54LS224 (J) SN74LS224 (J, N)
SN54LS228 (J) SN74LS228 (J, N)

See page 7-333

PIN ASSIGNMENTS (TOP VIEWS)

ASYNCHRONOUS FIRST IN, FIRST OUT MEMORIES

225 16 5-BIT WORDS

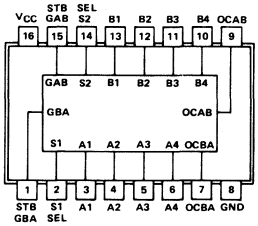


See page 7-341

SN74S225 (J, N)

4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

226 3-STATE OUTPUTS

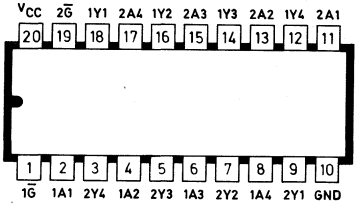


See page 7-347

SN54S226 (J, W) SN74S226 (J, N)

3-STATE OCTAL BUS DRIVER

230 TRUE AND INVERTING LOGIC

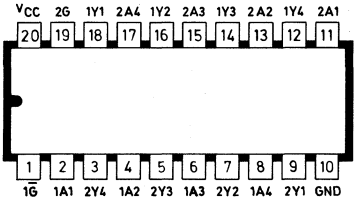


See Volume II

SN54AS230 (J) SN74AS230 (N)

3-STATE OCTAL BUS DRIVER

231 INVERTING LOGIC



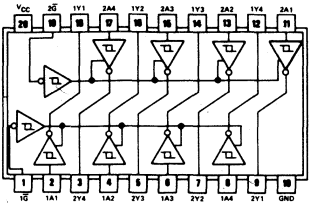
See Volume II

SN54AS231 (J) SN74AS231 (N)

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

240 INVERTED 3-STATE OUTPUTS



SN54ALS240 (J)
SN54AS240 (J)
SN54HC240 (J)
SN54LS240 (J)
SN54S240 (J)

SN74ALS240 (N)
SN74AS240 (N)
SN74HC240 (N)
SN74LS240 (J, N)
SN74S240 (J, N)

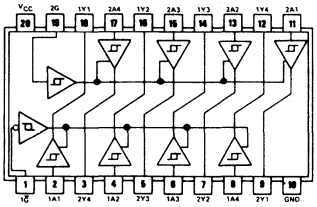
See page **7-351**

5

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

241 NONINVERTED 3-STATE OUTPUTS

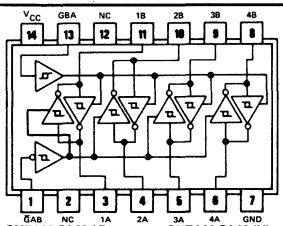


SN54ALS241 (J) SN74ALS241 (N)
SN54AS241 (J) SN74AS241 (N)
SN54HC241 (J) SN74HC241 (N)
SN54LS241 (J) SN74LS241 (J, N)
SN54S241 (J) SN74S241 (J, N)

See page 7-351

QUADRUPLE BUS TRANSCEIVERS

242 INVERTED 3-STATE OUTPUTS

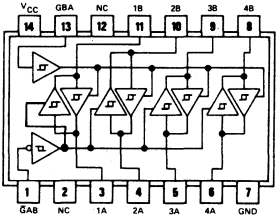


SN54ALS242 (J) SN74ALS242 (N)
SN54AS242 (J) SN74AS242 (N)
SN54HC242 (J) SN74HC242 (N)
SN54LS242 (J, W) SN74LS242 (J, N)
NC – No internal connection

See page 7-355

QUADRUPLE BUS TRANSCEIVERS

243 NONINVERTED 3-STATE OUTPUTS

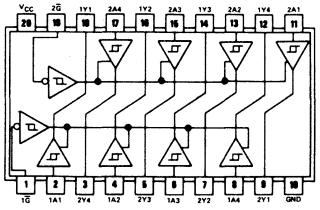


SN54ALS243 (J) SN74ALS243 (N)
SN54AS243 (J) SN74AS243 (N)
SN54HC243 (J) SN74HC243 (N)
SN54LS243 (J, W) SN74LS243 (J, N)
NC – No internal connection

See page 7-355

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

244 NONINVERTED 3-STATE OUTPUTS



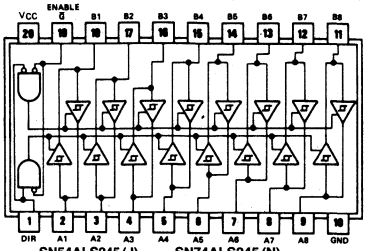
SN54ALS244 (J) SN74ALS244 (N)
SN54AS244 (J) SN74AS244 (N)
SN54HC244 (J) SN74HC244 (N)
SN54LS244 (J) SN74LS244 (J, N)
SN54S244 (J) SN74S244 (J, N)

See pages 7-351 and 7-357

PIN ASSIGNMENTS (TOP VIEW)

OCTAL BUS TRANCEIVERS

245 NONINVERTED 3-STATE OUTPUTS



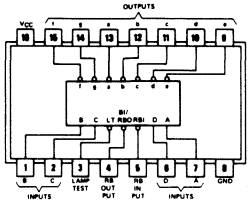
SN54ALS245 (J) SN74ALS245 (N)
SN54HC245 (J) SN74HC245 (N)
SN54LS245 (J) SN74LS245 (J, N)

See page 7-359

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

246 ACTIVE-LOW, OPEN-COLLECTOR, 30-V OUTPUTS

247 ACTIVE-LOW, OPEN-COLLECTOR, 15-V OUTPUTS



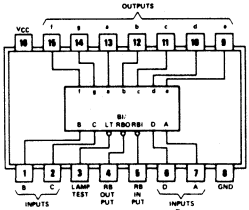
SN54246 (J, W) SN74246 (J, N)
SN54247 (J, W) SN74247 (J, N)
SN54LS247 (J, W) SN74LS247 (J, N)

See page 7-361

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

248 INTERNAL PULL-UP OUTPUTS

249 OPEN-COLLECTOR OUTPUTS

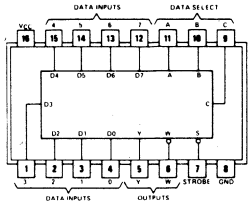


SN54248 (J, W) SN74248 (J, N)
SN54LS248 (J, W) SN74LS248 (J, N)
SN54249 (J, W) SN74249 (J, N)
SN54LS249 (J, W) SN74LS249 (J, N)

See page 7-361

DATA SELECTORS/MULTIPLEXERS

251 TRUE AND INVERTED 3-STATE OUTPUTS



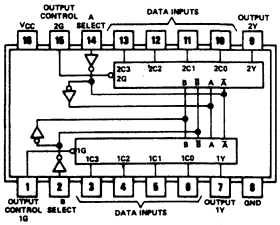
SN54251 (J, W) SN74251 (J, N)
SN54ALS251 (J) SN74ALS251 (N)
SN54AS251 (J) SN74AS251 (N)
SN54HC251 (J) SN74HC251 (N)
SN54LS251 (J, W) SN74LS251 (J, N)
SN54S251 (J, W) SN74S251 (J, N)

See page 7-372

PIN ASSIGNMENTS (TOP VIEWS)

DUAL DATA SELECTORS/MULTIPLEXERS

253 3-STATE OUTPUTS

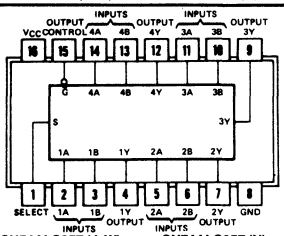


See page 7-379

SN54ALS253 (J) SN74ALS253 (N)
SN54AS253 (J) SN74AS253 (N)
SN54HC253 (J) SN74HC253 (N)
SN54LS253 (J, W) SN74LS253 (N)

QUAD DATA SELECTORS/MULTIPLEXERS

257 NONINVERTED 3-STATE OUTPUTS

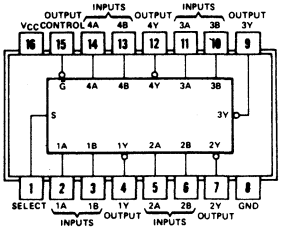


See page 7-382

SN54ALS257 (J, W) SN74ALS257 (N)
SN54AS257 (J) SN74AS257 (N)
SN54HC257 (J) SN74HC257 (N)
SN54LS257B (J, W) SN74LS257B (J, N)
SN54S257 (J, W) SN74S257 (J, N)

QUAD DATA SELECTORS/MULTIPLEXERS

258 INVERTED 3-STATE OUTPUTS

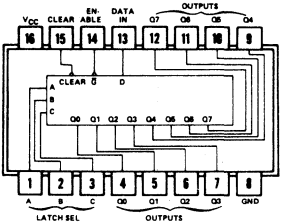


See page 7-382

SN54ALS258 (J, W) SN74ALS258 (N)
SN54AS258 (J) SN74AS258 (N)
SN54HC258 (J) SN74HC258 (N)
SN54LS258B (J, W) SN74LS258B (J, N)
SN54S258 (J, W) SN74S258 (J, N)

EIGHT-BIT ADDRESSABLE LATCHES

259



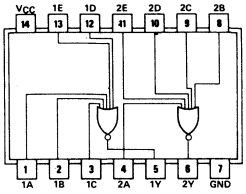
See page 7-386

SN54259 (J, W) SN74259 (J, N)
SN54ALS259 (J) SN74ALS259 (N)
SN54HC259 (J) SN74HC259 (N)
SN54LS259 (J, W) SN74LS259 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

DUAL 5-INPUT POSITIVE NOR GATES

260

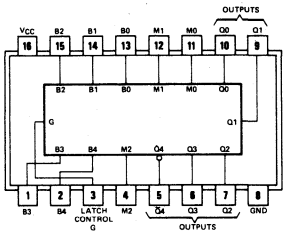


See page 6-8

SN54S260 (J, W) SN74S260 (J, N)

2-BIT BY 4-BIT PARALLEL BINARY MULTIPLIERS

261

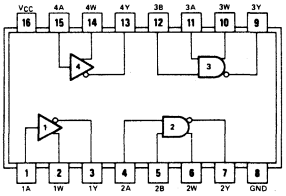


See page 7-390

SN54LS261 (J, W) SN74LS261 (J, N)

QUAD COMPLEMENTARY-OUTPUT ELEMENTS

265



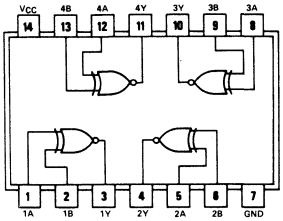
See page 6-91

SN54265 (J, W) SN74265 (J, N)

QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

266

positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$



See page 7-396

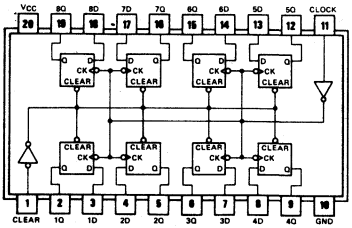
SN54HC266 (J) SN74HC266 (N)
SN54LS266 (J, W) SN74LS266 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE FLIP-FLOPS

273 COMMON CLOCK
SINGLE-RAIL OUTPUTS

See page 7-398



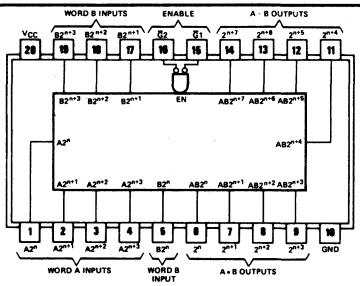
SN54273 (J)
SN54ALS273 (J)
SN54HC273 (J)
SN54LS273 (J)

SN74273 (J, N)
SN74ALS273 (N)
SN74HC273 (N)
SN74LS273 (J, N)

4-BIT BY 4-BIT BINARY MULTIPLIERS

274 3-STATE OUTPUTS
8-BIT PRODUCTS
SUB-MULTIPLE PRODUCTS

See page 7-401



SN54S274 (J)

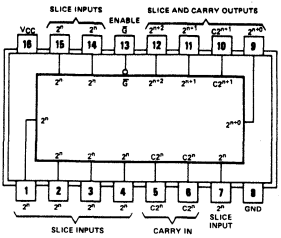
SN74S274 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

7-BIT SLICE WALLACE TREES

275 3-STATE OUTPUTS

See page 7-401

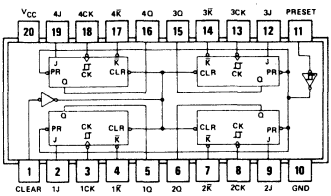


SN54LS275 (J) SN74LS275 (J, N)
SN54S275 (J) SN74S275 (J, N)

QUAD J-$\overline{K}$ FLIP-FLOPS

276 SEPARATE CLOCKS
EDGE-TRIGGERING
COMMON DIRECT CLEAR AND PRESET

See page 7-411

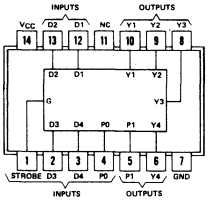


SN54276 (J) SN74276 (J, N)

4-BIT CASCADEABLE PRIORITY REGISTERS

278 LATCHED DATA INPUTS
PRIORITY OUTPUT GATING

See page 7-413



SN54278 (J, W) SN74278 (J, N)
NC — No internal connection

QUAD $\overline{S}$-$\overline{R}$ LATCHES

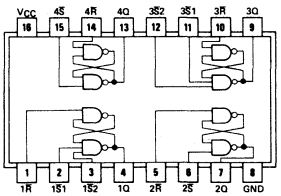
279 DIODE-CLAMPED INPUTS
TOTEM-POLE OUTPUTS

FUNCTION TABLE

INPUTS $\overline{S}$	INPUTS $\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

See page 6-58



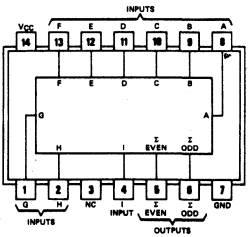
SN54279 (J, W) SN74279 (J, N)
SN54LS279A (J, W) SN74LS279A (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

280 N-BIT CASCADEABLE

See page 7-416

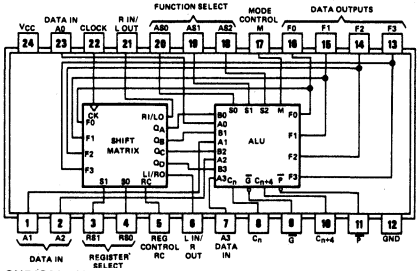


SN54AS280 (J)
SN54HC280 (J)
SN54LS280 (J, W)
SN54S280 (J, W)
SN74AS280 (N)
SN74HC280 (N)
SN74LS280 (J, N)
SN74S280 (J, N)

4-BIT PARALLEL BINARY ACCUMULATORS

281 15 ARITHMETIC/
LOGIC-TYPE OPERATIONS
LOGIC SHIFT (L OR R)
EXPANDABLE TO N WORDS

See page 7-420

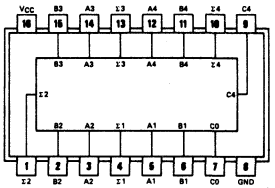


SN54S281 (J, W)
SN74S281 (J, N, NT)

4-BIT BINARY FULL ADDERS

283

See page 7-425



SN54283 (J, W)
SN54HC283 (J)
SN54LS283 (J, W)
SN54S283 (J)
SN74283 (J, N)
SN74HC283 (N)
SN74LS283 (J, N)
SN74S283 (J, N)

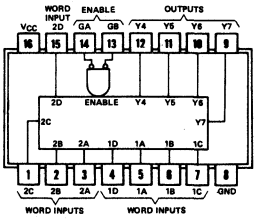
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '285

284 EXPANDABLE FOR N-BIT-
BY-N-BIT MULTIPLICATION

USE 'S274 FOR NEW DESIGNS

USE 'LS275/'S275 FOR LARGE MULTIPLIERS

See page 7-430



SN54284 (J, W)
SN74284 (J, N)

PIN ASSIGNMENTS (TOP VIEW)

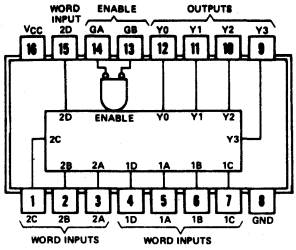
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS USED WITH '284

285 EXPANDABLE FOR N-BIT-BY-N-BIT MULTIPLICATION

USE 'S274 FOR NEW DESIGNS

USE 'LS275/'S275 FOR LARGE MULTIPLIERS

See page 7-430



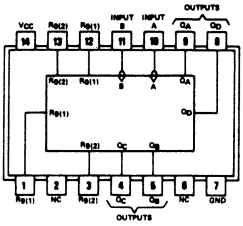
SN54285 (J, W) **SN74285 (J, N)**

PIN ASSIGNMENTS (TOP VIEWS)

DECADE COUNTERS

290 DIVIDE-BY-TWO AND DIVIDE-BY-5

See page 7-433



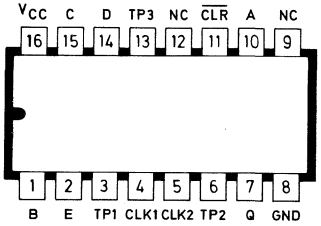
SN54290 (J, W) SN74290 (J, N)
SN54LS290 (J, W) SN74LS290 (J, N)

PROGRAMMABLE FREQUENCY DIVIDER / DIGITAL TIMER

292

DIGITALLY PROGRAMMABLE FROM 2^2 TO 2^{31}

See page 7-439

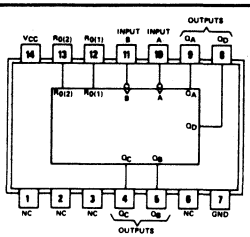


SN54LS292 (J or W) SN74LS292 (J or N)

4-BIT BINARY COUNTERS

293 DIVIDE-BY-TWO AND DIVIDE-BY-EIGHT

See page 7-433



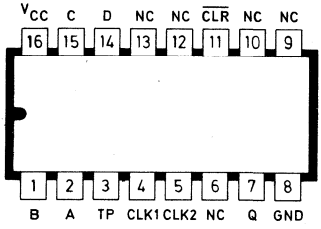
SN54293 (J, W) SN74293 (J, N)
SN54LS293 (J, W) SN74LS293 (J, N)

PROGRAMMABELE FREQUENCY DIVIDER / DIGITAL TIMER

294

DIGITALLY PROGRAMMABLE FROM 2^2 TO 2^{15}

See page 7-439



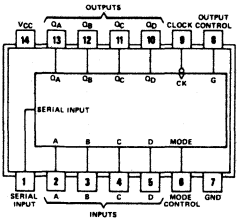
SN74LS294 (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

295

See page 7-446



SN54LS295B (J, W) SN74LS295B (J, N)

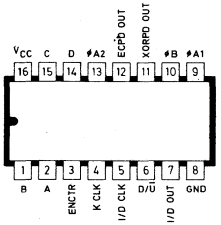
DIGITAL PHASE LOCKED LOOP FILTER

297

logic: see description

See page 7-449

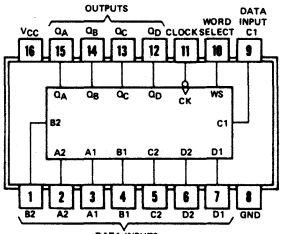
SN54LS297 (J or W) SN74LS297 (J or N)



QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

298

See page 7-455



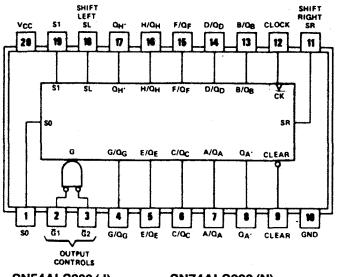
SN54298 (J, W)
SN54AS298 (J)
SN54HC298 (J)
SN54LS298 (J, W)

SN74298 (J, N)
SN74AS298 (N)
SN74HC298 (N)
SN74LS298 (J, N)

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

299 3-STATE OUTPUTS

See page 7-460



SN54ALS299 (J)
SN54HC299 (J)
SN54LS299 (J)
SN54S299 (J)

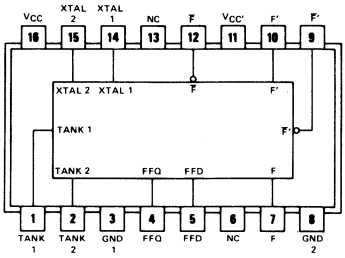
SN74ALS299 (N)
SN74HC299 (N)
SN74LS299 (J, N)
SN74S299 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

CRYSTAL CONTROLLED OSCILLATOR

320

logic: see description



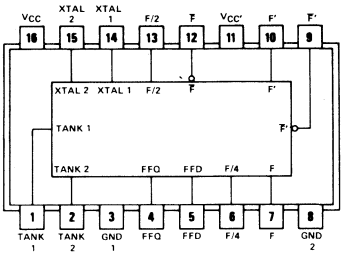
SN54LS320 (J) SN74LS320 (J or N)

See page 7-466

CRYSTAL CONTROLLED OSCILLATOR

321

logic: see description



SN54LS321 (J) SN74LS321 (J or N)

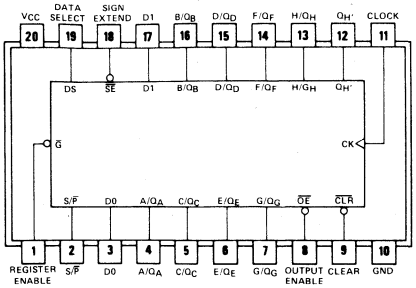
See page 7-466

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT SHIFT REGISTER WITH SIGN EXTEND

322

logic: see description and function table

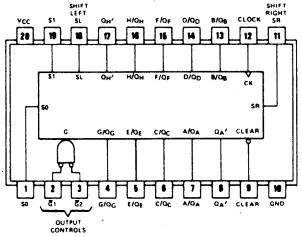


SN54HC322 (J) **SN74HC322 (N)**
SN54LS322A (J) **SN74LS322A (J or N)**

See page 7-469

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

323 3-STATE OUTPUTS



SN54ALS323 (J) **SN74ALS323 (N)**
SN54HC323 (J) **SN74HC323 (N)**
SN54LS323 (J) **SN74LS323 (J, N)**

See page 7-473

PIN ASSIGNMENTS (TOP VIEWS)

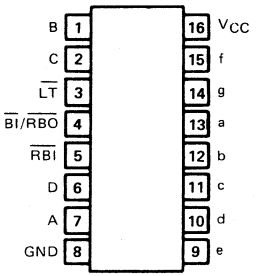
BCD-TO-SEVEN-SEGMENT DECODERS / DRIVERS

347

logic: see function table

See page 7-475

(TOP VIEW)

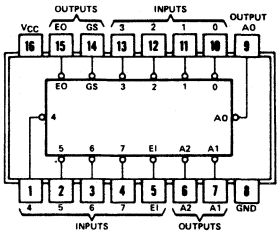


SN54LS347 (J or W)
SN74LS347 (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

8-LINE TO 3-LINE PRIORITY ENCODERS

348 3-STATE OUTPUTS

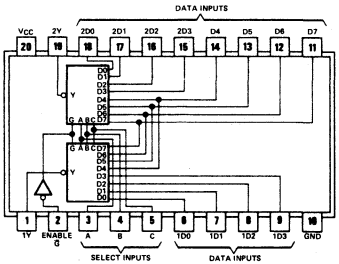


See page 7-477

SN54LS348 (J, W) SN74LS348 (J, N)

DUAL 8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

351 3-STATE OUTPUTS
4 COMMON DATA INPUTS

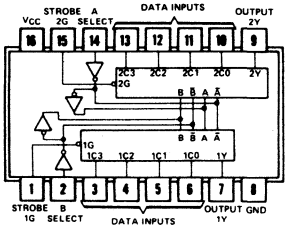


See page 7-480

SN74351 (N)

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

352 INVERTING VERSION OF 'LS153

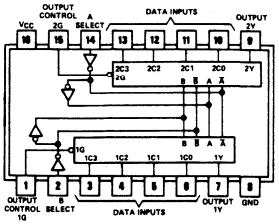


SN54ALS352 (J) SN74ALS352 (N)
SN54AS352 (J) SN74AS352 (N)
SN54HC352 (J) SN74HC352 (N)
SN54LS352 (J, W) SN74LS352 (J, N)

See page 7-483

DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

353 3-STATE OUTPUTS
INVERTING VERSION OF 'LS253



SN54ALS353 (J) SN74ALS353 (N)
SN54AS353 (J) SN74AS353 (N)
SN54HC353 (J) SN74HC353 (N)
SN54LS353 (J, W) SN74LS353 (J, N)

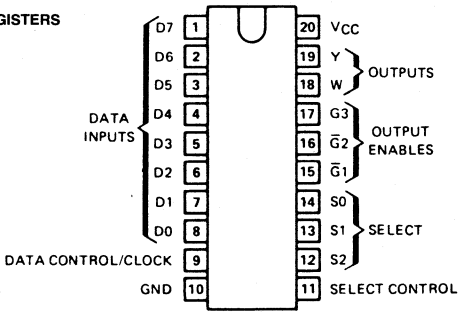
See page 7-486

PIN ASSIGNMENTS (TOP VIEWS)

8-LINE TO 1-LINE DATA SELECTORS / MULTIPLEXERS / REGISTERS

354
355
356
357

OUTPUTS: 3-STATE (LS354, LS356, HC354, HC356)
OPEN COLLECTOR (LS355, LS357)
DATA REGISTERS: TRANSPARENT (LS354, LS355, HC354)
EDGE TRIGGERED (LS356, LS357, HC356)

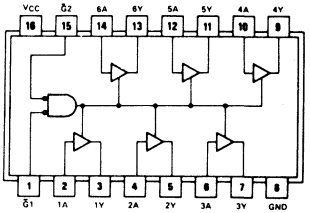


SN54LS' (J) **SN74LS' (J, N)**
SN54HC354 (J) **SN74HC354 (N)**
SN54HC356 (J) **SN74HC356 (N)**

See page 7-489

HEX BUS DRIVERS

365 NONINVERTED 3-STATE OUTPUTS
GATED ENABLE INPUTS

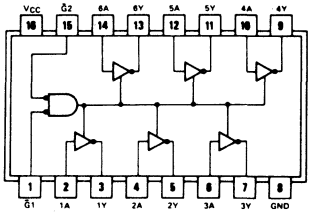


SN54365A (J, W) **SN74365A (J, N)**
SN54HC365 (J) **SN74HC365 (N)**
SN54LS365A (J, W) **SN74LS365A (J, N)**

See page 6-36

HEX BUS DRIVERS

366 INVERTED 3-STATE OUTPUTS
GATED ENABLE INPUTS



SN54366A (J, W) **SN74366A (J, N)**
SN54HC366 (J) **SN74HC366 (N)**
SN54LS366A (J, W) **SN74LS366A (J, N)**

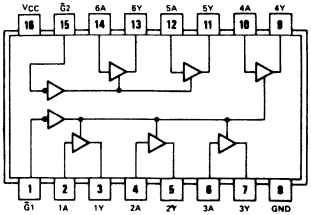
See page 6-36

PIN ASSIGNMENTS (TOP VIEWS)

HEX BUS DRIVERS

367 NONINVERTED 3-STATE OUTPUTS ORGANIZED TO FACILITATE HANDLING OF 4-BIT DATA

See page 6-36



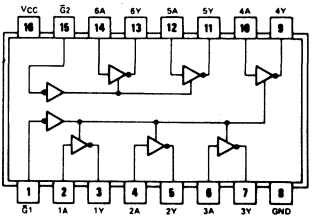
SN54367A (J, W)
SN54HC367 (J)
SN54LS367A (J, W)

SN74367A (J, N)
SN74HC367 (N)
SN74LS367A (J, N)

HEX BUS DRIVERS

368 INVERTED 3-STATE OUTPUTS ORGANIZED TO FACILITATE HANDLING OF 4-BIT DATA

See page 6-36



SN54368A (J, W)
SN54HC368 (J)
SN54LS368A (J, W)

SN74368A (J, N)
SN74HC368 (N)
SN74LS368A (J, N)

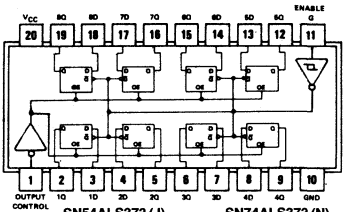
5

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE LATCHES

373 3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON ENABLE

See page 7-496



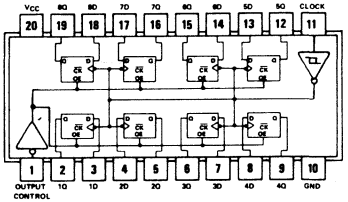
SN54ALS373 (J)
SN54AS373 (J)
SN54HC373 (J)
SN54LS373 (J)
SN54S373 (J)

SN74ALS373 (N)
SN74AS373 (N)
SN74HC373 (N)
SN74LS373 (J, N)
SN74S373 (J, N)

OCTAL D-TYPE FLIP-FLOPS

374 3-STATE OUTPUTS
COMMON OUTPUT CONTROL
COMMON CLOCK

See page 7-496



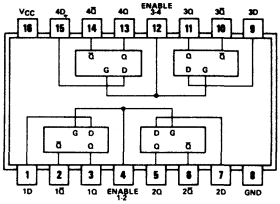
SN54ALS374 (J)
SN54AS374 (J)
SN54HC374 (J)
SN54LS374 (J)
SN54S374 (J)

SN74ALS374 (N)
SN74AS374 (N)
SN74HC374 (N)
SN74LS374 (J, N)
SN74S374 (J, N)

4-BIT BISTABLE LATCHES

375

See page 7-503



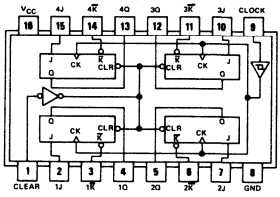
SN54HC375 (J)
SN54LS375 (J, W)

SN74HC375 (N)
SN74LS375 (J, N)

QUAD J-$\overline{K}$ FLIP-FLOPS

376 COMMON CLOCK
COMMON CLEAR

See page 7-504



SN54376 (J, W)

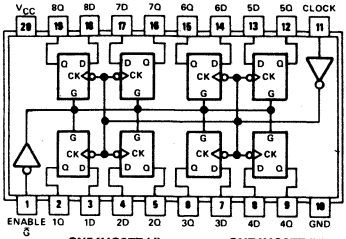
SN74376 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE FLIP-FLOPS

377 SINGLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK

See page 7-506



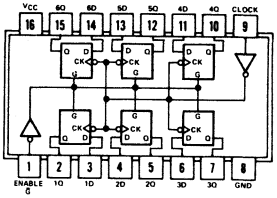
SN54HC377 (J)
SN54LS377 (J)

SN74HC377 (N)
SN74LS377 (J, N)

HEX D-TYPE FLIP-FLOPS

378 SINGLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK

See page 7-506



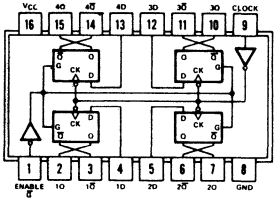
SN54HC378 (J)
SN54LS378 (J, W)

SN74HC378 (N)
SN74LS378 (J, N)

QUAD D-TYPE FLIP-FLOPS

379 DOUBLE-RAIL OUTPUTS
COMMON ENABLE
COMMON CLOCK

See page 7-506



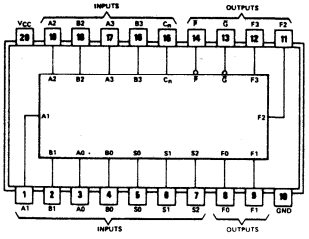
SN54HC379 (J)
SN54LS379 (J, W)

SN74HC379 (N)
SN74LS379 (J, N)

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

381 8 BINARY FUNCTIONS
USE 'S182 FOR LOOK-AHEAD CARRY

See page 7-509



SN54LS381A (J)
SN54S381 (J)

SN74LS381A (J, N)
SN74S381 (J, N)

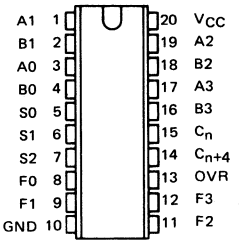
PIN ASSIGNMENTS (TOP VIEWS)

ARITHMETIC LOGIC UNITS / FUNCTION GENERATORS

382

logic: see function table

See page 7-509



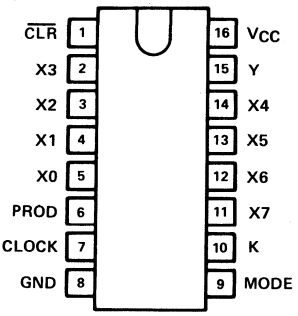
SN54LS382 (J) **SN74LS382 (J or N)**

8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

384

logic: see function table

See page 7-518



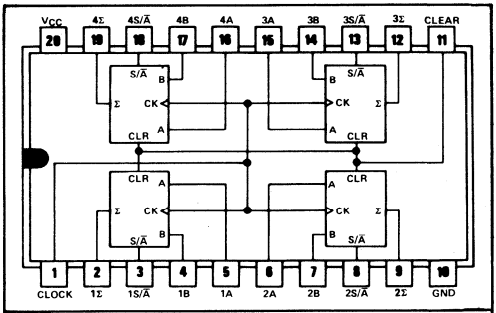
SN54LS384 (J or W) **SN74LS384 (J or N)**

QUADRUPLE SERIAL ADDERS / SUBSTRACTORS

385

positive logic: see function table

See page 7-522



positive logic: see function table

SN54LS385 (J) **SN74LS385 (J or N)**

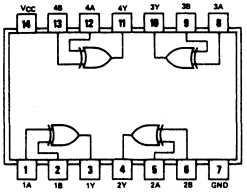
PIN ASSIGNMENTS (TOP VIEWS)

QUAD 2-INPUT EXCLUSIVE-OR GATES

386

POSITIVE LOGIC:
$Y = A \oplus B = \overline{A}B + A\overline{B}$

See page 7-524

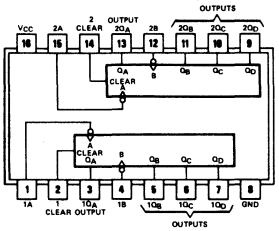


SN54HC386 (J)
SN54LS386A (J, W)
SN74HC386 (N)
SN74LS386A (J, N)

DUAL DECADE COUNTERS

390 BI-QUINARY OR BCD SEQUENCES

See page 7-526

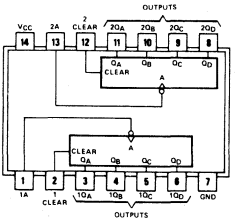


SN54390 (J, W)
SN54HC390 (J)
SN54LS390 (J, W)
SN74390 (J, N)
SN74HC390 (N)
SN74LS390 (J, N)

DUAL 4-BIT BINARY COUNTERS

393

See page 7-526



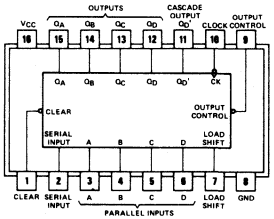
SN54393 (J, W)
SN54HC393 (J)
SN54LS393 (J, W)
SN74393 (J, N)
SN74HC393 (N)
SN74LS393 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT UNIVERSAL SHIFT REGISTERS

395 3-STATE OUTPUTS

See page 7-533



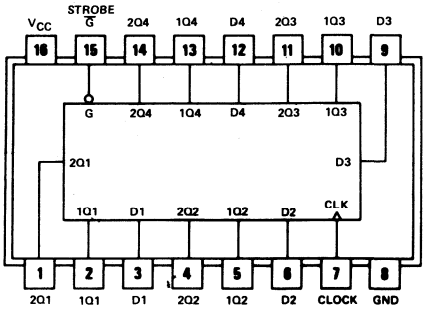
SN54LS395A (J, W) SN74LS395A (J, N)
SN54AS395 (J) SN74AS395 (N)

OCTAL STORAGE REGISTERS

396

logic: see function table

See page 7-536

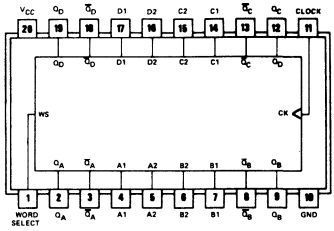


SN54LS396 (J or W) SN74LS369 (J or N)

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

398 DOUBLE-RAIL OUTPUTS

See page 7-538

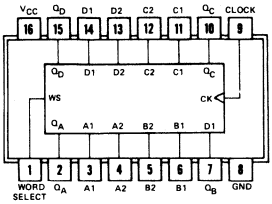


SN54LS398 (J) SN74LS398 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

399 SINGLE-RAIL OUTPUTS

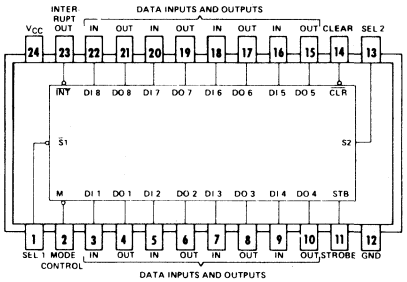


See page 7-538

SN54LS399 (J,W) SN74LS399 (J, N)

MULTI-MODE BUFFERED 8-BIT LATCHES

412 3-STATE OUTPUTS
DIRECT CLEAR

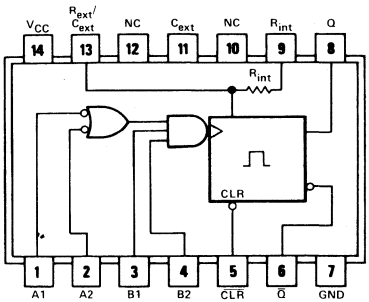


See page 7-541

SN54S412 (J) SN74S412 (J, N)

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

422



logic: see function table

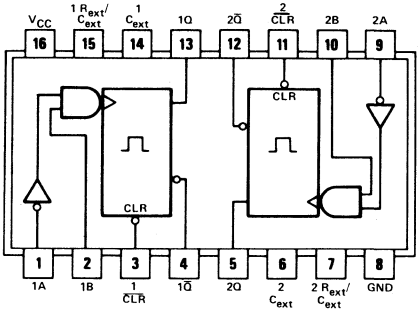
See page 7-546

SN54LS422 (J or W) SN74LS422 (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

423



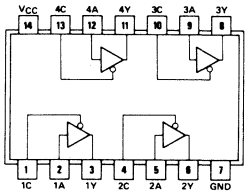
logic: see function table

See page 7-546

SN54LS423 (J or W) **SN74LS423 (J or N)**

QUAD GATES

425 3-STATE OUTPUTS
ACTIVE-LOW ENABLING



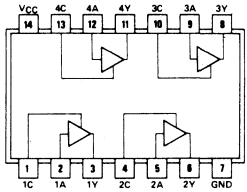
positive logic: Y = A

SN54425 (J, W) **SN74425 (J, N)**

See page 6-33

QUAD GATES

426 3-STATE OUTPUTS
ACTIVE-HIGH ENABLING



positive logic: Y = A

SN54426 (J, W) **SN74426 (J, N)**

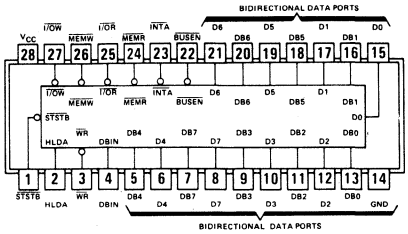
See page 6-33

PIN ASSIGNMENTS (TOP VIEWS)

SYSTEM CONTROLLER FOR 8080A

428 BIDIRECTIONAL DATA PORTS

438 BIDIRECTIONAL DATA PORTS

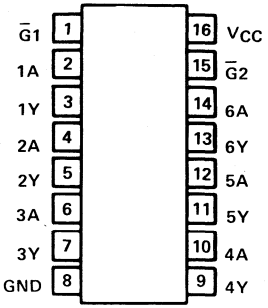


See page 7-550

SN74S428 (N)
SN74S438 (N)

LINE DRIVER / MEMORY DRIVER CIRCUITS

436
437



See page 7-556

SN54S436 (J, W)
SN54S437 (J, W)

SN74S436 (J, N)
SN74S437 (J, N)

QUAD TRIDIRECTIONAL BUS TRANSCEIVERS

440 OPEN-COLLECTOR NONINVERTED OUTPUTS

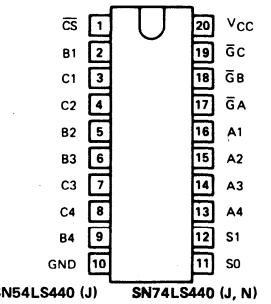
441 OPEN-COLLECTOR INVERTED OUTPUTS

442 3-STATE NONINVERTED OUTPUTS

443 3-STATE INVERTED OUTPUTS

444 3-STATE INVERTED AND NONINVERTED OUTPUTS

448 OPEN-COLLECTOR INVERTED AND NONINVERTED OUTPUTS



See page 7-560

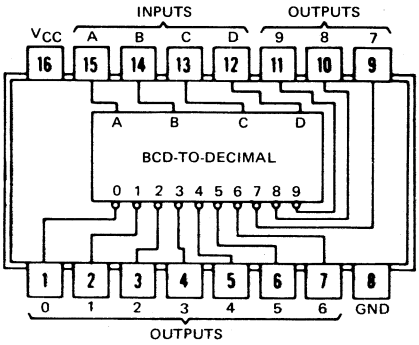
SN54LS440 (J)
SN54LS441 (J)
SN54LS442 (J)
SN54LS443 (J)
SN54LS444 (J)
SN54LS448 (J)

SN74LS440 (J, N)
SN74LS441 (J, N)
SN74LS442 (J, N)
SN74LS443 (J, N)
SN74LS444 (J, N)
SN74LS448 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

BCD-TO-DECIMAL DECODER / DRIVER

445

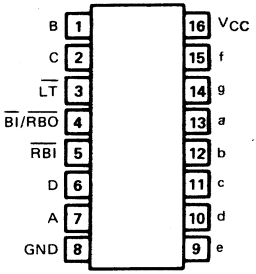


See page 7-566

SN54LS445 (J or W) SN74LS445 (J or N)

BCD-TO-SEVEN SEGMENT DECODER/DRIVER

447



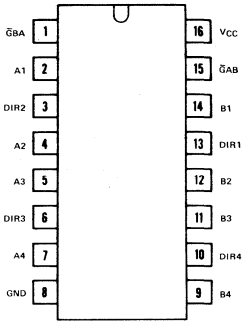
See page 7-572

SN54LS447 (J or W) SN74LS447 (J or N)

QUADRUPLE BUS TRANCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

446 INVERTING LOGIC

449 TRUE LOGIC



See page 7-568

SN54LS' (J) SN74LS' (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

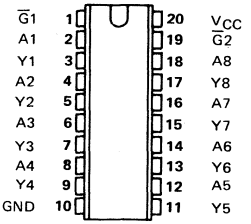
OCTAL BUFFERS WITH 3-STATE OUTPUTS

465 TRUE LOGIC

466 INVERTING LOGIC

2-input active low AND enable gate controls all 8 buffers

See page 7-574



SN54LS' (J)
SN54ALS' (J)

SN74LS' (J or N)
SN74ALS' (N)

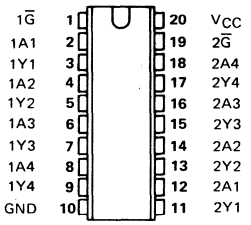
OCTAL BUFFERS WITH 3-STATE OUTPUTS

467 TRUE LOGIC

468 INVERTING LOGIC

2 separate active low enable inputs each control four buffers

See page 7-574



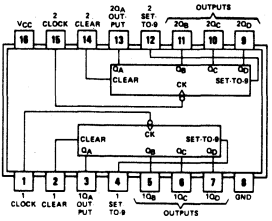
SN54LS' (J)
SN54ALS' (J)

SN74LS' (J or N)
SN74ALS' (N)

PIN ASSIGNMENTS (TOP VIEWS)

DUAL DECADE COUNTERS

490

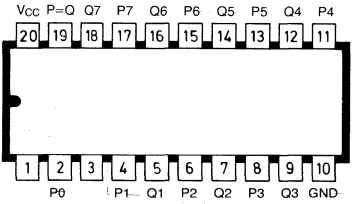


SN54490 (J, W) **SN74490 (J, N)**
SN54HC490 (J) **SN74HC490 (N)**
SN54LS490 (J, W) **SN74LS490 (J, N)**

See page 7-577

OCTAL COMPARATOR

518



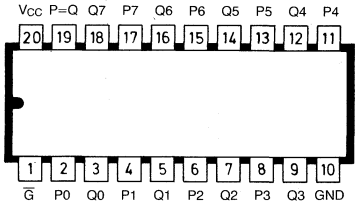
SN54ALS518 (J, W) **SN74ALS518 (N)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL COMPARATOR

519

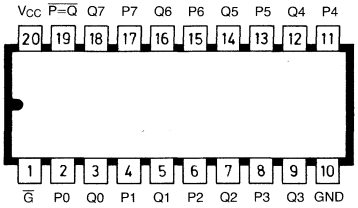


SN54ALS519 (J, W) **SN74ALS519 (N)**

See volume II

OCTAL COMPARATOR

520

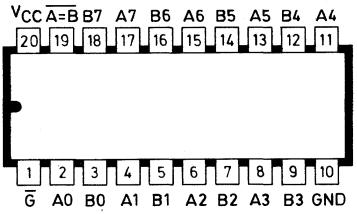


SN54ALS520 (J, W) **SN74ALS520 (N)**

See volume II

OCTAL COMPARATOR

521

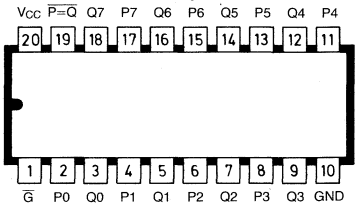


SN54ALS521 (J, W) **SN74ALS521 (N)**
SN54HC521 (J) **SN74HC521 (N)**

See volume II

OCTAL COMPARATOR

522



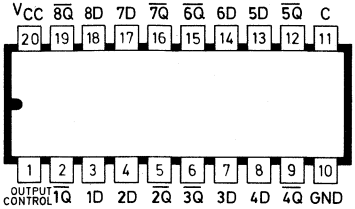
SN54ALS522 (J, W) **SN74ALS522 (N)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE LATCHES – INVERTING

533 (INVERTED 373)

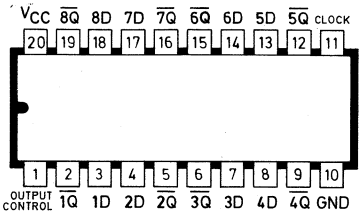


SN54ALS533 (J, W) **SN74ALS533 (N)**
SN54AS533 (J) **SN74AS533 (N)**
SN54HC533 (J) **SN74HC533 (N)**

See volume II

OCTAL D-TYPE FLIP FLOPS – INVERTING

534 (INVERTED 374)



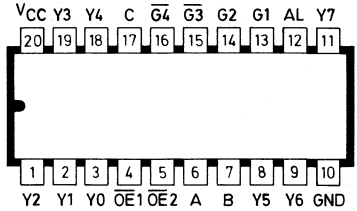
SN54ALS534 (J, W) **SN74ALS534 (N)**
SN54AS534 (J) **SN74AS534 (N)**
SN54HC534 (J) **SN74HC534 (N)**

See volume II

I-OF-8 LINE DECODERS

538

3-State Outputs
Output polarity control
Multiple enables for expansion.
Data Demultiplexing Capability



SN54ALS538 (J) **SN74ALS538 (N)**

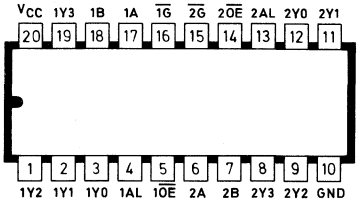
See volume II

PIN ASSIGNMENTS (TOP VIEWS)

DUAL I-OF-4 LINE DECODERS

539 3-State Outputs

Output polarity control
Data multiplexing capability

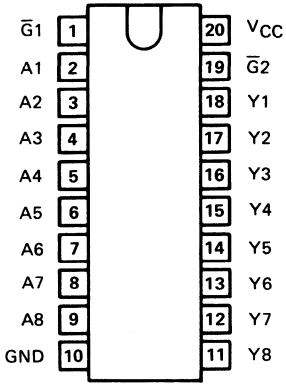


See volume II

SN54ALS539 (J) **SN74ALS539 (N)**

OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

540 INVERTING DATA
541 TRUE DATA



SN54ALS' (J)
SN54HC' (J)
SN54LS' (J)

SN74ALS' (N)
SN74HC' (N)
SN74LS' (J or N)

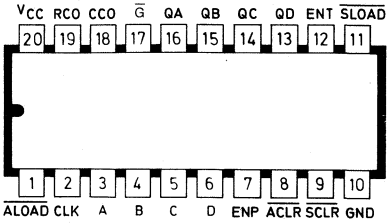
See page 7-583

PIN ASSIGNMENTS (TOP VIEWS)

SYNCHRONOUS 4-BIT COUNTERS WITH 3-STATE OUTPUTS

560 DECADE COUNTER

561 BINARY COUNTER

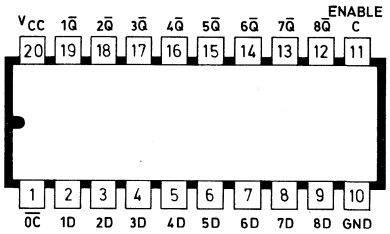


SN54ALS560 (J) **SN74ALS560 (N)**
SN54ALS561 (J) **SN74ALS561 (N)**

See volume II

OCTAL TRANSPARENT LATCHES WITH INVERTED OUTPUTS

563

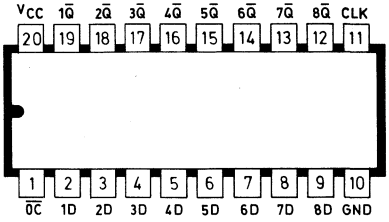


SN54ALS563 (J) **SN74ALS563 (N)**
SN54HC563 (J) **SN74HC563 (N)**

See volume II

OCTAL EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

564



SN54ALS564 (J) **SN74ALS564 (N)**
SN54HC564 (J) **SN74HC564 (N)**

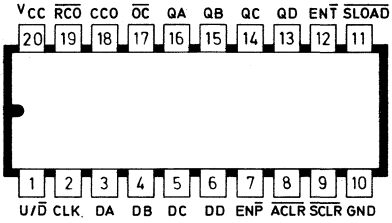
See volume II

PIN ASSIGNMENTS (TOP VIEWS)

SYNCHRONOUS UP-DOWN COUNTERS WITH 3-STATE OUTPUTS

568 DECADE COUNTER

569 BINARY COUNTER

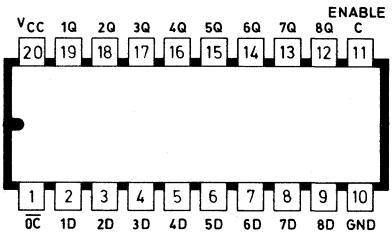


SN54ALS568 (J) **SN74ALS568 (N)**
SN54ALS569 (J) **SN74ALS569 (N)**

See volume II

OCTAL D-TYPE TRANSPARENT LATCHES

573

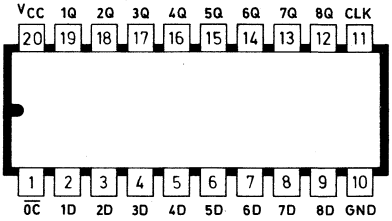


SN54ALS573 (J) **SN74ALS573 (N)**
SN54AS573 (J) **SN74AS573 (N)**
SN54HC573 (J) **SN74HC573 (N)**

See volume II

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

574



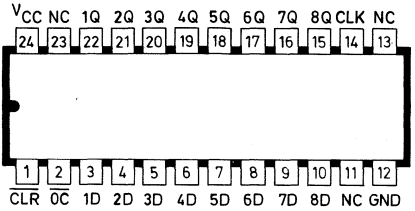
SN54ALS574 (J) **SN74ALS574 (N)**
SN54AS574 (J) **SN74AS574 (N)**
SN54HC574 (J) **SN74HC574 (N)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE FLIP FLOPS

575 TRUE LOGIC

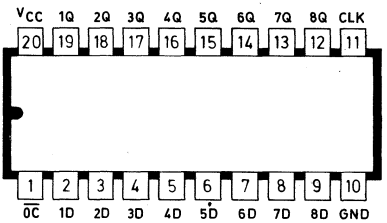


SN54ALS575 (JT) **SN74ALS575 (NT)**
SN54AS575 (JT) **SN74AS575 (NT)**

See volume II

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH INVERTED OUTPUTS

576 INVERTING 574

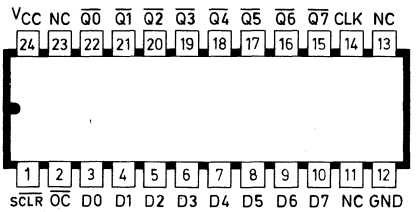


SN54ALS576 (J) **SN74ALS576 (N)**
SN54AS576 (J) **SN74AS576 (N)**

See volume II

OCTAL D-TYPE FLIP FLOPS WITH SYNCHRONOUS CLEAR

577 INVERTING LOGIC



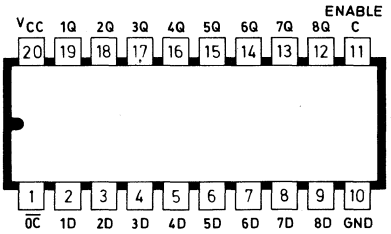
SN54ALS577 (JT) **SN74ALS577 (NT)**
SN54AS577 (JT) **SN74AS577 (NT)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

580 INVERTING 580



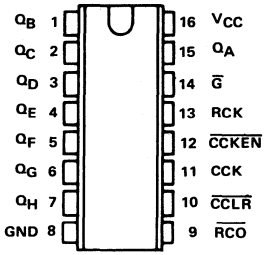
SN54ALS580 (J) SN74ALS580 (N)
SN54AS580 (J) SN74AS580 (N)

See volume II

8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

590 3 STATE OUTPUTS

591 OPEN COLLECTOR OUTPUTS

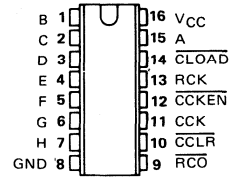


See page 7-586

SN54HC' (J) SN74HC' (N)
SN54LS' (J or W) SN74LS' (J or N)

8-BIT BINARY COUNTERS WITH INPUT REGISTERS

592 PARALLEL REGISTER INPUTS



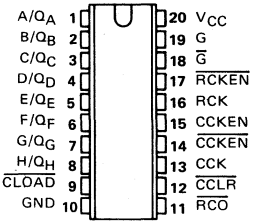
See page 7-590

SN54HC592 (J) SN74HC592 (N)
SN54LS592 (J or W) SN74LS592 (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT BINARY COUNTERS WITH INPUT REGISTER AND 3-STATE I/O

593



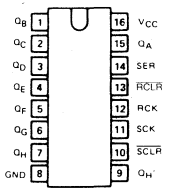
See page 7-590

SN54HC593 (J) SN74HC593 (N)
SN54LS593 (J) SN74LS593 (J or N)

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTER

594 TOTEM POLE OUTPUTS

599 OPEN COLLECTOR OUTPUTS



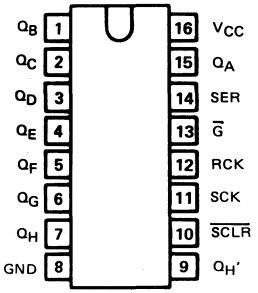
See page 7-595

SN54HC594 (J) SN74HC594 (N)
SN54LS' (J) SN74LS' (N)

8-BIT SHIFT REGISTERS WITH OUTPUT REGISTER

595 3-STATE OUTPUTS

596 OPEN COLLECTOR OUTPUTS

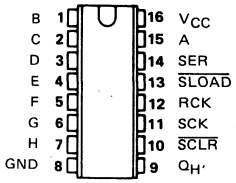


See page 7-599

SN54LS' (J or W) SN74LS' (J or N)
SN54HC595 (J) SN74HC595 (N)

8-BIT SHIFT REGISTERS WITH INPUT REGISTER

597 8 BIT PARALLEL STORAGE REGISTER INPUTS



See page 7-603

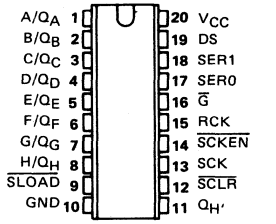
SN54HC597 (J) SN74HC597 (N)
SN54LS597 (J or W) SN74LS597 (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT SHIFT REGISTERS WITH INPUT REGISTER

598 PARALLEL 3-STATE I/O
STORAGE REGISTER INPUTS
SHIFT REGISTER OUTPUTS

See page 7-603



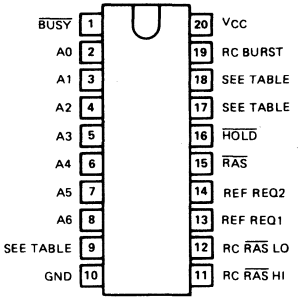
SN54HC598 (J)
SN54LS598 (J)

SN74HC598 (N)
SN74LS598 (J or N)

MEMORY REFRESH CONTROLLERS

600 TRANSPARENT, BURST 4K or 16K
601 TRANSPARENT, BURST 64K
602 CYCLE STEAL, BURST 4K or 16K
603 CYCLE STEAL, BURST 64K

See page 7-608



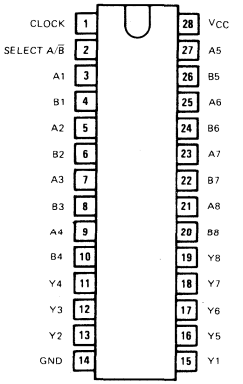
SN54LS' (J)

SN74LS' (J or N)

OCTAL 2-INPUT MULTIPLEXED LATCHES

604 3-STATE OUTPUTS – MAXIMUM SPEED
605 OPEN COLLECTOR O/P – MAXIMUM SPEED
606 3-STATE OUTPUTS – GLITCH FREE
607 OPEN COLLECTOR O/P – GLITCH FREE

See page 7-613



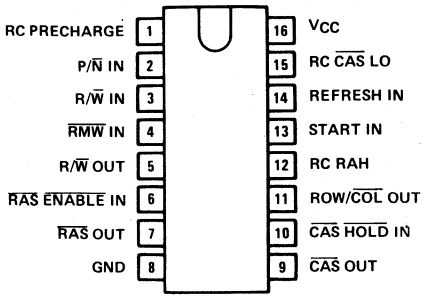
SN54LS' (J)
SN54HC604 (J)

SN74LS' (J or N)
SN74HC604 (N)

PIN ASSIGNMENTS (TOP VIEWS)

MEMORY CYCLE CONTROLLER

608



See page 7-617

SN54LS608 (J) SN74LS608 (J or N)

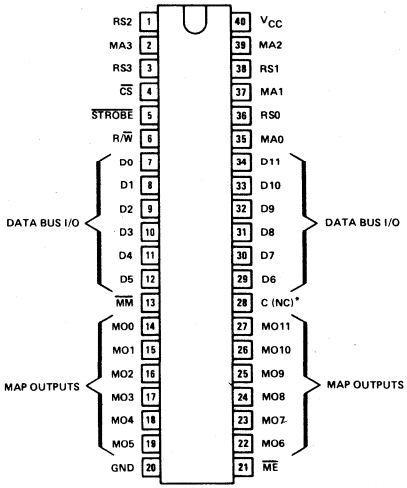
MEMORY MAPPERS

610 3-STATE LATCHED O/P

611 OPEN COLLECTOR LATCHED O/P

612 3-STATE OUTPUTS

613 OPEN COLLECTOR OUTPUTS



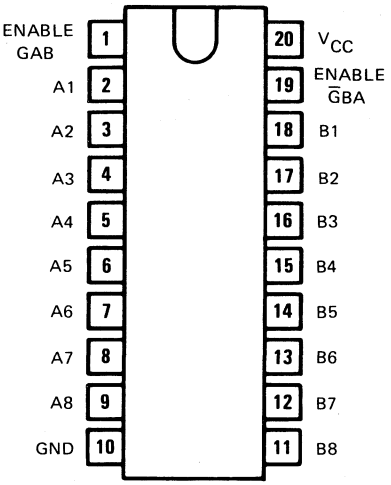
See page 7-622

SN54LS' (J) SN74LS' (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUS TRANCEIVERS

620 3-STATE, INVERTING LOGIC
621 OPEN COLLECTOR, TRUE LOGIC
622 OPEN COLLECTOR, INVERTING
623 3-STATE, TRUE LOGIC

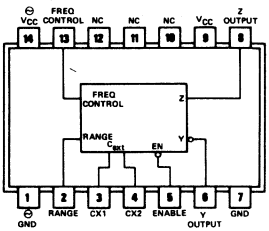


SN54ALS' (J) **SN74ALS' (N)**
SN54AS' (J) **SN74AS' (N)**
SN54HC620 (J) **SN74HC620 (N)**
SN54HC623 (J) **SN74HC623 (N)**
SN54LS' (J) **SN74LS' (N)**

See page 7-630

VOLTAGE-CONTROLLED OSCILLATORS

624 TWO-PHASE OUTPUTS
ENABLE CONTROL
RANGE CONTROL



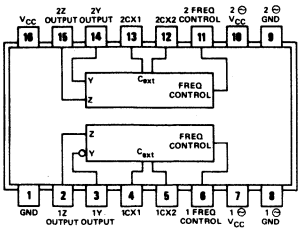
See page 7-634

SN54LS624 (J, W) **SN74LS624 (J, N)**

PIN ASSIGNMENTS (TOP VIEWS)

DUAL VOLTAGE-CONTROLLED OSCILLATORS

625 TWO-PHASE OUTPUTS

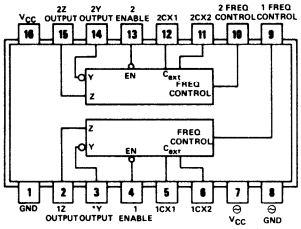


See page 7-634

SN54LS625 (J, W) SN74LS625 (J, N)

DUAL VOLTAGE-CONTROLLED OSCILLATORS

626 TWO-PHASE OUTPUTS
ENABLE CONTROL



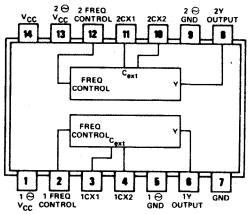
See page 7-634

SN54LS626 (J, W) SN74LS626 (J, N)

PIN ASSIGNMENTS (TOP VIEWS)

DUAL VOLTAGE-CONTROLLED OSCILLATORS

627

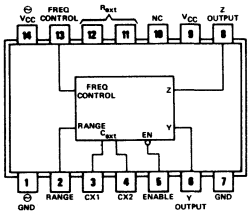


SN54LS627 (J, W) SN74LS627 (J, N)

See page 7-634

VOLTAGE-CONTROLLED OSCILLATORS

628 TWO-PHASE OUTPUTS
ENABLE CONTROL
RANGE CONTROL
EXTERNAL TEMPERATURE COMPENSATION

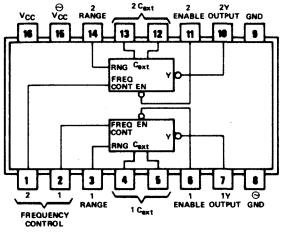


SN54LS628 (J, W) SN74LS628 (J, N)

See page 7-634

DUAL VOLTAGE-CONTROLLED OSCILLATORS

629 ENABLE CONTROL
RANGE CONTROL



SN54LS629 (J, W) SN74LS629 (J, N)

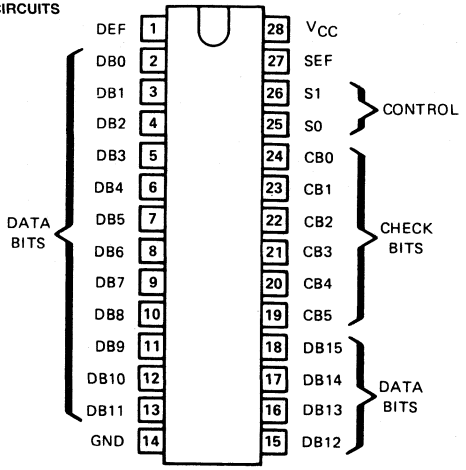
See page 7-634

PIN ASSIGNMENTS (TOP VIEWS)

16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

630 3-STATE OUTPUTS

631 OPEN COLLECTOR OUTPUTS



SN54HC630 (J) **SN74HC630 (N)**
SN54LS630 (J) **SN74LS630 (J, N)**
SN54LS631 (J) **SN74LS631 (J, N)**

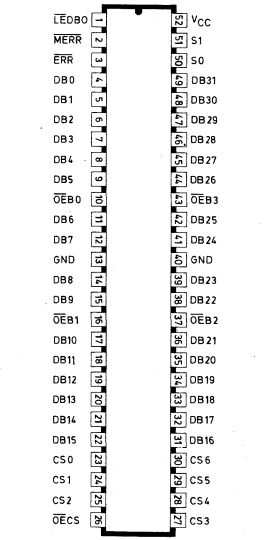
See page 7-640

32-BIT PARALLEL ERROR DETECTION AN CORRECTION CIRCUITS

632 3-STATE OUTPUTS

633 OPEN COLLECTOR OUTPUTS

INCORPORATES BYTE WRITE CAPABILITY



SN54ALS632 (JD) **SN74ALS632 (JD)**
SN54HC632 (J) **SN74HC632 (N)**
SN54ALS633 (JD) **SN74ALS633 (JD)**

See volume II

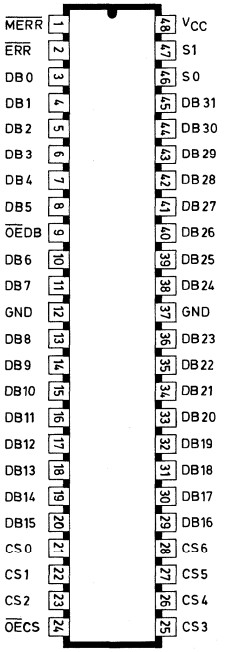
5

PIN ASSIGNMENTS (TOP VIEWS)

32-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

634 3-STATE OUTPUTS

635 OPEN COLLECTOR OUTPUTS



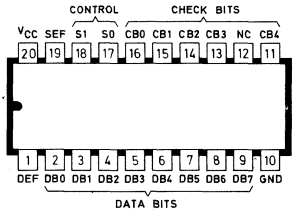
SN54ALS634 (JD) **SN74ALS634 (JD)**
SN54ALS635 (JD) **SN74ALS635 (JD)**

See volume II

8 BIT ERROR DETECTION/CORRECTION CIRCUITS

636 3 STATE OUTPUTS

637 OPEN-COLLECTOR OUTPUTS



SN54LS636 (J) **SN74LS636 (N, J)**
SN54LS637 (J) **SN74LS637 (N, J)**

See page 7-646

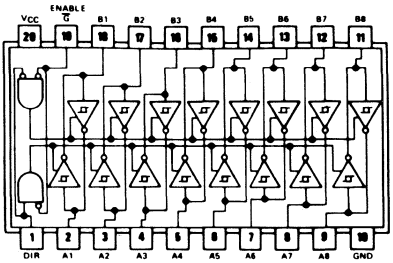
PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUS TRANSCEIVER

638 A BUS OUTPUTS ARE O/C
B BUS OUTPUTS ARE 3-STATE

Inverting logic

See page 7-652



SN54ALS638 (J) **SN74ALS638 (N)**
SN54AS638 (J) **SN74AS638 (N)**
SN54LS638 (J) **SN74LS638 (J or N)**

5

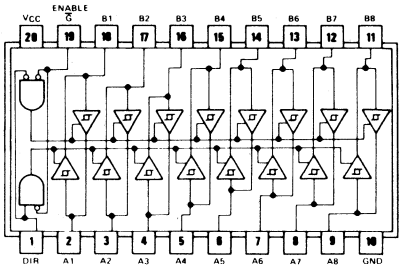
PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUS TRANCEIVER

639 A BUS OUTPUTS ARE O/C
B BUS OUTPUTS ARE 3-STATE

positive logic: see functional table

See page 7-652

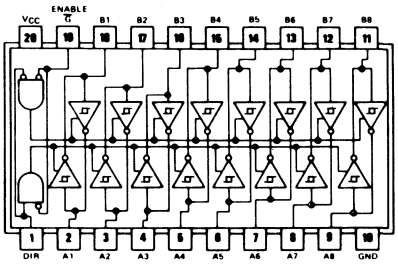


SN54ALS639 (J) **SN74ALS639 (N)**
SN54AS639 (J) **SN74AS639 (N)**
SN54LS639 (J) **SN74LS639 (J or N)**

OCTAL BUS TRANCEIVERS

640 3 STATE INVERTING
642 OPEN-COLLECTOR INVERTING

See page 7-656



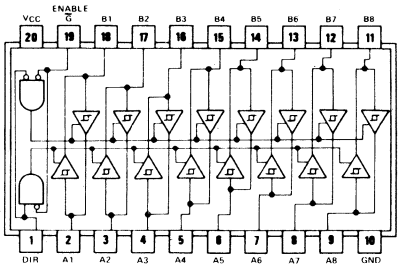
SN54ALS' (J) **SN74ALS' (N)**
SN54LS' (J) **SN74LS' (N, J)**
SN54AS640 (J) **SN74AS640 (N)**
SN54HC640 (J) **SN74HC640 (N)**

OCTAL BUS TRANSCEIVERS

641 OPEN COLLECTOR, TRUE
645 3-StATE, TRUE

positive logic: see function table

See page 7-656



SN54ALS' (J) **SN74ALS' (N)**
SN54AS' (J) **SN74AS' (N)**
SN54LS' (J) **SN74LS' (J or N)**
SN54HC645 (J) **SN74HC645 (N)**

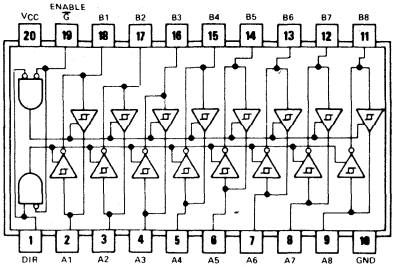
PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUS TRANCEIVERS

643 3-STATE OUTPUTS

644 OPEN COLLECTOR O/P

TRUE AND INVERTING LOGIC



SN54ALS' (J) **SN74ALS' (N)**
SN54AS' (J) **SN74AS' (N)**
SN54LS' (J) **SN74LS' (J or N)**
SN54HC643 (J) **SN74HC643 (N)**

See page 7-656

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OCTAL BUS TRANCEIVERS AND REGISTERS

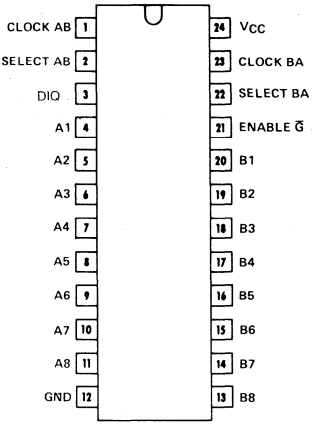
646 3 STATE O/P, TRUE LOGIC

647 OPEN-COLLECTOR O/P, TRUE LOGIC

648 3-STATE O/P, INVERTING LOGIC

649 OPEN COLLECTOR O/P, INVERTING LOGIC

INDEPENDANT REGISTERS FOR A AND B BUSES
MULTIPLEXED REAL-TIME AND STORED DATA



SN54LS' (JT) **SN74LS' (JT or NT)**
SN54AS646 (JT) **SN74AS646 (NT)**
SN54HC646 (JT) **SN74HC646 (NT)**
SN54AS648 (JT) **SN74AS648 (NT)**
SN54HC648 (JT) **SN74HC648 (NT)**

See page 7-663

PIN ASSIGNMENTS (TOP VIEWS)

OCTAL BUS TRANCEIVERS AND REGISTER

651 INVERTING LOGIC, 3-STATE OUTPUTS

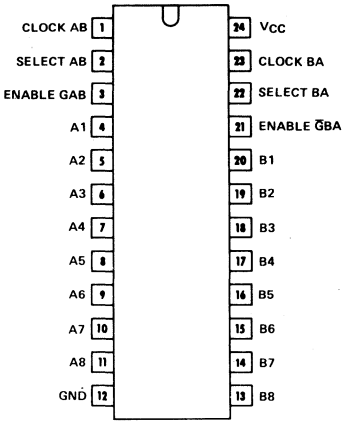
652 TRUE LOGIC, 3-STATE OUTPUTS

653 INVERTING, LOGIC, OPENCOLLECTOR OUTPUTS

654 TRUE LOGIC, OPEN COLLECTOR OUTPUTS

INDEPENDANT REGISTERS AND ENABLES FOR A AND B BUSES
MULTIPLEXED REAL-TIME AND STORED DATA

See page 7-670



SN54LS' (JT)
SN54AS651 (JT)
SN54HC651 (JT)
SN54AS652 (JT)
SN54HC652 (JT)

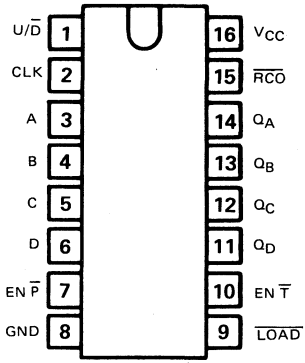
SN74LS' (JT or NT)
SN74AS651 (NT)
SN74HC651 (NT)
SN74AS652 (NT)
SN74HC652 (NT)

SYNCHRONOUS 4-BIT UP-DOWN COUNTERS

668 DECADE COUNTER

669 BINARY COUNTER

See page 7-676



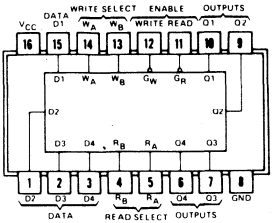
SN54LS' (J or W)

SN74LS' (J or N)

PIN ASSIGNMENTS (TOP VIEWS)

4-BY-4 REGISTER FILES

670 3-STATE OUTPUTS
SIMULTANEOUS READ/WRITE
EXPANDABLE TO 1024 WORDS



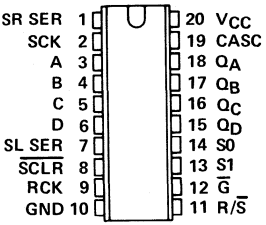
See page 7-684

SN54HC670 (J) SN74HC670 (N)
SN54LS670 (J, W) SN74LS670 (J, N)

4-BIT UNIVERSAL SHIFT REGISTERS/STORAGE REGISTERS WITH 3-STATE OUTPUTS

671 DIRECT SR CLEAR

672 SYNCHRONOUS SR CLEAR



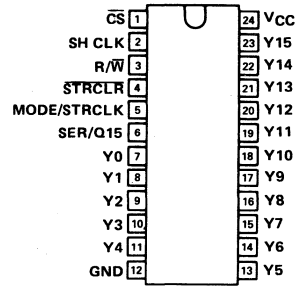
See page 7-690

SN54HC' (J) SN74HC' (N)
SN54LS' (J) SN74LS' (J or N)

16-BIT SHIFT REGISTERS

673 SERIAL-IN, SERIAL OUT SHIFT REGISTER WITH
16 BIT PARALLEL OUT STORAGE REGISTER

- SERIAL TO PARALLEL CONVERSION



SN54LS673 (J) SN74LS673 (J or N)

See page 7-696

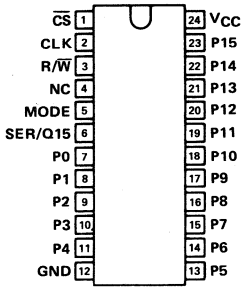
PIN ASSIGNMENTS (TOP VIEWS)

16-BIT SHIFT REGISTERS

674

PARALLEL IN, SERIAL OUT SHIFT REGISTER

- PARALLEL TO SERIAL CONVERSION



NC — No internal connection

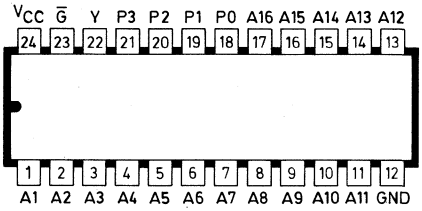
See page 7-696

SN54LS674 (J) SN74LS674 (N)

ADDRESS COMPARATOR

677

16 TO 4 BIT COMPARATOR WITH ENABLE



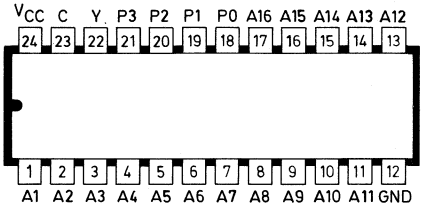
See volume II

SN54ALS677 (JT) SN74ALS677 (NT)
SN54HC677 (JT) SN74HC677 (NT)

ADDRESS COMPARATOR

678

16 TO 4 BIT COMPARATOR WITH LATCH



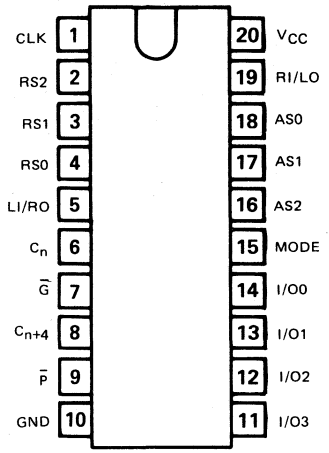
See volume II

SN54ALS678 (JT) SN74ALS678 (NT)
SN54HC678 (JT) SN74HC678 (NT)

PIN ASSIGNMENTS (TOP VIEWS)

4-BIT PARALLEL BINARY ACCUMULATORS

681



See page 7-700

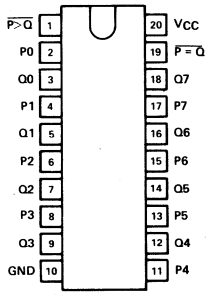
SN54LS681 (J) SN74LS681 (J or N)

5

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT MAGNITUDE COMPARATORS

682 TOTEM POLE O/P (20 KΩ PULL UP ON I/P)
683 OPEN COLLECTOR O/P (20 KΩ PULL UP ON I/P)
684 TOTEM POLE O/P
685 OPEN COLLECTOR O/P



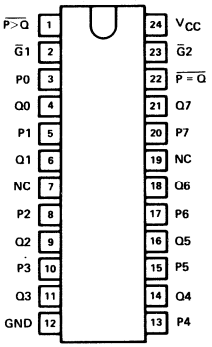
SN54LS' (J) **SN74LS' (J or N)**
SN54HC682 (J) **SN74HC682 (N)**
SN54HC684 (J) **SN74HC684 (N)**

See page 7-706

8-BIT MAGNITUDE COMPARATORS

686 TOTEM POLE O/P
687 OPEN COLLECTOR O/P

WITH OUTPUT ENABLE



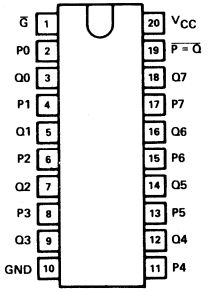
NC = no connection

SN54LS' (JT) **SN74LS' (JT or NT)**

See page 7-706

8-BIT MAGNITUDE COMPARATORS

688 TOTEM POLE O/P
689 OPEN COLLECTOR O/P



SN54ALS' (J) **SN74ALS' (N)**
SN54LS' (J) **SN74LS' (J or N)**
SN54HC688 (J) **SN74HC688 (N)**

See page 7-706

PIN ASSIGNMENTS (TOP VIEWS)

SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

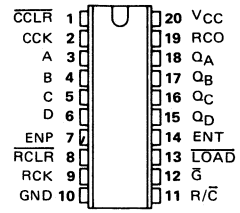
690 DECADE COUNTER, DIRECT CLEAR

691 BINARY COUNTER, DIRECT CLEAR

692 DECADE COUNTER, SYNCHRONOUS CLEAR

693 BINARY COUNTER, SYNCHRONOUS CLEAR

See page 7-714



SN54HC' (J) SN74HC' (N)
SN54LS' (J) SN74LS' (J or N)

SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

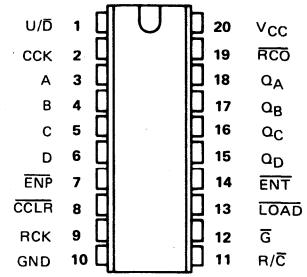
696 DECADE COUNTER, DIRECT CLEAR

697 BINARY COUNTER, DIRECT CLEAR

698 DECADE COUNTER, SYNCHRONOUS CLEAR

699 BINARY COUNTER, SYNCHRONOUS CLEAR

See page 7-720

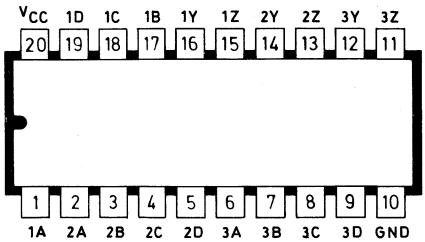


SN54HC' (J) SN74HC' (N)
SN54LS' (J) SN74LS' (J or N)

TRIPLE 4-INPUT AND/NAND DRIVERS

800

positive logic: $Y = \overline{ABCD}$
$Z = \overline{ABCD}$



SN54AS800 (J) SN74AS800 (N)

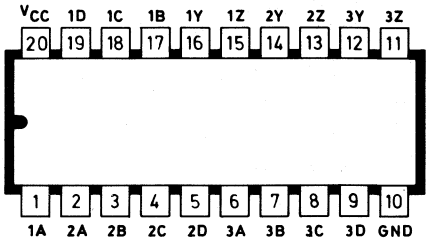
See volume II

PIN ASSIGNMENTS (TOP VIEWS)

TRIPLE 4-INPUT OR/NOR LINE DRIVERS

802

positve logic: $Y = A+B+C+D$
$Z = \overline{A+B+C+D}$

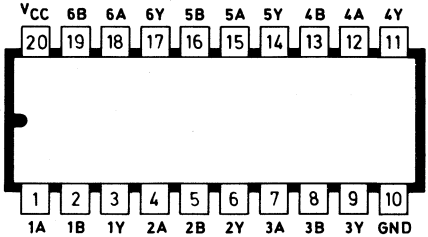


SN54AS802 (J) SN74AS802 (N)

See volume II

HEX 2-INPUT NAND DRIVERS

804



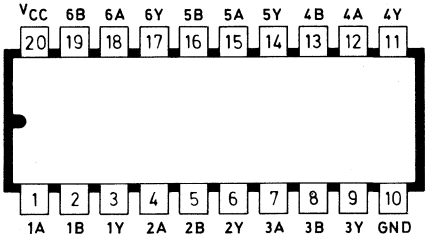
positive logic: $Y = \overline{AB}$

SN54ALS804 (J) SN74ALS804 (N)
SN54AS804A (J) SN74AS804A (N)
SN54HC804 (J) SN74HC804 (N)

See volume II

HEX 2-INPUT NOR DRIVERS

805



positive logic: $Y = \overline{A+B}$

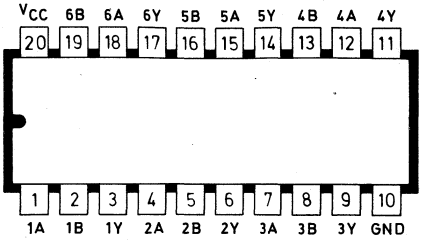
SN54ALS805 (J) SN74ALS805 (N)
SN54AS805A (J) SN74AS805A (N)
SN54HC805 (J) SN74HC805 (N)

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

HEX 2-INPUT AND DRIVERS

808



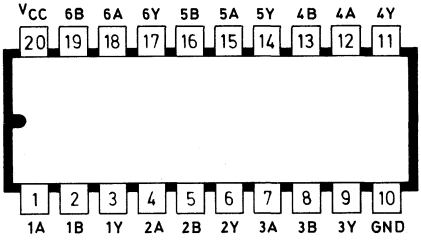
positive logic: Y = AB

See volume II

SN54ALS808 (J) **SN74ALS808 (N)**
SN54AS808A (J) **SN74AS808A (N)**
SN54HC808 (J) **SN74HC808 (N)**

HEX 2-INPUT OR DRIVERS

832



positive logic: Y = A + B

See volume II

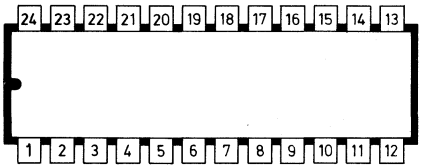
SN54ALS832 (J) **SN74ALS832 (N)**
SN54AS832A (J) **SN74AS832A (N)**
SN54HC832 (J) **SN74HC832 (N)**

5

PIN ASSIGNMENTS (TOP VIEWS)

16 TO 1 MULTIPLEXER

850 3-STATE OUTPUTS



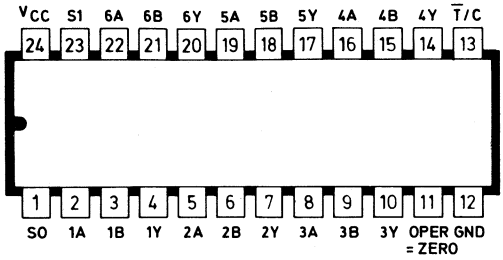
SN54AS850 (JT) **SN74AS850 (NT)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

HEX 2 TO 1 UNIVERSAL MULTIPLEXER

857



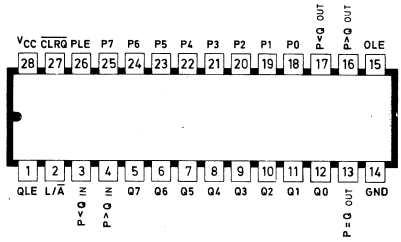
SN54ALS857 (JT) **SN74ALS857 (NT)**
SN54AS857 (JT) **SN74AS857 (NT)**

See volume II

8-BIT MAGNITUDE COMPARATORS WITH LATCHED 8-BIT INPUT

866

INPUT AND OUTPUT LATCHES
WITH ACTIVE-LOW ENABLES



SN54AS866 (JD) **SN74AS866 (N)**

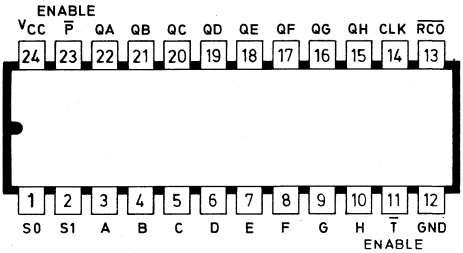
See volume II

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTERS

867 ASYNCHRONOUS CLEAR

869 SYNCHRONOUS CLEAR



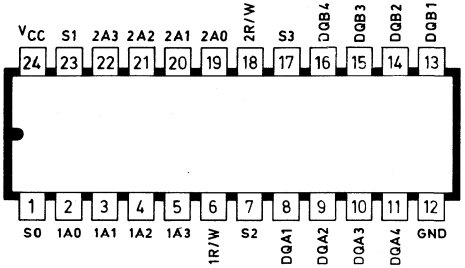
SN54AS867 (JT) SN74AS867 (NT)
SN54AS869 (JT) SN74AS869 (NT)

See volume II

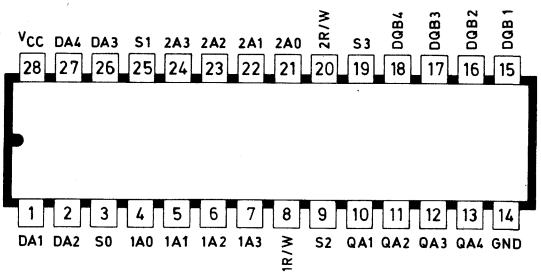
DUAL 16-BY-4 REGISTER FILES

870

871



SN54AS870 (JT) SN74AS870 (NT)



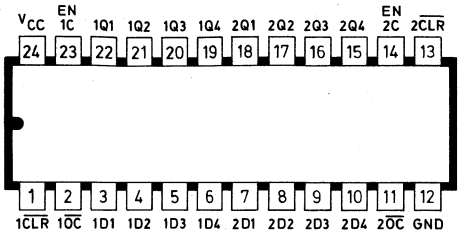
SN54AS871 (J) SN74AS871 (N)

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-BIT D-TYPE LATCHES

873

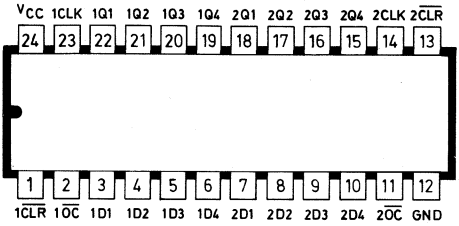


SN54ALS873 (JT) SN74ALS873 (NT)
SN54AS873 (JT) SN74AS873 (NT)

See volume II

DUAL 4-BIT D-TYPE FLIP-FLOP

874

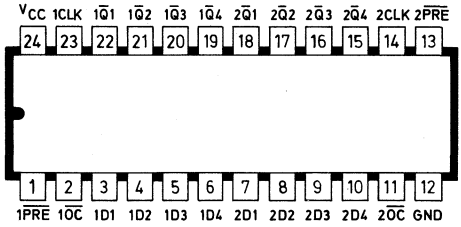


SN54ALS874 (JT) SN74ALS874 (NT)
SN54AS874 (JT) SN74AS874 (NT)

See volume II

DUAL 4-BIT D-TYPE FLIP-FLOP WITH INVERTED OUTPUTS

876



SN54ALS876 (JT) SN74ALS876 (NT)
SN54AS876 (JT) SN74AS876 (NT)

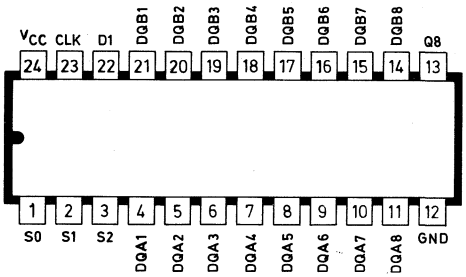
See volume II

5

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT UNIVERSAL TRANCEIVER/PORT CONTROPLLERS

877



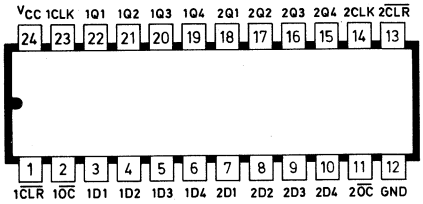
See volume II

SN54AS877 (JT) SN74AS877 (NT)

DUAL 4-BIT D-TYPE EDGE TRIGGERED FLIP FLOPS

878

- 3-STATE OUTPUTS
- FULL PARALLEL ACCESS FOR LOADING
- BUFFERED CONTROL INPUTS
- SYNCHRONOUS CLEAR
- TRUE LOGIC



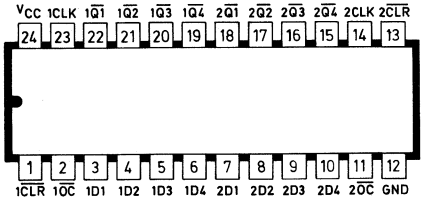
See volume II

SN54ALS878 (JT) SN74ALS878 (NT)
SN54AS878 (JT) SN74AS878 (NT)

DUAL 4-BIT D-TYPE EDGE TRIGGERED FLIP FLOPS

879

- 3-STATE OUTPUTS
- FULL PARALLEL ACCESS FOR LOADING
- BUFFERED CONTROL INPUTS
- SYNCHRONOUS CLEAR
- INVERTING LOGIC



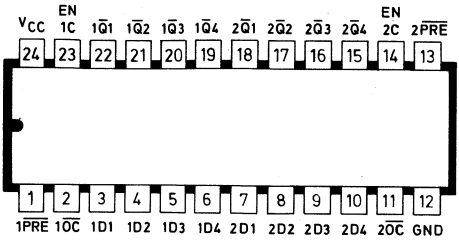
See volume II

SN54ALS879 (JT) SN74879 (NT)
SN54AS879 (JT) SN74AS879 (NT)

PIN ASSIGNMENTS (TOP VIEWS)

DUAL 4-BIT D-TYPE LATCHES WITH INVERTED OUTPUTS

880

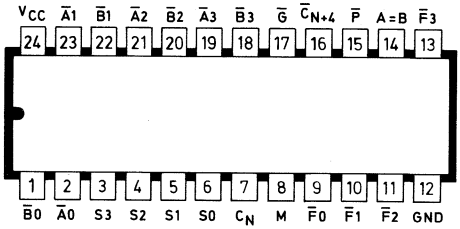


SN54ALS880 (JT) SN74ALS880 (NT)
SN54AS880 (JT) SN74AS880 (NT)

See volume II

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

881

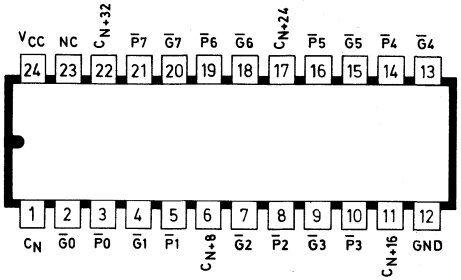


SN54AS881A (JT) SN74AS881A (NT)

See volume II

32-BIT LOOK-AHEAD CARRY GENERATORS

882



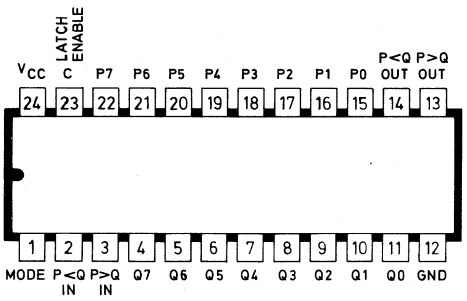
SN54AS882 (JT) SN74AS882 (NT)

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

8-BIT MAGNITUDE COMPARATORS

885

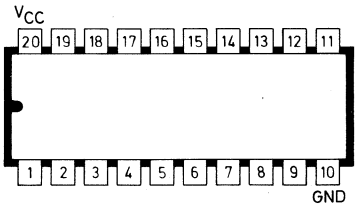


See volume II

SN54AS885 (JT) SN74AS885 (NT)

EX-OR, HEX 2-INPUT LINE DRIVERS

886

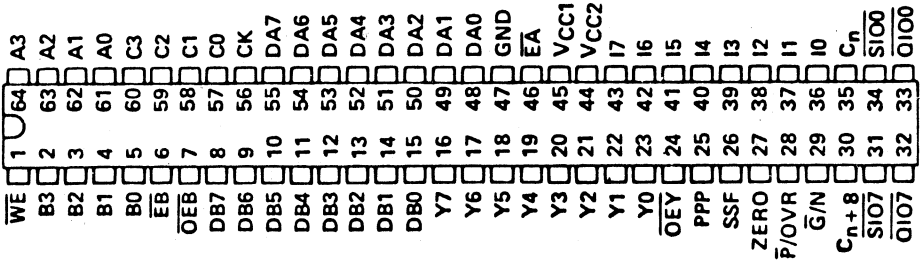


See volume II

SN54AS886 (J) SN74AS886 (N)

8-BIT SLICE

888



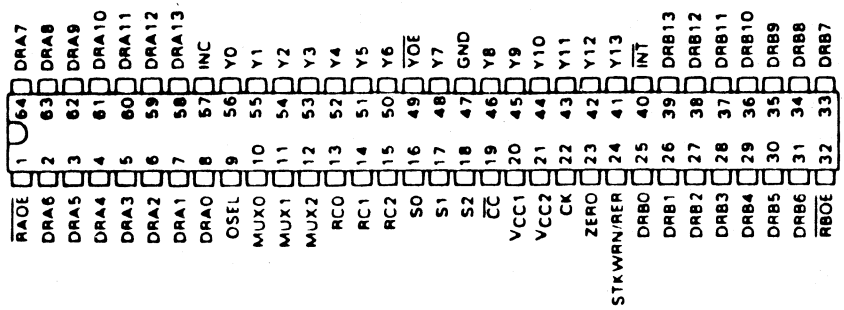
See volume II

SN54AS888 (J) SN74AS888 (N)

PIN ASSIGNMENTS (TOP VIEWS)

14-BIT CONTROLLER FOR 'AS888

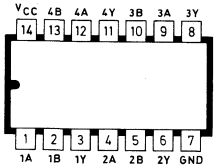
890



See volume II

SN54AS890 (J) SN74AS890 (N)

positive logic: Y = AB



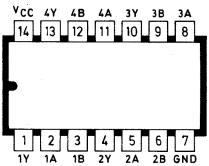
QUAD 2-INPUT NAND GATE

1000

SN54ALS1000 (J) SN74ALS1000 (N)
SN54AS1000 (J) SN74AS1000 (N)

See volume II

positive logic: $Y = \overline{A + B}$



QUAD 2-INPUT NOR GATE

1002

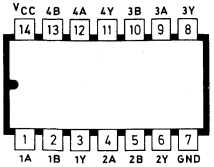
SN54ALS1002 (J) SN74ALS1002 (N)

See volume II

5

PIN ASSIGNMENTS (TOP VIEWS)

positive logic: $Y = \overline{AB}$



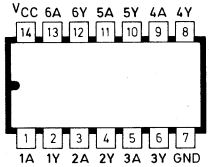
QUAD 2-INPUT NAND GATE (OC)

1003

SN54ALS1003 (J) SN74ALS1003 (N)

See volume II

positive logic: $Y = \overline{A}$



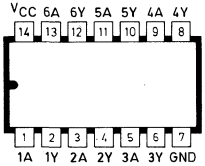
HEX INVERTORS

1004

SN54ALS1004 (J) SN74ALS1004 (N)
SN54AS1004 (J) SN74AS1004 (N)

See volume II

positive logic: $Y = \overline{A}$



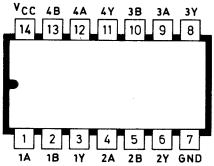
HEX INVERTORS (O.C. OUTPUTS)

1005

SN54ALS1005 (J) SN74ALS1005 (N)

See volume II

positive logic: Y = AB



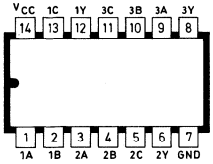
QUAD 2-INPUT AND GATE

1008

SN54ALS1008 (J) SN74ALS1008 (N)
SN54AS1008 (J) SN74AS1008 (N)

See volume II

positive logic: $Y = \overline{ABC}$



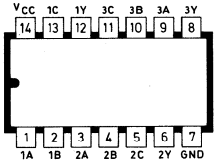
TRIPLE 3-INPUT NAND GATE

1010

SN54ALS1010 (J) SN74ALS1010 (N)

See volume II

positive logic: Y = ABC



TRIPLE 3-INPUT AND GATE

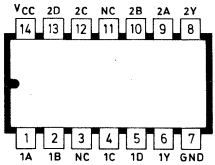
1011

SN54ALS1011 (J) SN74ALS1011 (N)

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

positive logic: $Y = \overline{ABCD}$



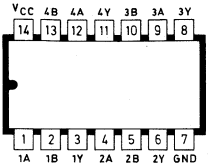
DUAL 4-INPUT NAND GATE

1020

SN54ALS1020 (J) SN74ALS1020 (N)

See volume II

positive logic: $Y = A + B$



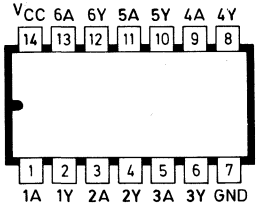
QUAD 2-INPUT OR GATE

1032

SN54ALS1032 (J) SN74ALS1032 (N)
SN54AS1032 (J) SN74AS1032 (N)

See volume II

positive logic: $Y = A$



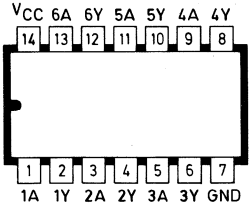
HEX NON INVERTING BUFFERS

1034

SN54ALS1034 (J) SN74ALS1034 (N)
SN54AS1034 (J) SN74AS1034 (N)

See volume II

positive logic: $Y = A$



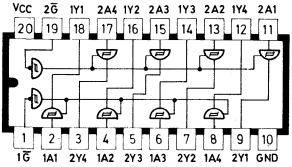
HEX NON INVERTING BUFFERS WITH OPEN COLLECTOR OUTPUTS

1035

SN54ALS1035 (J) SN74ALS1035 (N)
SN54AS1035 (J) SN74AS1035 (N)

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

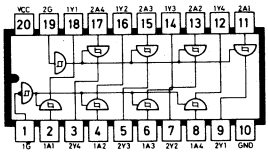


OCTAL BUFFERS / LINE DRIVERS / LINE RECEIVERS

1240 INVERTED 3-STATE OUTPUTS

SN54ALS1240 (J) **SN74ALS1240 (N)**

See volume II

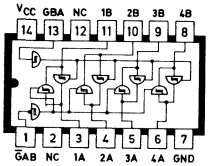


OCTAL BUS TRANCEIVERS

1241 NON-INVERTED 3-STATE OUTPUTS

SN54ALS1241 (J) **SN74ALS1241 (N)**

See volume II

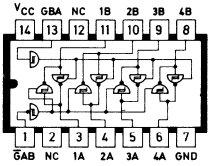


QUADRUPLE BUS TRANCEIVERS

1242 INVERTED 3-STATE OUTPUTS

PLANNED PRODUCTS:
SN54ALS1242 (J) **SN74ALS1242 (N)**

See volume II

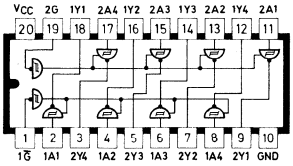


QUADRUPLE BUS TRANCEIVERS

1243 NON INVERTED 3-STATE OUTPUTS

PLANNED PRODUCTS:
SN54ALS1243 (J) **SN74ALS1243 (N)**

See volume II

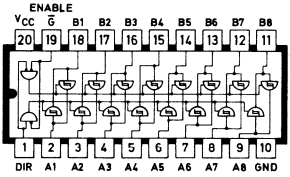


OCTAL BUFFERS / LINE DRIVERS / LINE RECEIVERS

1244 NON-INVERTED 3-STATE OUTPUTS

SN54ALS1244 (J) **SN74ALS1244 (N)**

See volume II



OCTAL BUS TRANCEIVERS

1245 NON-INVERTED 3-STATE OUTPUTS

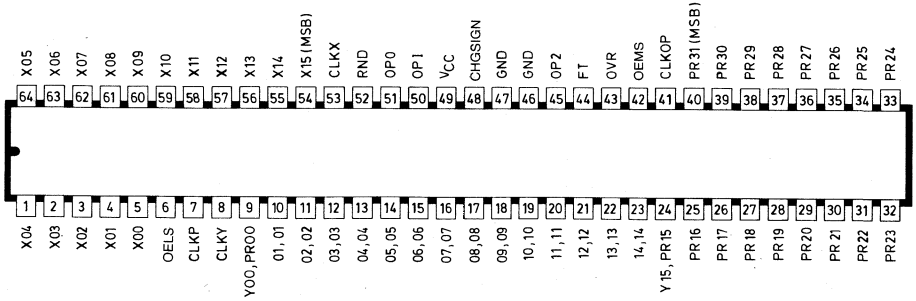
SN54ALS1245 (J) **SN74ALS1245 (N)**

See volume II

PIN ASSIGNMENTS (TOP VIEWS)

16 × 16 BIT MULTIMODE MULTIPLIERS

1616



See volume II **SN54ALS1616 (J)** **SN74ALS1616 (J, N)**

OCTAL BUS TRANCEIVERS

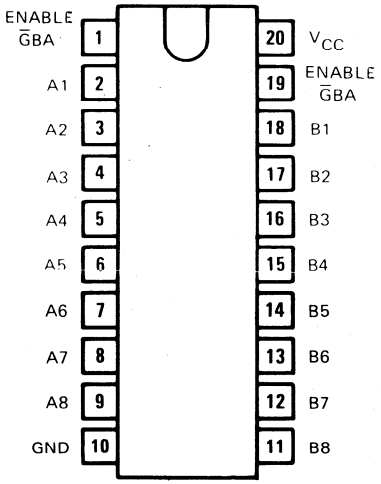
1620 3-STATE, INVERTING-LOGIC

1621 OPEN COLLECTOR, TRUE LOGIC

1622 OPEN COLLECTOR, INVERTING

1623 3-STATE, TRUE LOGIC

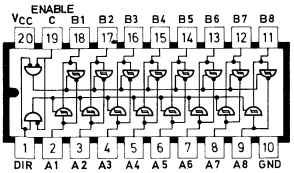
LOW POWER SELECTIONS OF '620 SERIES



See volume II **PLANNED PRODUCTS: SN54ALS' (J)** **SN74ALS' (N)**

PIN ASSIGNMENTS (TOP VIEWS)

1638 OCTAL BUS TRANCEIVER

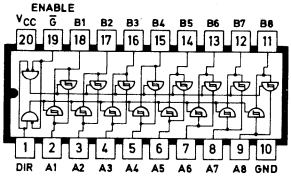


positive logic: see function fable

PLANNED PRODUCTS:
SN54ALS1638 (J) **SN74ALS1638 (N)**

See volume II

1639 OCTAL BUS TRANCEIVER

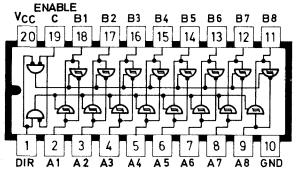


positive logic: see function table

PLANNED PRODUCTS:
SN54ALS1639 (J) **SN74ALS1639 (N)**

See volume II

1640 OCTAL BUS TRANCEIVERS
1642

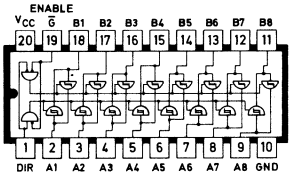


positive logic: see function table

SN54ALS1640 (J) **SN74ALS1640 (N)**
PLANNED PRODUCTS:
SN54ALS1642 (J) **SN74ALS1642 (N)**

See volume II

1641 OCTAL BUS TRACEIVERS
1645

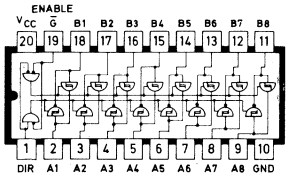


positive logic: see function table

SN54ALS1641 (J) **SN74ALS1641 (N)**
PLANNED PRODUCTS:
SN54ALS1645 (J) **SN74ALS1645 (N)**

See volume II

1643 OCTAL BUS TRANCEIVERS
1644

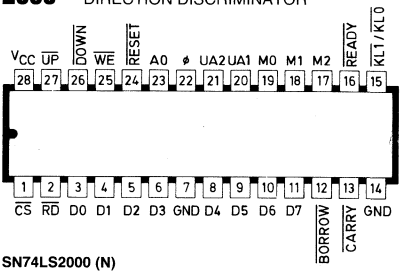


positive logic: see function table

PLANNED PROUCTS:
SN54ALS1643 (J) **SN74ALS1643 (N)**
SN54ALS1644 (J) **SN74ALS1644 (N)**

See volume II

2000 DIRECTION DISCRIMINATOR

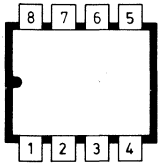


SN74LS2000 (N)

See page 7-726

PIN ASSIGNMENTS (TOP VIEWS)

8003 DUAL INPUT NAND GATES



SN54ALS8003 (JG) **SN74ALS8003 (P)**

See volume II

5

54/74 Family SSI Circuits

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−400			−1000	μA
	74 Family			−400			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			4			20	mA
	74 Family			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.25	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS						0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V										mA
					V_{IL} = 0.4 V			−1.6			−0.4				
					V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
					74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS', and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.

supply current¶

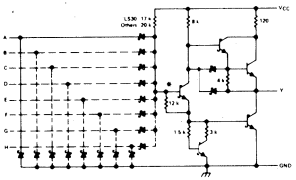
TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	6	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'S00	10	16	20	36	3.75
'S04	15	24	30	54	3.75
'S10	7.5	12	15	27	3.75
'S20	5	8	10	18	3.75
'S30	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15
'LS00, 'LS04 'LS10, 'LS20	C_L = 15 pF, R_L = 2 kΩ		9	15		10	15
'LS30			8	15		13	20
'S00, 'S04	C_L = 15 pF, R_L = 280 Ω		3	4.5		3	5
'S10, 'S20	C_L = 50 pF, R_L = 280 Ω		4.5			5	
'S30, 'S133	C_L = 15 pF, R_L = 280 Ω		4	6		4.5	7
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5	

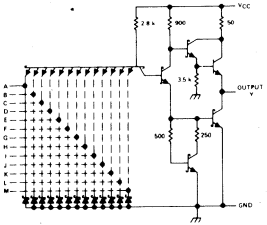
#Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.



'LS00, 'LS04, 'LS10, 'LS20, 'LS30 CIRCUITS

*The 12-kΩ resistor is not on 'LS30.



'S00, 'S04, 'S10, 'S20, 'S30, 'S133 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '01, '03, '05, '12, '22			SERIES 54LS / SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS12, 'LS22			SERIES 54S / SERIES 74S 'S03, 'S05, 'S22			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			16			4			20	mA
	74 Family			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '01, '03, '05, '12, '22			SERIES 54LS / SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS12, 'LS22			SERIES 54S / SERIES 74S 'S03, 'S05, 'S22			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{OH} = 5.5 V					250			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V										mA
					V_{IL} = 0.4 V			−1.6			−0.4				
					V_{IL} = 0.5 V									−2	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

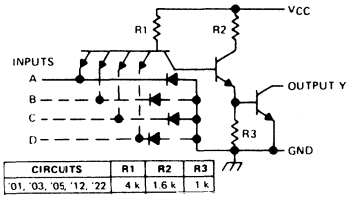
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per Gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'01	4	8	12	22	2
'03	4	8	12	22	2
'05	6	12	18	33	2
'12	3	6	9	16.5	2
'22	2	4	6	11	2
'LS01	0.8	1.6	2.4	4.4	0.4
'LS03	0.8	1.6	2.4	4.4	0.4
'LS05	1.2	2.4	3.6	6.6	0.4
'LS12	0.7	1.4	1.8	3.3	0.42
'LS22	0.4	0.8	1.2	2.2	0.4
'S03	6	13.2	20	36	3.25
'S05	9	19.8	30	54	3.25
'S22	3	6.6	10	18	3.25

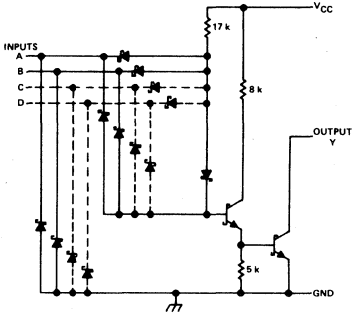
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)

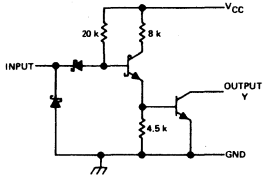


CIRCUITS	R1	R2	R3
'01, '03, '05, '12, '22	4 k	1.6 k	1 k

'01, '03, '05, '12, '22, CIRCUITS



'LS01, 'LS03, 'LS12, 'LS22 CIRCUITS

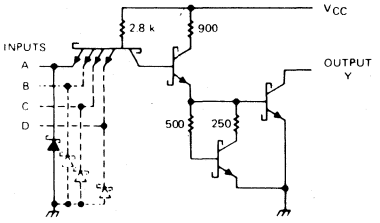


'LS05 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'01, '03	C_L = 15 pF, R_L = 4 kΩ for t_{PLH}, 400 Ω for t_{PHL}		35	45		8	15
'05			40	55		8	15
'12, '22			35	45		8	15
'LS01, 'LS03, 'LS05, 'LS12, 'LS22	C_L = 15 pF, R_L = 2 kΩ		17	32		15	28
'S03, 'S05, 'S22	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω		7.5			7	

#Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

OPEN-COLLECTOR OUTPUT APPLICATION DATA

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

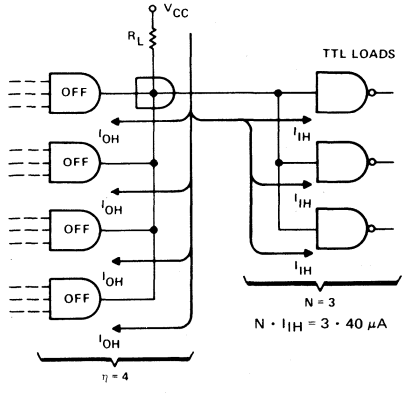
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\ \Omega = \frac{2.6}{0.00112}\ \Omega = 2321\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For devices in other series, substitute appropriate values.

FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

APPLICATION DATA

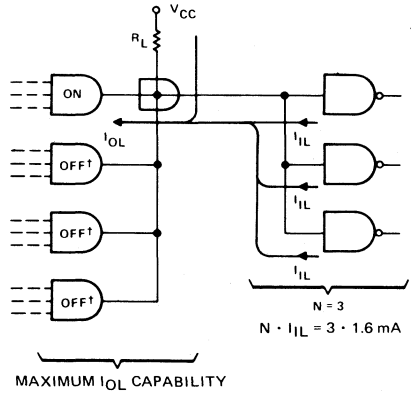
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL}, the maximum current which will ensure that the low-level output voltage, V_{OL}, will be below V_{OL} max.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For devices in other series, substitute the appropriate values.

†Current into OFF outputs is negligible at the low logic level.

FIGURE B–LOW-LEVEL CIRCUIT CONDITIONS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '02			SERIES 54 / SERIES 74 '25, '27			SERIES 54LS / SERIES 74LS 'LS02, 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−800			−400			−1000	μA
	74 Family			−400			−800			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			16			4			20	mA
	74 Family			16			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '02, '25, '27			SERIES 54LS / SERIES 74LS 'LS02 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
							MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2				2			2			2			V
V_{IL}	Low-level input voltage		1, 2			54 Family			0.8			0.7			0.8	V
						74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
						74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
						74 Family		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
						V_I = 7 V						0.1				
I_{IH}	High-level input current	Data inputs	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
		Strobe of '25							160							
		All inputs				V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	All inputs	5	V_{CC} = MAX		V_{IL} = 0.3 V										mA
		Data inputs				V_{IL} = 0.4 V			−1.6			−0.4				
		Strobe of '25							−6.4							
		All inputs				V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
						74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current		7	V_{CC} = MAX			See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S/SN74S'.

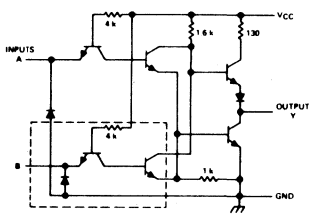
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'02	8	16	14	27	2.75
'25	8	16	10	19	2.25
'27	10	16	16	26	4.34
'LS02	1.6	3.2	2.8	5.4	0.55
'LS27	2.0	4	3.4	6.8	0.9
'S02	17	29	26	45	5.38
'S260	17	29	26	45	10.75

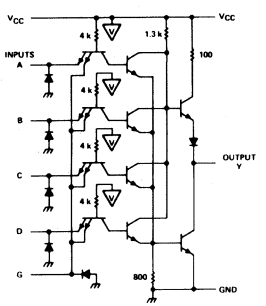
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



'25 CIRCUITS

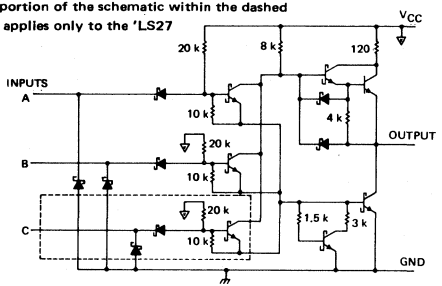
Resistor values are nominal and in ohms.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

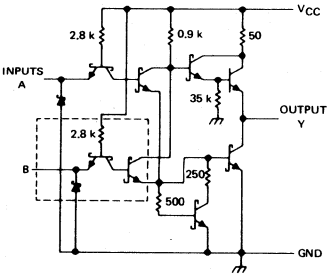
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C_L = 15 pF, R_L = 400 Ω		12	22		8	22
'25			13	22		8	15
'27			10	15		7	11
'LS02, 'LS27	C_L = 15 pF, R_L = 2 kΩ		10	15		10	15
'S02	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5	
'S260	C_L = 15 pF, R_L = 280 Ω		4	5.5		4	6

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

The portion of the schematic within the dashed lines applies only to the 'LS27



'LS02, 'LS27 CIRCUITS



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '08,			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400			−1000	μA
Low-level output current, I_{OL}		54 Family			16			4			20	mA
		74 Family			16			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '08			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S08, 'S11			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7.0 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−0.4				mA
					V_{IL} = 0.5 V									−2	
I_{OS}	Short circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
					74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡All typical values are at V_{CC} = 25°C.

§I_I = −12 mA for SN54'/SN74', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short circuit should not exceed one second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'LS08	2.4	4.8	4.4	8.8	0.85
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S08	18	32	32	57	6.25
'S11	13.5	24	24	42	6.25

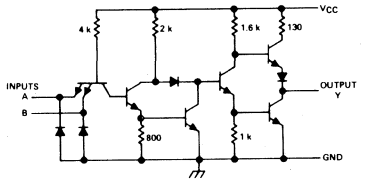
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

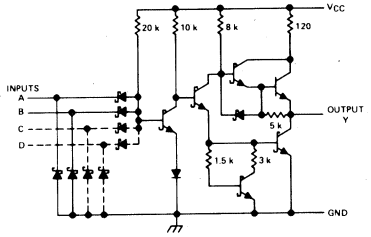
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
'LS08, 'LS11 'LS21	C_L = 15 pF, R_L = 2 kΩ		8	15		10	20
'S08, 'S11	C_L = 15 pF, R_L = 280 Ω		4.5	7		5	7.5
	C_L = 50 pF, R_L = 280 Ω		6			7.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

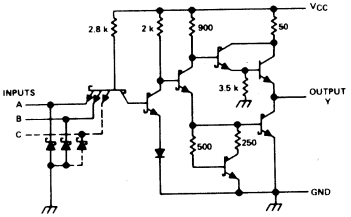
schematics (each gate)



'08 CIRCUITS



'LS08, 'LS11, 'LS21 CIRCUITS



'S08, 'S11 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '09			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			16			4			20	mA
	74 Family			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '09			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S09, 'S15			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V,					250			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = $V_{IL\ MAX}$	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−0.4				mA
					V_{IL} = 0.5 V									−2	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = − 12 mA for SN54'/SN74', and −18 mA for SN54LS'/SN74LS'.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'09	11	21	20	33	3.88
'LS09	2.4	4.8	4.4	8.8	0.85
'LS15	1.8	3.6	3.3	6.6	0.85
'S09	18	32	32	57	6.25
'S15	10.5	19.5	24	42	5.75

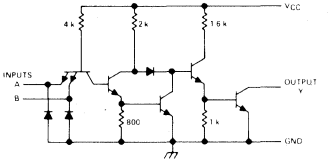
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

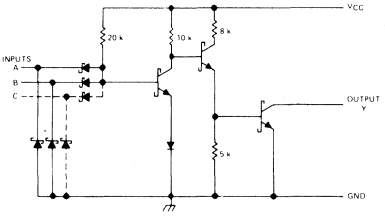
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'09	C_L = 15 pF, R_L = 400 Ω		21	32		16	24
'LS09, 'LS15	C_L = 15 pF, R_L = 2 kΩ		20	35		17	35
'S09	C_L = 15 pF, R_L = 280 Ω		6.5	10		6.5	10
	C_L = 50 pF, R_L = 280 Ω		9			9	
'S15	C_L = 15 pF, R_L = 280 Ω		5.5	8.5		6	9
	C_L = 50 pF, R_L = 280 Ω		8.5			8	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

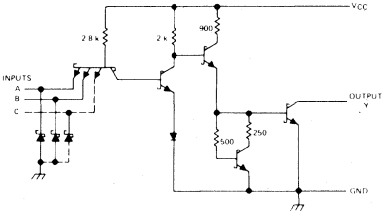
schematics (each gate)



'09 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S09, 'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '13			SERIES 54 SERIES 74 '14, '132			SERIES 54LS SERIES 74LS 'LS13, 'LS14, 'LS132			SERIES 54S SERIES 74S 'S132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High level output current, I_{OH}				−800			−800			−400			−1000	μA
Low-level output current, I_{OL}	54 Family			16			16			4			20	mA
	74 Family			16			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '13			SERIES 54 SERIES 74 '14, '132			SERIES 54LS SERIES 74LS 'LS13, 'LS14, 'LS132			SERIES 54S SERIES 74S 'S132			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	8	V_{CC} = 5 V			1.5	1.7	2	1.5	1.7	2	1.4	1.6	1.9	1.6	1.77	1.9	V
V_{T-}	Negative-going threshold voltage	9	V_{CC} = 5 V			0.6	0.9	1.1	0.6	0.9	1.1	0.5	0.8	1	1.1	1.22	1.4	V
	Hysteresis (V_{T+}-V_{T-})	8, 9	V_{CC} = 5 V			0.4	0.8		0.4	0.8		0.4	0.8		0.2	0.55		V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	9	V_{CC} = MIN, V_I = V_{T-} min	I_{OH} = MAX,	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	8	V_{CC} = MIN, V_I = V_{T+} max	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS								0.25	0.4				
I_{T+}	Input current at positive-going threshold	8	V_{CC} = 5 V,	V_I = V_{T+}			−0.65			−0.43			−0.14			−0.9		mA
I_{T-}	Input current at negative-going threshold	9	V_{CC} = 5 V,	V_I = V_{T-}			−0.85			−0.56			−0.18			−1.1		mA
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_I = 2.4 V			40			40							μA
					V_I = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V		−1	−1.6		−0.8	−1.2			−0.4				mA
					V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX			−18		−55	−18		−55	−20		−100	−40		−100	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for 'LS13, 'LS14, 'LS132, and 'S132.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and 'S132, duration of output short-circuit should not exceed one second.

supply current¶

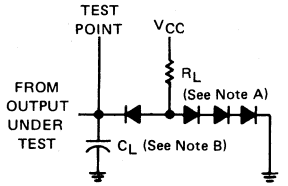
TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'13	14	23	20	32	8.5
'14	22	36	39	60	5.1
'132	15	24	26	40	5.1
'LS13	2.9	6	4.1	7	1.75
'LS14	8.6	16	12	21	1.72
'LS132	5.9	11	8.2	14	1.76
'S132	28	44	44	68	9

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A: typical values are at V_{CC} = 5 V, T_A = 25°C.

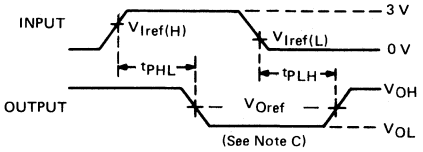
switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'13	C_L = 15 pF, R_L = 400 Ω		18	27		15	22
'14, '132			15	22		15	22
'LS13	C_L = 15 pF, R_L = 2 kΩ		15	22		18	27
'LS14			15	22		15	22
'LS132			15	22		15	22
'S132	C_L = 15 pF, R_L = 280 Ω		7	10.5		8.5	13

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

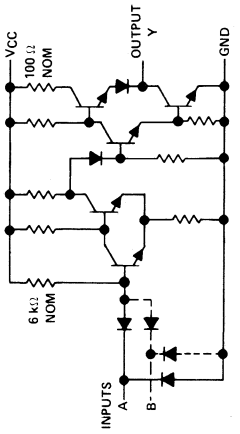


VOLTAGE WAVEFORMS

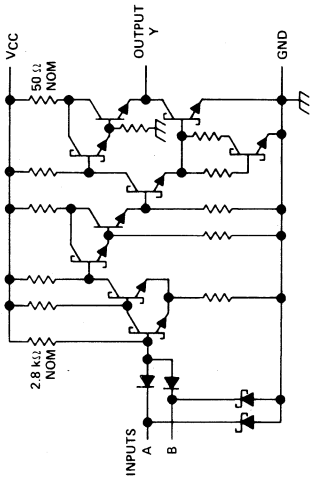
NOTES: A. All diodes are 1N916 or 1N3064.
B. C_L includes probe and jrg capacitance.
C. Generator characteristics and reference voltages are:

	Generator Characteristics				Reference Voltages		
	Z_{out}	PRR	t_r	t_f	$V_{I\ ref(H)}$	$V_{I\ ref(L)}$	$V_{O\ ref}$
SN54'/SN74'	50 Ω	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V
SN54LS'/SN74LS'	50 Ω	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V
'S132	50 Ω	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V

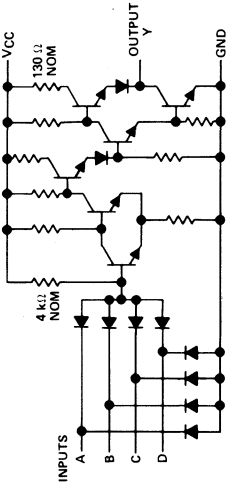
schematics (each gate)



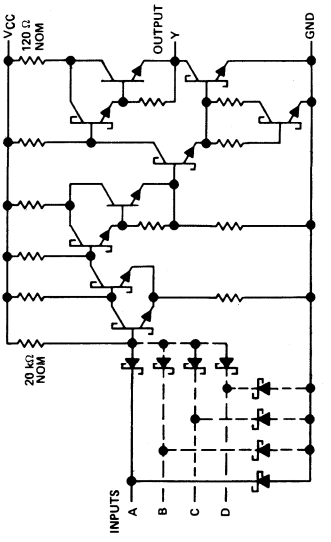
'14, '132 CIRCUITS



'S132 CIRCUITS



'13 CIRCUITS



'LS13, 'LS14, 'LS132 CIRCUITS

Resistor values shown are nominal.

TYPICAL CHARACTERISTICS OF '13, '14, AND '132 CIRCUITS†

POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

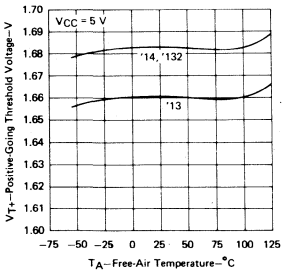


FIGURE 1

NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

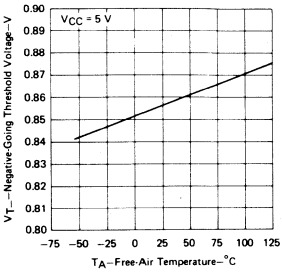


FIGURE 2

HYSTERESIS
vs
FREE-AIR TEMPERATURE

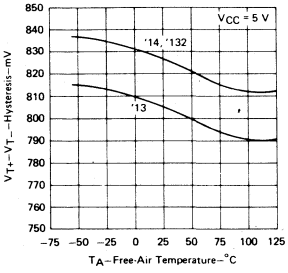


FIGURE 3

'13
DISTRIBUTION OF UNITS
FOR HYSTERESIS

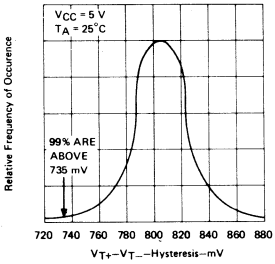


FIGURE 4

'14, '132
DISTRIBUTION OF UNITS
FOR HYSTERESIS

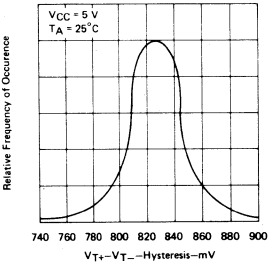


FIGURE 5

THRESHOLD VOLTAGES
vs
SUPPLY VOLTAGE

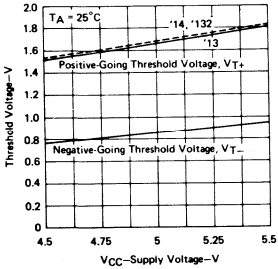


FIGURE 6

HYSTERESIS
vs
SUPPLY VOLTAGE

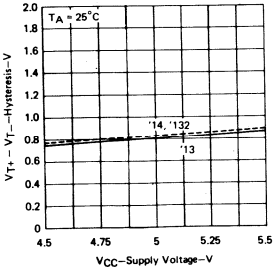


FIGURE 7

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

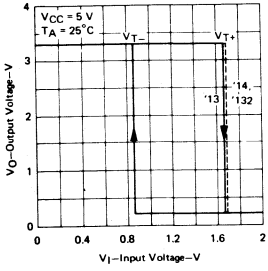
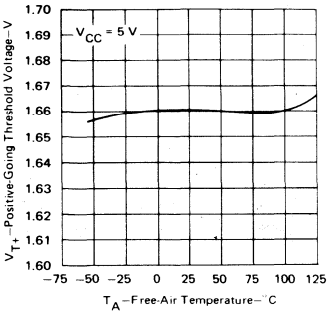


FIGURE 8

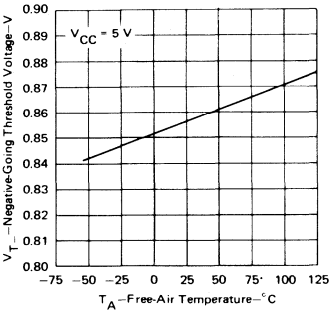
†Data for temperatures below 0°C and 70°C and supply voltages below 4.75V and above 5.25 V are applicable for SN5413, SN5414, and SN54132 only.

TYPICAL CHARACTERISTICS OF 'LS13, 'LS14, AND 'LS132 CIRCUITS†

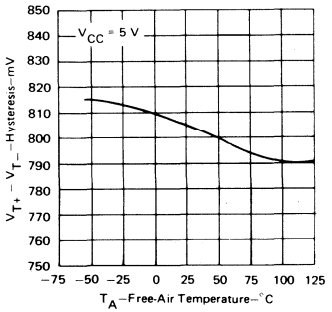
POSITIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



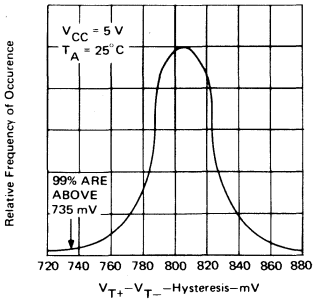
NEGATIVE-GOING THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE



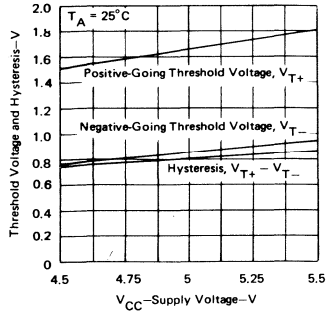
HYSTERESIS
vs
FREE-AIR TEMPERATURE



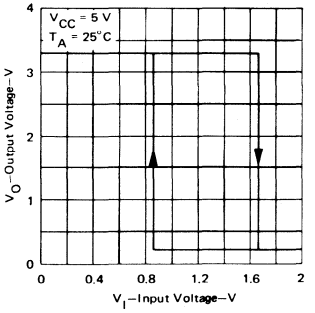
DISTRIBUTION OF UNITS
FOR HYSTERESIS



THRESHOLD VOLTAGES AND HYSTERESIS
vs
SUPPLY VOLTAGE

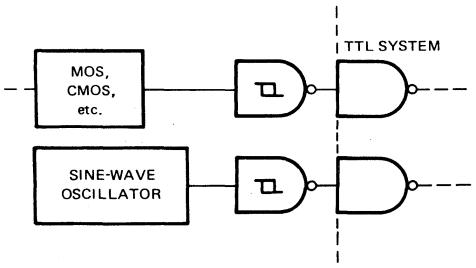


OUTPUT VOLTAGE
vs
INPUT VOLTAGE

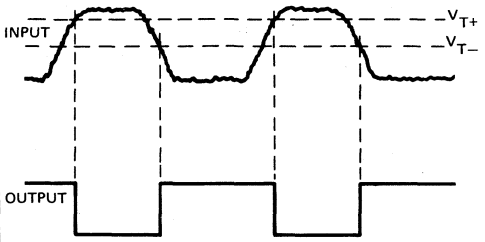


†Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 are applicable for SN54LS13, SN54LS14, and SN54LS132 only.

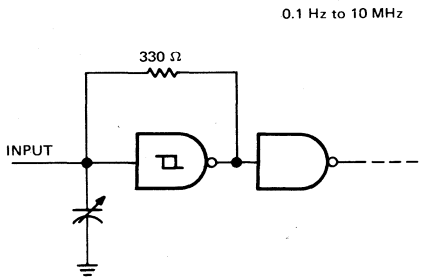
TYPICAL APPLICATION DATA



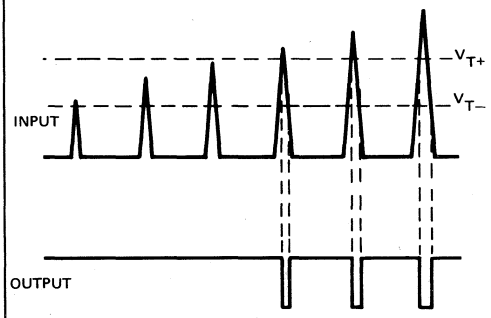
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



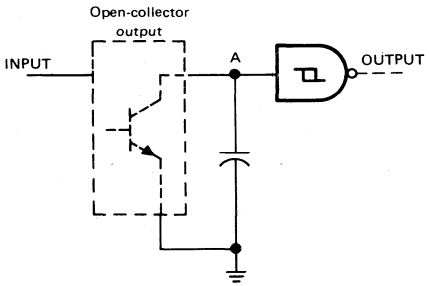
PULSE SHAPER

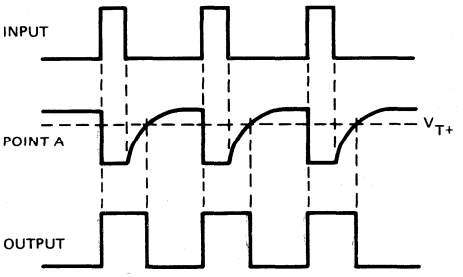


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '28			SERIES 54 SERIES 74 '37, '40			SERIES 54LS SERIES 74LS 'LS28, 'LS37 'LS40			SERIES 54S SERIES 74S 'S37, 'S40			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−2.4			−1.2			−1.2			−3	mA
Low-level output current, I_{OL}	54 Family			48			48			12			60	mA
	74 Family			48			48			24			60	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '28			SERIES 54 SERIES 74 '37, '40			SERIES 54LS SERIES 74LS 'LS28, 'LS37, 'LS40			SERIES 54S SERIES 74S 'S37, 'S40			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, I_{OH} = MAX	V_{IL} = V_{IL} max,	54 Family	2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.3		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 12 mA	Series 74LS								0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1			1						1	mA
					V_I = 7 V									0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			40							µA
					V_{IH} = 2.7 V									20			100	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−1.6			−0.4				mA
					V_{IL} = 0.5 V												−4	
I_{OS}	Short-circuit output current♦	6			54 Family	−70		−180	−20		−70	−30		−130	−50		−225	mA
					74 Family	−70		−180	−18		−70	−30		−130	−50		−225	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C.

§I_I = −12 mA for SN54'/SN74', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for all of these circuits except 'S37 and 'S40, or 100 milliseconds for 'S37 and 'S40.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'28	12	21	33	57	5.63
'37	9	15.5	34	54	5.38
'40	4	8	17	27	5.25
'LS28	1.8	3.6	6.9	13.8	1.09
'LS37	0.9	2	6	12	0.86
'LS40	0.45	1	3	6	0.86
'S37	20	36	46	80	8.25
'S40	10	18	25	44	8.75

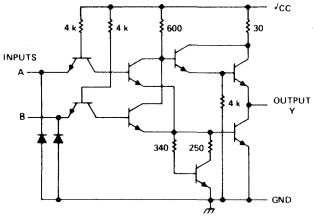
¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

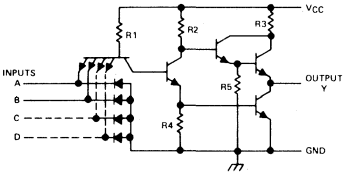
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low output		
		MIN	TYP	MAX	MIN	TYP	MAX
'28	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'37	C_L = 45 pF, R_L = 133 Ω		13	22		8	15
'40	C_L = 15 pF, R_L = 133 Ω		13	22		8	15
'LS28	C_L = 45 pF, R_L = 667 Ω		12	24		12	24
'LS37			12	24		12	24
'LS40			12	24		12	24
'S37, 'S40	C_L = 50 pF, R_L = 93 Ω		4	6.5		4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

schematics (each gate)

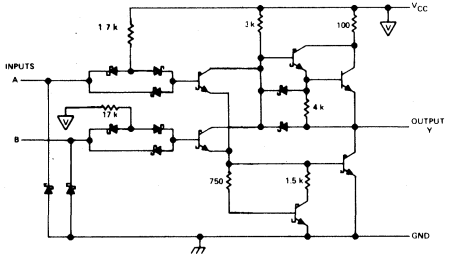


'28 CIRCUITS

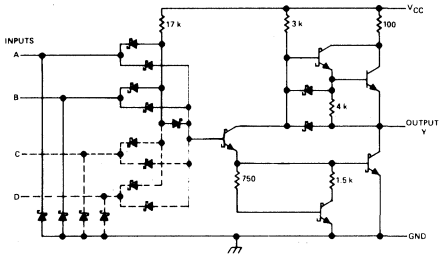


'37, '40, CIRCUITS

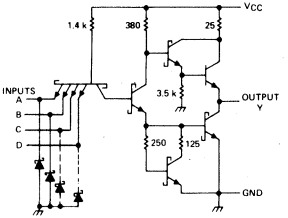
	'37	'40	'H40
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k



'LS28 CIRCUITS



'LS37, 'LS40 CIRCUITS



'S37, 'S40 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '128 MIN	'128 NOM	'128 MAX	SERIES 54S / SERIES 74S 'S140 MIN	'S140 NOM	'S140 MAX	UNIT
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−29			−40	mA
	74 Family			−42.4			−40	
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '128 MIN	'128 TYP‡	'128 MAX	SERIES 54S / SERIES 74S 'S140 MIN	'S140 TYP‡	'S140 MAX	UNIT
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	54 Family	2.4	3.4					V
				74 Family	2.4	3.4					
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = −13.2 mA		2.4						
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = MAX		2						
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	54 Family				2.5	3.4		
				74 Family				2.7	3.4		
			V_{CC} = MIN, V_{IL} = 0.5 V, R_Q = 50 Ω to GND					2			
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.26	0.4			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−70		−180	−50		−225	mA
I_{CC}	Supply current, Total, outputs high	7	V_{CC} = MAX			12	21		10	18	mA
	Supply current, Total, outputs low					33	57		25	44	
	Supply current, Average per gate		V_{CC} = 5 V, 50% duty cycle			5.63			8.75		

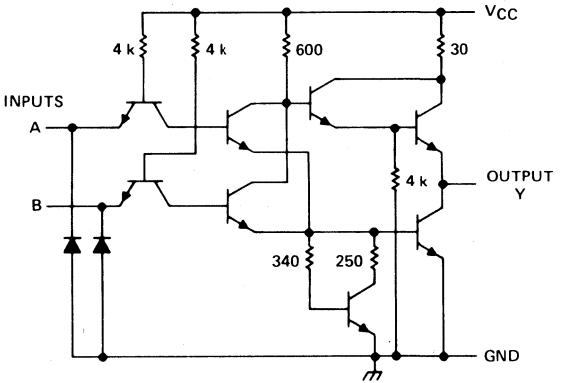
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for '128 and −18 mA for 'S140.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

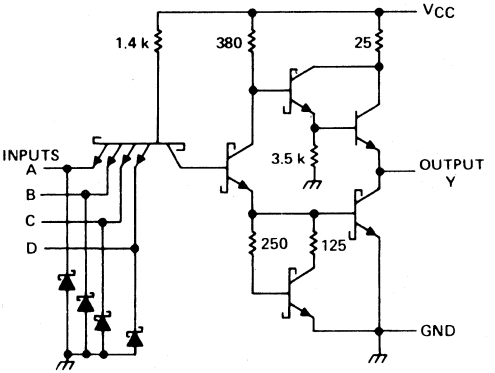
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'128	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'S140	C_L = 50 pF, R_L = 93 Ω		4	6.5		4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each driver)



'128 CIRCUITS



'S140 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54, SERIES 54LS SERIES 74, SERIES 74LS						SERIES 54 SERIES 74						UNIT
			'06, '07			'16, '17			'26			'33, '38			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}					30			15			15			5.5	V
Low-level output current, I_{OL}		54 Family			30			30			16			48	mA
		74 Family			40			40			16			48	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54' SERIES 74'												UNIT
					'06, '07			'16, '17			'26			'33, '38			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5			−1.5			−1.5	V
V_{IK}	('LS')		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5							
I_{OH}	High-level output current	1	V_{CC} = MIN, V_I = ▲	V_{OH} = 12 V									50				μA
				V_{OH} = MAX			250			250			1000			250	
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_I = ▲	I_{OL} = 16 mA			0.4			0.4			0.4				V
				I_{OL} = MAX			0.7			0.7			0.4			0.4	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_{IH} = 2.4 V				40			40			40			40	μA
I_{IH}	('LS')		V_{CC} = MAX, V_{IH} = 2.7 V				20			20							
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−1.6			−1.6			−1.6	mA
I_{IL}	('LS')						−0.2			−0.2							
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page												mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

▲ The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'06, '16	30	48	32	51	5.17
'LS06, 'LS16	9	18	35	60	3.67
'07, '17	29	41	21	30	4.17
'LS07, 'LS17	7	14	25	45	2.67
'26	4	8	12	22	2.00
'33	12	21	33	57	5.63
'38	5	8.5	34	54	4.88

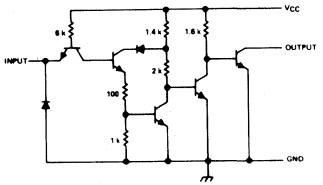
¶Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

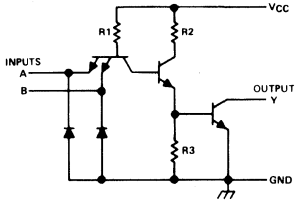
TYPE	TEST CONDITIONS▲	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'06, '16	C_L = 15 pF, R_L = 110 Ω	10	15	15	23
'07, '17		6	10	20	30
'LS06, 'LS16		7	15	10	20
'LS07, 'LS17		6	10	18	30
'26	C_L = 15 pF, R_L = 1 kΩ	16	24	11	17
'33	C_L = 50 pF, R_L = 133 kΩ	10	15	12	18
	C_L = 150 pF, R_L = 133 kΩ	15	22	16	24
'38	C_L = 45 pF, R_L = 133 kΩ	14	22	11	18

▲ Load circuit and voltage wafeforms are shown on page 3-10.

schematics (each gate)

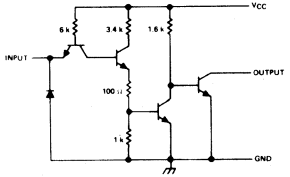


'06, '16 CIRCUITS

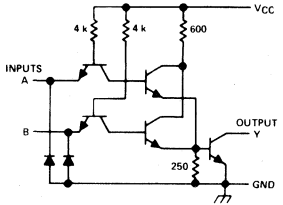


CIRCUITS	R1	R2	R3
'26	4 kΩ	1.6 kΩ	1 kΩ
'38	4 kΩ	600 Ω	400 Ω

'26, '38 CIRCUITS



'07, '17 CIRCUITS



'33 CIRCUITS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54LS' / SERIES 74LS'									SERIES 54S' / SERIES 74S'			UNIT
		'LS26			'LS33			'LS38			'S38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				15			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			4			12			12			60	mA
	74 Family			8			24			24			60	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54LS' / SERIES 74LS'						SERIES 54S' / SERIES 74S'			UNIT
						'LS26			'LS33			'LS38			'S38			
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.7			0.7			0.7			0.8	V
					74 Family			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = @18 mA					−1.5			−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_I = ▲		V_{OH} = 12 V			50										μA
					V_{OH} = MAX			1000			250			250			250	
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_I = ▲	I_{OL} = MAX	54 Family	0.25		0.4	0.25		0.4	0.25		0.4			0.5	V
					74 Family	0.35		0.5	0.35		0.5	0.35		0.5			0.5	
				I_{OL} = 4 mA	Series 74LS'	0.25		0.4										
				I_{OL} = 12 mA					0.25		0.4	0.25		0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V												1	mA
					V_I = 7 V			0.1			0.1			0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.7 V			20			20			20			100	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−0.4			−0.4			−0.4				mA
					V_{IL} = 0.5 V												−4	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'LS26	0.8	1.6	2.4	4.4	0.4
'LS33	1.8	3.6	6.9	13.8	1.09
'LS38	0.9	2	6	12	0.86
'S38	20	36	46	80	8.25

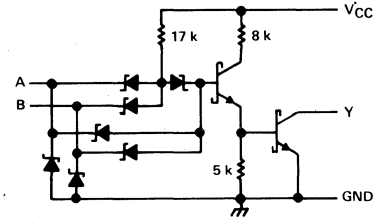
¶Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

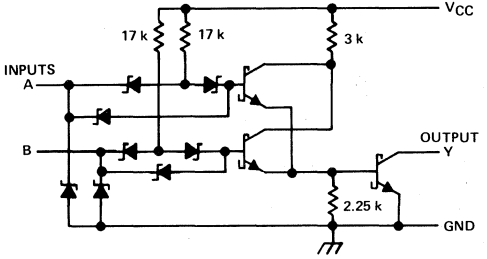
TYPE	TEST CONDITIONS#		t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
			TYP	MAX	TYP	MAX
'LS26	C_L = 15 pF,	R_L = 2 kΩ	17	32	15	28
'LS33	C_L = 45 pF,	R_L = 667 Ω	20	32	18	28
'LS38			20	32	18	28
'S38	R_L = 93 Ω	C_L = 50 pF	6.5	10	6.5	10
		C_L = 150 pF	9		8.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

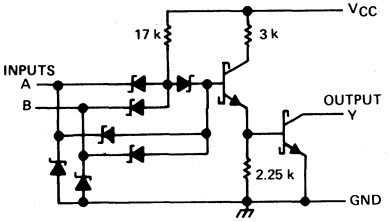
schematics (each gate)



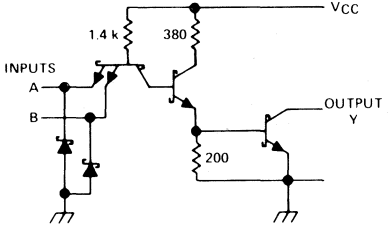
'LS26 CIRCUITS



'LS33 CIRCUITS



'LS38 CIRCUITS



'S38 CIRCUITS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '32			SERIES 54LS / SERIES 74LS 'LS32			SERIES 54S / SERIES 74S 'S32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400			−1000	μA
Low-level output current, I_{OL}	54 Family			16			4			20	mA
	74 Family			16			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '32			SERIES 54LS / SERIES 74LS 'LS32			SERIES 54S / SERIES 74S 'S32			UNIT
							MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2				2			2			2			V
V_{IL}	Low-level input voltage		1, 2			54 Family			0.8			0.7			0.8	V
						74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
						74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IL} = V_{IL} max	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
						74 Family		0.2	0.4		0.35	0.5			0.5	
					I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage		4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
						V_I = 7 V						0.1				
I_{IH}	High-level input current		4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
						V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current		5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6			−0.4				mA
						V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
						74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	Total, outputs high	7	V_{CC} = MAX				15	22		3.1	6.2		18	32	mA
		Total, outputs low						23	38		4.9	9.8		38	68	
		Average per gate		V_{CC} = 5 V,	50% duty cycle			4.75			1.0			7		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

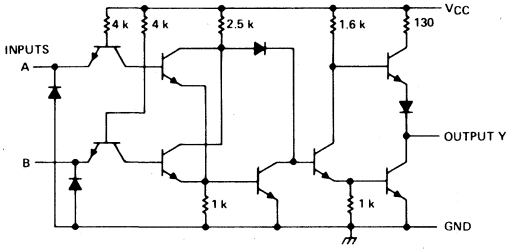
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of the short-circuit should be less than one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

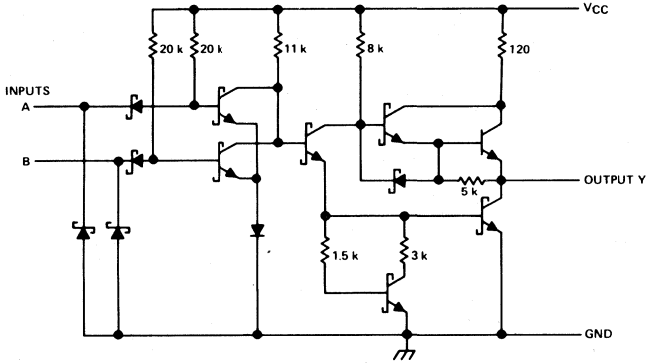
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
'LS32	C_L = 15 pF, R_L = 2 kΩ		14	22		14	22
'S32	C_L = 15 pF, R_L = 280 Ω		4	7		4	7
	C_L = 50 pF, R_L = 280 Ω		5			5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

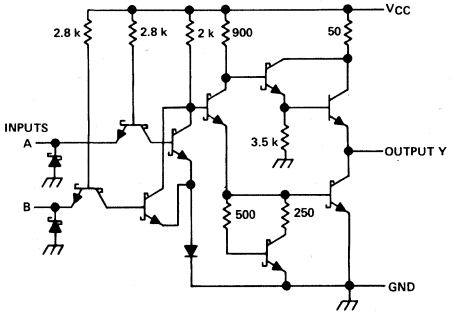
schematics (each gate)



'32 CIRCUITS



'LS32 CIRCUITS



'S32 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '51, '54			SERIES 54LS SERIES 74LS 'LS51, 'LS54, 'LS55			SERIES 54S SERIES 74S 'S51, 'S64			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		54 Family			400			400			1000	μA
		74 Family			400			400			1000	
Low-level output current, I_{OL}		54 Family			16			4			20	mA
		74 Family			16			8			20	
Operating free-air temperature, T_A		54 Family	55		125	55		125	55		125	°C
		74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 SERIES 74 '51, '54			SERIES 54LS SERIES 74LS 'LS51, 'LS54, 'LS55			SERIES 54S SERIES 74S 'S51, 'S64			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §‡				−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = $V_{IL\ max}$, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.35	0.5			0.5	
				I_{OL} = 4 mA	Series 74LS					0.25	0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.3 V										mA
					V_{IL} = 0.4 V			−1.6			−0.4				
					V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		54 Family	−20		−55	−20		−100	−40		−100	mA
					74 Family	−18		−55	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.

♦ Not more than one output should be shorted at a time, and for SN54LS'/SN74LS', and SN54S'/SN74S', duration of the short-circuit should not exceed one second.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per AOI gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'51	4	8	7.4	14	2.85
'54	4	8	5.1	9.5	4.55
'LS51	0.8	1.6	1.4	2.8	0.55
'LS54	0.8	1.6	1.0	2	0.9
'LS55	0.4	0.8	0.7	1.3	0.55
'S51	8.2	17.8	13.6	22	5.45
'S64	7	12.5	8.5	16	7.75

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

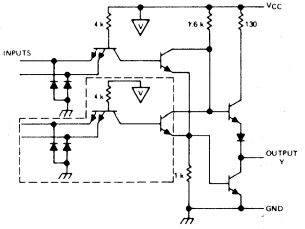
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'51, '54	C_L = 15 pF, R_L = 400 Ω		13	22		8	15
'LS51, 'LS55	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
'LS54	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
'S51, 'S64	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5.5	

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

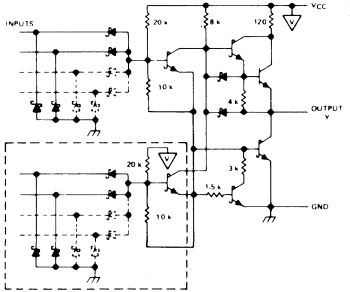
schematics (each gate)

The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

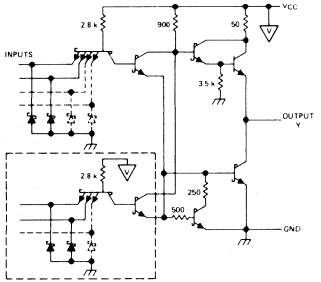
Resistor values shown are nominal and in ohms.



'51, '54 CIRCUITS



'LS51, 'LS54, 'LS55 CIRCUITS



'S51, 'S64 CIRCUITS

recommended operating conditions

	SN54S65			SN74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	'S65			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2		2			V
V_{IL}	Low-level input voltage	1, 2				0.8	V
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.7 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, output high	7	V_{CC} = MAX		6	11	mA
I_{CCL}	Supply current, output low	7	V_{CC} = MAX		8.5	16	mA

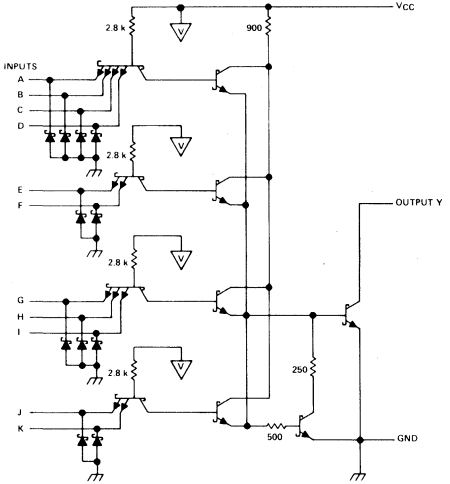
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS#	'S65			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF, R_L = 280 Ω		8		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		6.5		ns

#Load circuit and voltage waveforms are shown on page 3-10.

schematic



Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '125, '126, '425, '426			SERIES 54LS / SERIES 74LS 'LS125A, 'LS126A			SERIES 54S / SERIES 74S 'S134			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−2			−1			−2	mA
	74 Family			−5.2			−2.6			−6.5	
Low-level output current, I_{OL}	54 Family			16			12			20	mA
	74 Family			16			24			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			SERIES 54 / SERIES 74 '125, '126, '425, '426			SERIES 54LS / SERIES 74LS 'LS125A, 'LS126A			SERIES 54S / SERIES 74S 'S134			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.7			0.8	V
					74 Family			0.8			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN,	I_I = §				−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.3		2.4			2.4	3.4		V
					74 Family	2.4	3.1		2.4			2.4	3.2		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = MAX	54 Family			0.4		0.25	0.4			0.5	V
					74 Family			0.4		0.35	0.5			0.5	
				I_{OL} = 12mA	Series 74LS					0.25	0.4				
I_{OZ}	Off-state (high-impedance state) output current	19	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max		V_O = 2.4 V			40			20			50	μA
					V_O = 0.4 V			−40			−20				
					V_O = 0.5 V									−50	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX		V_I = 5.5 V			1						1	mA
					V_I = 7 V						0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40							μA
					V_{IH} = 2.7 V						20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX		V_{IL} = 0.4 V			−1.6							mA
				A inputs	V_{IL} = 0.4 V						−0.4				
				C inputs							−0.2				
					V_{IL} = 0.5 V									−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		54 Family	−30		−70	−40		−225	−40		−100	mA
					74 Family	−28		−70	−40		−225	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page									mA

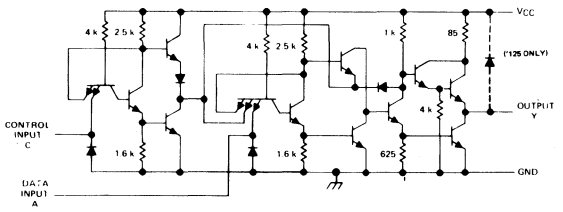
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of the short circuit should not exceed one second.

supply current¶

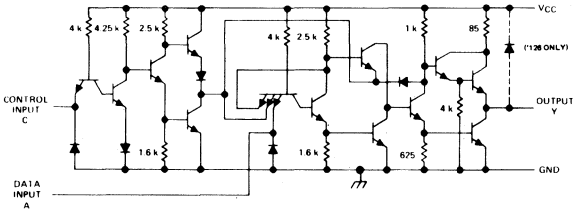
TYPE	TEST CONDITIONS		I_{CC} (mA)		
	DATA INPUTS	OUTPUT CONTROLS	MIN	TYP	MAX
'125, '425	0 V	4.5 V		32	54
'126, '426	0 V	0 V		36	62
'LS125A	0 V	4.5 V		11	20
'LS126A	0 V	0 V		12	22
'S134	0 V	0 V		7	13
	5 V	0 V		9	16
	5 V	5 V		14	25

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



'125, '425 CIRCUITS



'126, '426 CIRCUITS

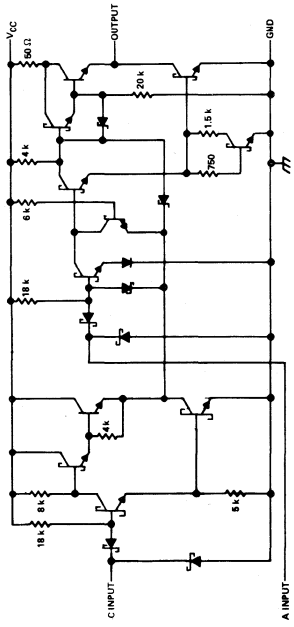
Resistor values shown are nominal and in ohms.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

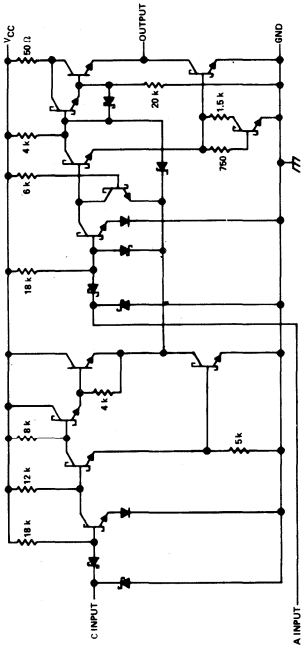
PARAMETER		SERIES 54/74				SERIES 54LS/74LS					SERIES 54S/74S			UNIT
		TEST CONDITIONS#	'125, '425 TYP	'125, '425 MAX	'126, '426 TYP	'126, '426 MAX	TEST CONDITIONS#	'LS125A TYP	'LS125A MAX	'LS126A TYP	'LS126A MAX	TEST CONDITIONS#	'S134 TYP	'S134 MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 667 Ω	8	13	8	13	C_L = 45 pF, R_L = 667 Ω	9	15	9	15	C_L = 15 pF, R_L = 280 Ω	4	6	ns
												C_L = 50 pF, R_L = 280 Ω	5.5		
t_{PHL}	Propagation delay time, high-to-low-level output		12	18	12	18		7	18	8	18	C_L = 15 pF, R_L = 280 Ω	5	7.5	ns
												C_L = 50 pF, R_L = 280 Ω	7		
t_{PZH}	Output enable time to high level		11	17	11	18		12	20	16	25	C_L = 50 pF, R_L = 280 Ω	13	19.5	ns
t_{PZL}	Output enable time to low level		16	25	16	25		15	25	21	35		14	21	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, R_L = 667 Ω	5	8	10	16	C_L = 5 pF, R_L = 667 Ω		20		25	C_L = 5 pF, R_L = 280 Ω	5.5	8.5	ns
t_{PLZ}	Output disable time from low level		7	12	12	18			20		25		9	14	ns

#Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

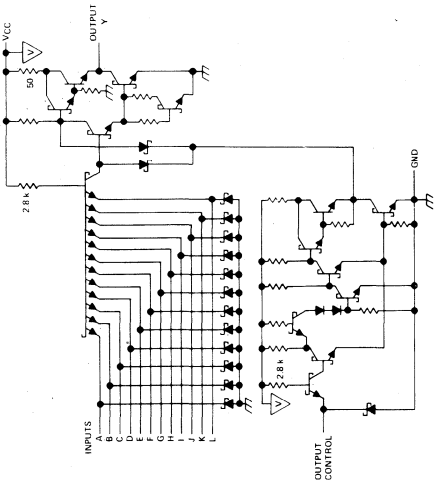
schematics (each gate)



'LS125A CIRCUITS



'LS126A CIRCUITS



'S134 CIRCUITS

Resistor values shown are nominal and in ohms.

6

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '365A, '366A '367A, '368A			SERIES 54LS SERIES 74LS 'LS365A, 'LS366A 'LS367A, 'LS368A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−2			−1	mA
	74 Family			−5.2			−2.6	
Low-level output current, I_{OL}	54 Family			32			12	mA
	74 Family			32			24	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '365A, '366A '367A, '368A			SERIES 54LS SERIES 74LS 'LS365A, 'LS366A 'LS367A, 'LS368A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.7	V
				74 Family			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.5	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.3		2.4	3.3		V
				74 Family	2.4	3.1		2.4	3.1		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OL} = MAX,	54 Family			0.4		0.25	0.4	V
				74 Family			0.4		0.35	0.5	
			I_{OL} = 12 mA	Series 74LS					0.25	0.4	
I_{OZ}	Off-state (high-impedance state) output current	19	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.4 V			40			20	µA
				V_O = 0.4 V			−40			−20	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX	V_I = 5.5 V			1				mA
				V_I = 7 V						0.1	
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				µA
				V_{IH} = 2.7 V						20	
I_{IL}	Low-level input current, A inputs		V_{CC} = MAX, V_I = 0.5 V, Either $\overline{G}$ input at 2 V				−40			−20	µA
	Low-level input current, A inputs		V_{CC} = MAX, V_I = 0.4 V, Both $\overline{G}$ inputs at 0.4 V				−1.6			−0.4	mA
	Low-level input current, $\overline{G}$ inputs		V_{CC} = MAX, V_I = 0.4 V,				−1.6			−0.2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−40		−130	−40		−225	mA
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page						mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS', SN54S/SN74S'.

♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS' and SN54S'/SN74S', duration of output short-circuit should not exceed one second.

supply current¶

TYPE	DATA INPUTS	OUTPUT CONTROLS	I_{CC} (mA) TYP	MAX
'365A, '367A	0 V	4.5 V	65	85
'366A, '368A	0 V	4.5 V	59	77
'LS365A, 'LS367A	0 V	4.5 V	14	24
'LS366A, 'LS368A	0 V	4.5 V	12	21

¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

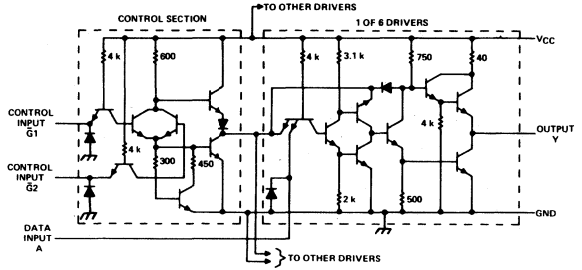
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 1

PARAMETER*	TEST CONDITIONS	SERIES 54/74 '365A, '367A TYP	'365A, '367A MAX	'366A, '368A TYP	'366A, '368A MAX	TEST CONDITIONS	SERIES 54LS/74LS 'LS365A, 'LS367A TYP	'LS365A, 'LS367A MAX	'LS366A, 'LS368A TYP	'LS366A, 'LS368A MAX
t_{PLH}	C_L = 50 pF, R_L = 400 Ω		16		17	C_L = 45 pF, R_L = 667 Ω	10	16	7	15
t_{PHL}			22		16		9	22	12	18
t_{PZH}			35		35		19	35	18	35
t_{PZL}			37		37		24	40	28	45
t_{PHZ}	C_L = 5 pF, R_L = 400 Ω		11		11	C_L = 5 pF, R_L = 667 Ω		30		32
t_{PLZ}			27		27			35		35

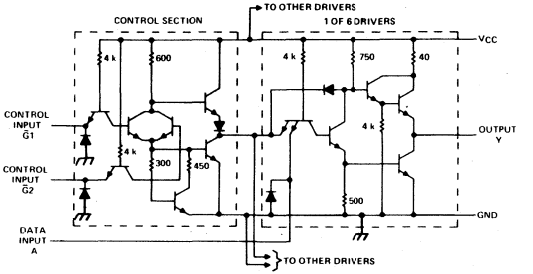
*t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

NOTE 1: Load circuits and voltage waveforms are shown on pages 3-10 and 3-11.

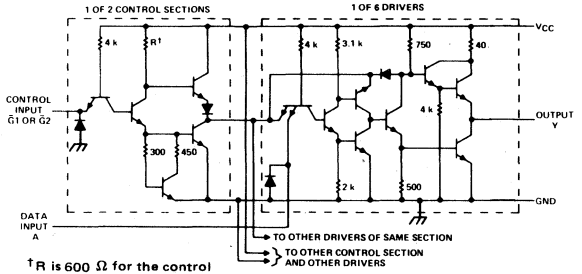
schematics



'365A CIRCUITS

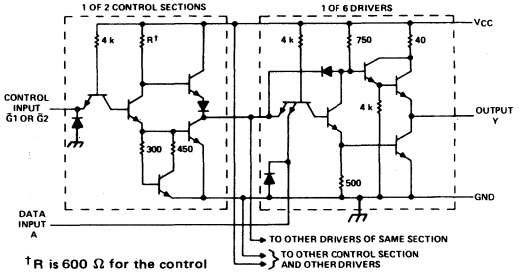


'366A CIRCUITS



†R is 600 Ω for the control section associated with $\overline{G}1$ and 900 Ω for the control section associated with $\overline{G}2$.

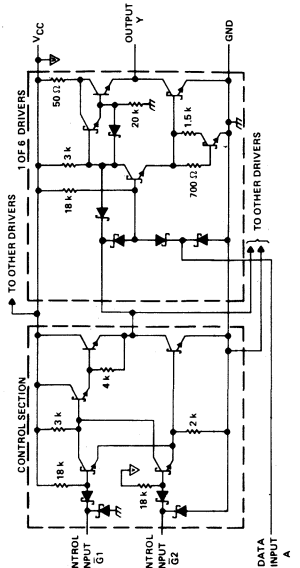
'367A CIRCUITS



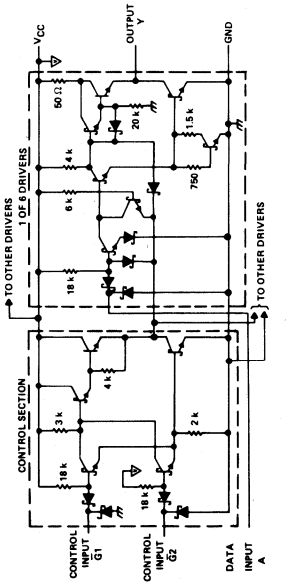
†R is 600 Ω for the control section associated with $\overline{G}1$ and 900 Ω for the control section associated with $\overline{G}2$.

'368A CIRCUITS

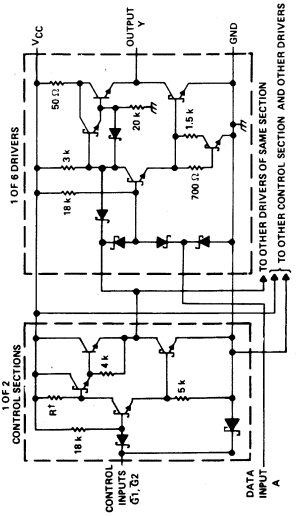
Resistor values shown are nominal and in ohms.



'LS366A CIRCUITS

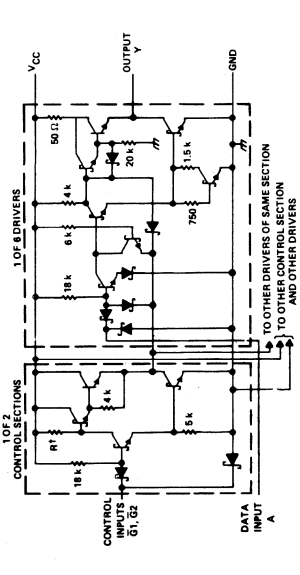


'LS365A CIRCUITS



'LS368A CIRCUITS

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with $\overline{G2}$.



'LS367A CIRCUITS

† R is 5 kΩ for the control section associated with G1 and 8 kΩ for the control section associated with $\overline{G2}$.

Resistor values shown are nominal and in ohms

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74						UNIT
		'23			'50, '53			
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400	μA
Low-level output current, I_{OL}	54 Family			16			16	mA
	74 Family			16			16	
Operating free-air temperature range, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

The '23, '50, and '53 are designed for use with up to four '60 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74						UNIT
					'23			'50, '53			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		1, 2			2			2			V
V_{IL} Low-level input voltage		1, 2					0.8			0.8	V
V_{IK} Input clamp voltage		3	V_{CC} = MIN, I_I = §				−1.5			−1.5	V
V_{OH} High-level output voltage		1	V_{CC} = MIN, V_I = ▲,	I_{OH} = MAX	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		2	V_{CC} = MIN, V_I = ▲,	I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	Data input	4	V_{CC} = MAX, V_{IH} = 2.4 V				40			40	μA
	Strobe of '23						160				
I_{IL} Low-level input current	Data inputs	5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−1.6	mA
	Strobe of '23						−6.4				
I_{OS} Short-circuit output current◆		6	V_{CC} = MAX	54 Family	−20		−55	−20		−55	mA
				74 Family	−18		−55	−18		−55	
I_{CC} Supply current		7	V_{CC} = MAX		See table on next page						mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for SN54'/SN74'
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.
◆Not more than one output should be shorted at a time.

electrical characteristics using expander inputs, V_{CC} = MIN, T_A = MIN (unless otherwise noted)

TYPE	$I_{\overline{X}}$ (mA) (I_X for 'H52) Expander current			$V_{BE(Q)}$ (V) Base-emitter voltage of output transistor Q			V_{OH} (V) High-level output voltage			V_{OL} (V) Low-level output voltage		
	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX
SN5423	$V_{\overline{X}X}$ = 0.4 V,		−3.5	$I_X + I_{\overline{X}}$ = 410 μA,			I_X = 150 μA,			$I_X + I_{\overline{X}}$ = 300 μA,		
SN5450	I_{OL} = 16 mA,		−2.9	$R_{\overline{X}X}$ = 0,		1.1	$I_{\overline{X}}$ = −150 μA,	2.4	3.4	$R_{\overline{X}X}$ = ▲		0.2 0.4
SN5453	See Figure 10		−2.9	I_{OL} = 16 mA, See Figure 11			I_{OH} = −400 μA, See Figure 12			I_{OL} = 16 mA, See Figure 11		
SN7423	$V_{\overline{X}X}$ = 0.4 V,		−3.8	$I_X + I_{\overline{X}}$ = 620 μA,			I_X = 270 μA,			$I_X + I_{\overline{X}}$ = 430 μA,		
SN7450	I_{OL} = 16 mA,		−3.1	$R_{\overline{X}X}$ = 0,		1	$I_{\overline{X}}$ = −270 μA,	2.4	3.4	$R_{\overline{X}X}$ = ▲		0.2 0.4
SN7453	See Figure 10		−3.1	I_{OL} = 16 mA, See Figure 11			I_{OH} = −400 μA, See Figure 12			I_{OL} = 16 mA, See Figure 11		

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

▲ R_{XX} equals 114Ω for SN5423, 138Ω for SN5450 and SN5453, 105Ω for SN7423, and 130Ω for SN7450 and SN7453.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'23	8	16	10	19	4.5
'50	4	8	7.4	14	2.85
'53	4	8	5.1	9.5	4.55

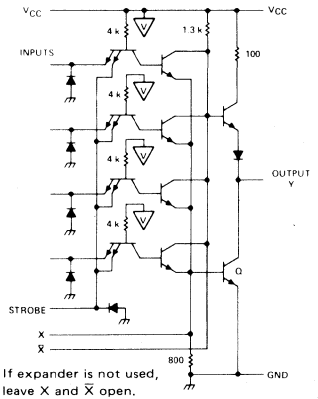
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'23, '50, '53	C_L = 15 pF, R_L = 400 Ω, Expander pins open	13	22	8	15
'50	C_L = 15 pF, R_L = 400 Ω, From input of '60 expander	15	30	10	20

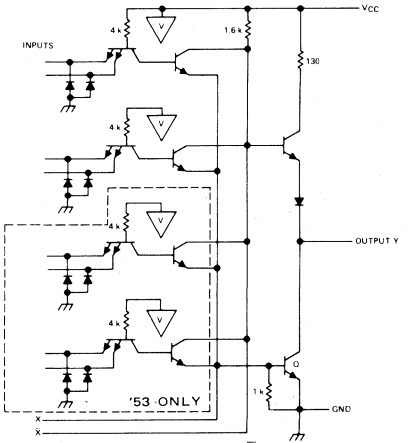
#Load circuit and voltage waveforms are shown on page 3-10.

schematics (each gate)



If expander is not used, leave X and $\overline{X}$ open.

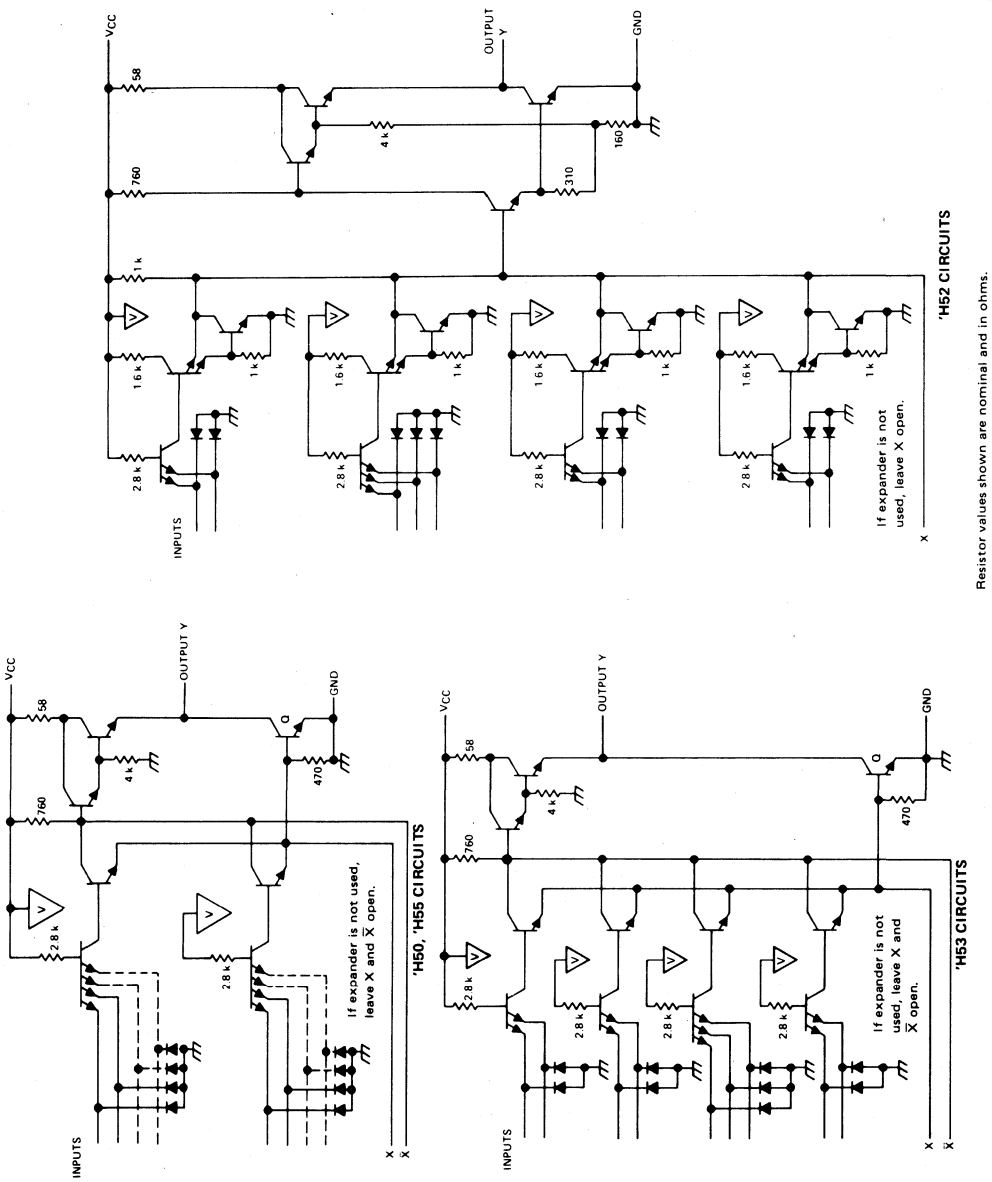
'23 CIRCUITS



If expander is not used, leave X and $\overline{X}$ open.

'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.



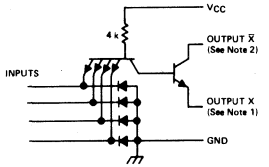
Phased out types!

recommended operating conditions

	SN5460			SN7460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

The '23, '50, and '53 are designed for use with up to four '60 expanders.

schematic (each gate)



'60 CIRCUITS

NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to X̄ inout of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	SN5460 TEST CONDITIONS	SN5460 MIN	SN5460 TYP‡	SN5460 MAX	SN7460 TEST CONDITIONS	SN7460 MIN	SN7460 TYP‡	SN7460 MAX	UNIT
V_{IH}	High-level input voltage	15		2				2			V
V_{IL}	Low-level input voltage	16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 3.5 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 3.8 mA, T_A = 0°C			0.4	V
$I_{X(on)}$	On-state expander current	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−0.3			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−0.43			mA
$I_{\overline{X}(off)}$	Off-state expander current	16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = −55°C			150	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = 0°C			270	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			40	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−1.6	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Phased out types!

recommended operating conditions

	SN54H60 SN54H62			SN74H60 SN74H62			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

See schematics next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	SN54H60, SN54H62 TEST CONDITIONS	MIN	TYP‡	MAX	SN74H60, SN74H62 TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		15		2				2			V
V_{IL}	Low-level input voltage		16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 5.85 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 6.3 mA, T_A = 0°C			0.4	V
				V_{CC} = 5.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.85 mA, T_A = 125°C			0.4	V_{CC} = 5.25 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.4 mA, T_A = 70°C			0.4	
$I_{X(on)}$	On-state expander current		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1.1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−470			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−600			μA
$I_{\overline{X}(off)}$	Off-state expander current		16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = −55°C			320	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = 0°C			570	μA
I_I	Input current at maximum input voltage		4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		4	V_{CC} = 5.5 V, V_I = 2.4 V			50	V_{CC} = 5.25 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current		5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	V_{CC} = 5.25 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	'H60	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0,		1.9	3.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.9	3.5	mA
		'H62				3.8	7			3.8	7	
$I_{CC(off)}$	Supply current, expander off	'H60	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		3	4.5	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		3	4.5	mA
		'H62				6	9			6	9	
$C_{\overline{X}}$	Expander output capacitance	'H60		V_{CC}, inputs, and X open; f = 1 MHz		5.4		V_{CC}, inputs, and X open; f = 1 MHz		5.4		pF
		'H62				6.0				6.0		

‡All typical values are at V_{CC} = 5 V (except $C_{\overline{X}}$), T_A = 25°C.

recommended operating conditions

	SN54H61			SN74H61			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

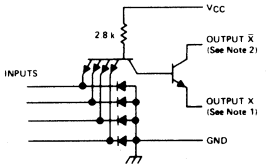
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

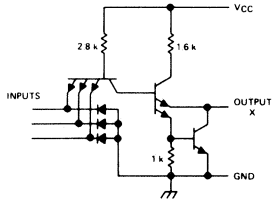
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	17		2			V
V_{IL}	Low-level input voltage	18				0.8	V
$V_{X(on)}$	On-state expander-output voltage	17	V_{CC} = MIN, V_{IH} = 2 V, I_X = 4.5 mA for SN54H61, 5.35 mA for SN74H61, T_A = MIN			1	V
$I_{X(off)}$	Off-state expander current	18	V_{CC} = MIN, V_{IL} = 0.8 V, V_X = 2.2 V, T_A = MAX			50	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V		11	16	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0		5	7	mA
C_X	Expander output capacitance		V_{CC} and inputs open, f = 1 MHz		5.4		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V (except C_X), T_A = 25°C.

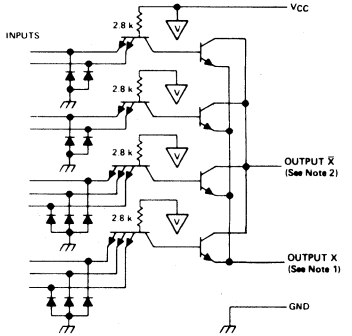
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

NOTES: 1. Connect to X input of 'H50, 'H53, or 'H55 circuit.
2. Connect to X̄ input of 'H50, 'H53, or 'H55 circuit.

Resistor values shown are nominal and in ohms.

recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{su}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_h			5↑			0↓			5↑			6↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1			1			1	mA
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 2.4 V			40			40			40			40			40			40	μA
		Clear				80			80			120			160			160			80	
		Preset				80			80			80			80			160			80	
		Clock				40			80			80			80			40			120	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6			−1.6			−1.6			−1.6	mA
		Clear ★				−3.2			−3.2			−3.2			−4.8			−3.2			−3.2	
		Preset ★				−3.2			−3.2			−1.6			−3.2			−3.2			−3.2	
		Clock				−1.6			−3.2			−3.2			−3.2			−1.6			−4.8	
I_{OS}	Short-circuit output current◆	Series 54	V_{CC} = MAX	−20		−57	−20		−57	−20		−57	−30		−85	−20		−57	−20		−57	mA
		Series 74		−18		−57	−18		−57	−18		−57	−30		−85	−18		−57	−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		13	26		10	20		8.5	15		9	15		20	34		14	20.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆Not more than one output should be shorted at a time.

★Clear is tested with preset high and preset is tested with clear high.

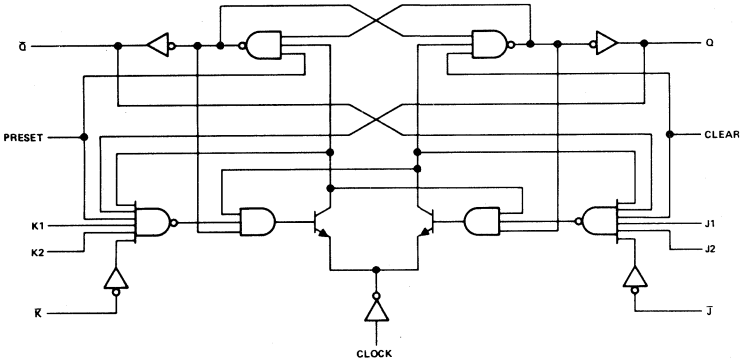
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and is grounded for all the others.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

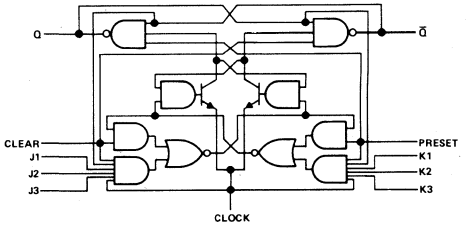
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q	C_L = 15 pF, R_L = 400 Ω, See Note 2			50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\bar{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\bar{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\bar{Q}$			27	50		16	25		14	25		10	16		20	30		12	17	ns
t_{PHL}					18	50		25	40		20	40		18	28		13	20		20	30	

¶f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



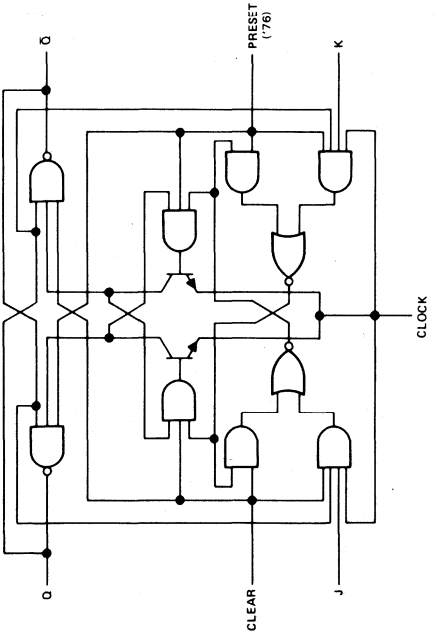
'70—GATED J-K WITH CLEAR AND PRESET



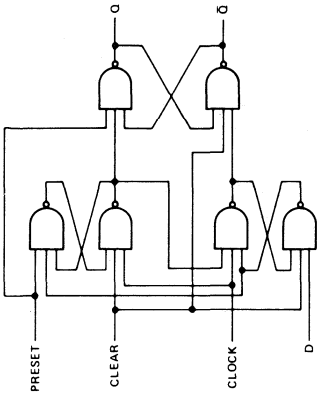
'72—GATED J-K WITH CLEAR AND PRESET

See following pages for:
'73—DUAL J-K WITH CLEAR
'74—DUAL D WITH CLEAR AND PRESET
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR
'109—DUAL J-$\bar{K}$ WITH CLEAR AND PRESET
'110—GATED J-K WITH CLEAR AND PRESET
'111—DUAL J-K WITH CLEAR AND PRESET

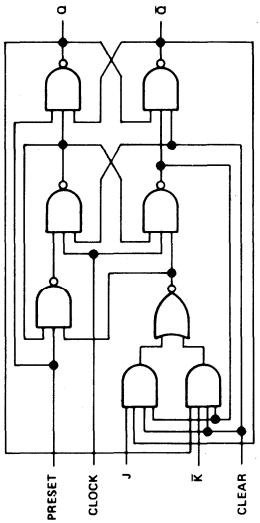
functional block diagrams (continued)



'73—DUAL J-K WITH CLEAR
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR

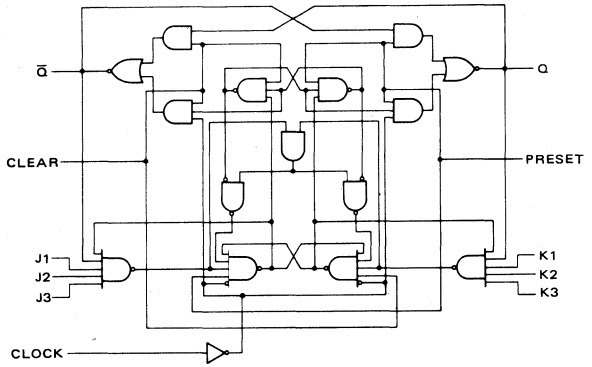


'74—DUAL D WITH CLEAR AND PRESET

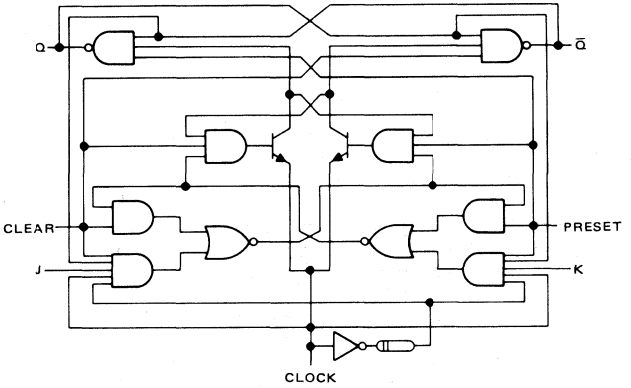


'109—DUAL J-K̄ WITH CLEAR AND PRESET

functional block diagrams (continued)



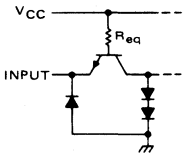
'110—GATED J-K WITH CLEAR AND PRESET



'111—DUAL J-K WITH CLEAR AND PRESET

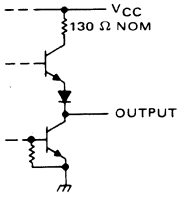
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−3.2 mA	2 kΩ
−4.8 mA	1.3 kΩ

TYPICAL OF ALL OUTPUTS



recommended operating conditions

		SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−1000			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		12			12			15			12			ns
	Clock low		28			28			13.5			28			
	Clear or preset low		16			16			25			16			
Setup time, t_{su}	High-level data		0↑			0↑			10↑			0↑			ns
	Low-level data		0↑			0↑			15↑			0↑			
Hold time, t_h			0↓			0↓			5↑			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA				−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1			1	mA
I_{IH}	High-level input current	D, J, or K	V_{CC} = MAX, V_I = 2.4 V				50			50			50			50	μA
		Clear								100			150			200	
		Preset					150			100			100			100	
		Clock					100			50			100			100	
I_{IL}	Low-level input current	D, J, or K	V_{CC} = MAX, V_I = 0.4 V				−2			−2			−2			−2	mA
		Clear *								−4			−4			−8	
		Preset *					−6			−4			−2			−4	
		Clock					−4			−2			−4			−4	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX		−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1	Series 54H		19	30		16	25		15	21		16	25	mA
				Series 74H		19	30		16	25		15	25		16	25	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
*Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

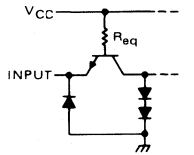
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78			'H74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 25 pF, R_L = 280 Ω, See Note 2	25	30		35	43		MHz
t_{PLH}	Preset (as applicable)	Q			6	13			20	ns
t_{PHL}		$\overline{Q}$			12	24			30	
t_{PLH}	Clear (as applicable)	$\overline{Q}$			6	13			20	ns
t_{PHL}		Q			12	24			30	
t_{PLH}	Clock	Q or $\overline{Q}$			14	21		8.5	15	ns
t_{PHL}					22	27		13	20	

¶ f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

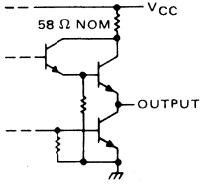
schematics of input and outputs

EQUIVALENT OF EACH INPUT

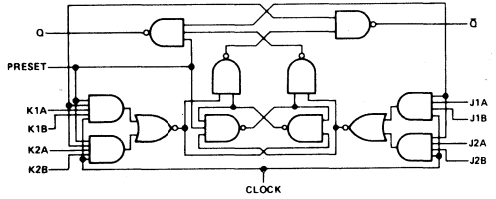


I_{IL} MAX	R_{eq} NOM
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	933 Ω
−8 mA	700 Ω

TYPICAL OF ALL OUTPUTS



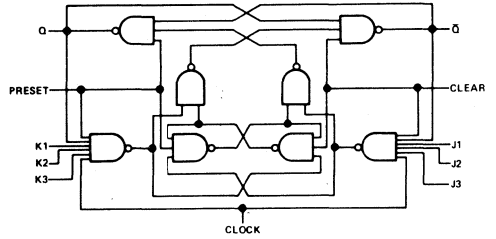
functional block diagrams



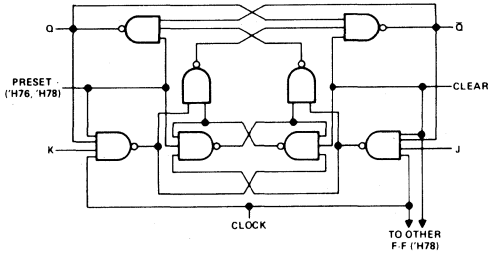
'H71–GATED J-K WITH PRESET

Same functional block diagram as for '74, see page 122.

'H74–DUAL D WITH CLEAR AND PRESET



'H72–GATED J-K WITH CLEAR AND PRESET



'H73–DUAL J-K WITH CLEAR
'H76–DUAL J-K WITH CLEAR AND PRESET
'H78–DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

Phased out types!

recommended operating conditions

		SERIES 54H/74H	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−500			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		10			10			10			10			ns
	Clock low		15			15			15			15			
	Clear or preset low		16			16			16			16			
Setup time, t_{su}	High-level data		10↓			10↓			10↓			10↓			ns
	Low-level data		13↓			13↓			13↓			13↓			
Hold time, t_h			0↓			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			2			2			V
V_{IL} Low-level input voltage					0.8			0.8			0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −500 μA	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH} High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			50			50			50			50	μA
	Clear							100			100			200	
	Preset				100			100						100	
	Clock		0		−1	0		−1	0		−1	0		−1	mA
I_{IL} Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.4 V		−1	−2		−1	−2		−1	−2		−1	−2	mA
	Clear						−1	−2		−1	−2		−2	−4	
	Preset			−1	−2		−1	−2					−1	−2	
	Clock			−3	−4.8		−3	−4.8		−3	−4.8		−6	−9.6	
I_{OS} Short-circuit output current♦		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		20	38		20	38		20	38		20	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

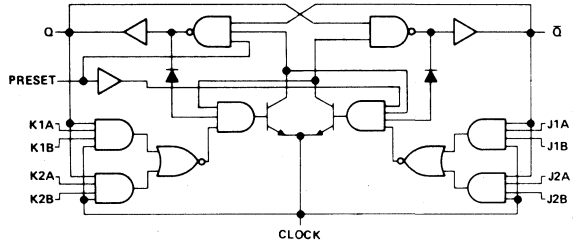
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

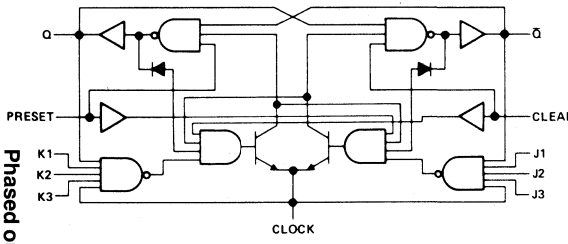
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 25 pF, R_L = 280 Ω, See Note 2	40	50		MHz
t_{PLH}	Preset or clear	Q or $\bar{Q}$			8	12	ns
t_{PHL}	Preset or clear (clock high)	$\bar{Q}$ or Q			15	20	ns
	Preset or clear (clock low)				23	35	
t_{PLH}	Clock	Q or $\bar{Q}$			10	15	ns
t_{PHL}					16	20	

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagrams



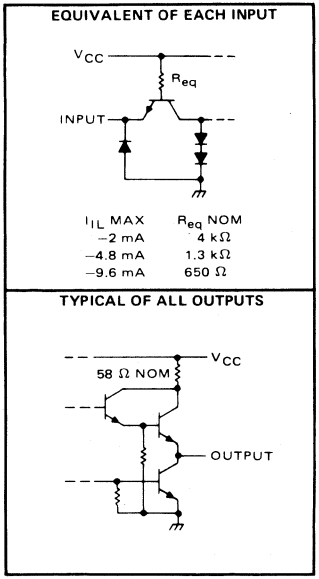
'H101—GATED J-K WITH PRESET

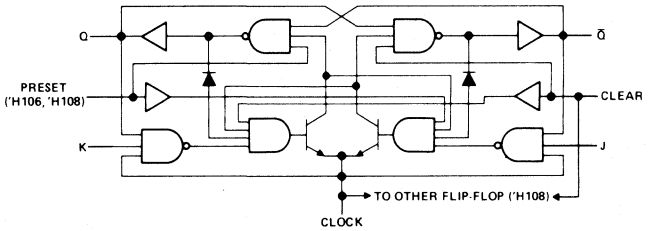


'H102—GATED J-K WITH CLEAR AND PRESET

Phased out types!

schematics of inputs and outputs





'H103—DUAL J-K WITH CLEAR
'H106—DUAL J-K WITH CLEAR AND PRESET
'H108—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SERIES 54LS/74LS	'LS73A, 'LS107A, 'LS113A			'LS74A			'LS76A, 'LS112A			'LS78A, 'LS114A			'LS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54LS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74LS	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−400			−400	μA
Low-level output current, I_{OL}		Series 54LS			4			4			4			4			4	mA
		Series 74LS			8			8			8			8			8	
Clock frequency, f_{clock}			0		30	0		25	0		30	0		30	0		25	MHz
Pulse width, t_w	Clock high		20			25			20			20			25			ns
	Preset or clear low		25			25			25			25			25			
Setup time, t_{su}	High-level data		20↓			20↑			20↓			20↓			35†			ns
	Low-level data		20↓			20↑			20↓			20↓			25†			
Hold time, t_h			0↓			5↑			0↓			0↓			5↑			ns
Operating free-air temperature, T_A		Series 54LS	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74LS	0		70	0		70	0		70	0		70	0		70	

†↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'LS73A, 'LS107A, 'LS113A			'LS74A			'LS76A, 'LS112A			'LS78A, 'LS114A			'LS109A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			2			V
V_{IL}	Low-level input voltage	Series 54LS					0.7			0.7			0.7			0.7			0.7	V
		Series 74LS					0.8			0.8			0.8			0.8			0.8	
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Series 54LS	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
		Series 74LS	V_{IL} = V_{IL} max,			0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
		Series 74LS	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	
I_I	Input current at maximum input voltage	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1			0.1			0.1			0.1	mA
		Clear					0.3			0.2			0.3			0.6			0.2	
		Preset					0.3			0.2			0.3			0.3			0.2	
		Clock					0.4			0.1			0.4			0.8			0.1	
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 2.7 V			20			20			20			20			20	μA
		Clear					60			40			60			120			40	
		Preset					60			40			60			60			40	
		Clock					80			20			80			160			20	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4			−0.4			−0.4			−0.4	mA
		Clear					−0.8			−0.8			−0.8			−1.6			−0.8	
		Preset					−0.8			−0.8			−0.8			−0.8			−0.8	
		Clock					−0.8			−0.4			−0.8			−1.6			−0.4	
I_{OS}	Short-circuit output current♦	Series 54LS	V_{CC} = MAX,	See Note 1	−20		−100	−20		−100	−20		−100	−20		−100	−20		−100	mA
		Series 74LS			−20		−100	−20		−100	−20		−100	−20		−100	−20		−100	
I_{CC}	Supply current (Total)		V_{CC} = MAX,	See Note 2		4	6		4	8		4	6		4	6		4	8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second.

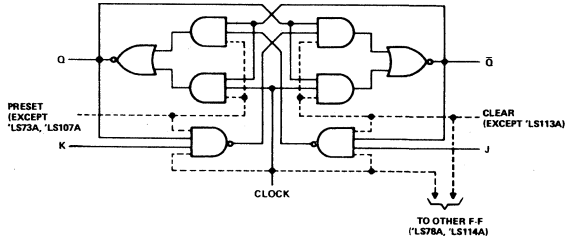
NOTES: 1. For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V_O = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.
2. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS73A,'LS76A,'LS78A, 'LS107A,'LS112A, 'LS113A,'LS114A			'LS74A, 'LS109A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF,	30	45		25	33		MHz
t_{PLH}	Clear, preset, or	Q or $\bar{Q}$	R_L = 2 kΩ,		15	20		13	25	ns
t_{PHL}	clock (as appropriate)		See Note 2		15	20		25	40	ns

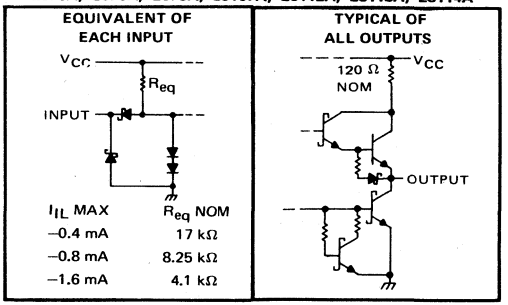
¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagrams and schematics of inputs and outputs

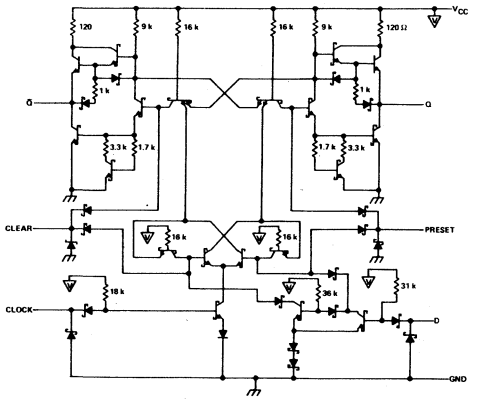


'LS73A, 'LS107A—DUAL J-K WITH CLEAR
'LS76A, 'LS112A—DUAL J-K WITH CLEAR AND PRESET
'LS78A, 'LS114A—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113A—DUAL J-K WITH PRESET

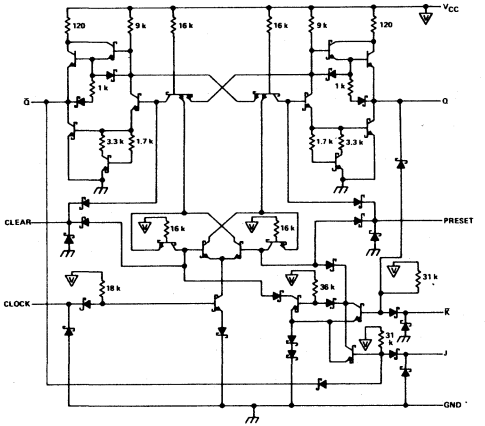
'LS73A, 'LS76A, 'LS78A, 'LS107A, 'LS112A, 'LS113A, 'LS114A



schematics of 'LS74A and 'LS109A



'LS74A—DUAL D WITH CLEAR AND PRESET



'LS109A—DUAL J-$\bar{K}$ WITH CLEAR AND PRESET

recommended operating conditions

		SERIES 54S/74S	'S74			'S112			'S113			'S114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−1			−1			−1			−1	mA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		6			6			6			6			ns
	Clock low		7.3			6.5			6.5			6.5			
	Clear or preset low		7			8			8			8			
Input setup time, t_{su}	High-level data		3↑			3↓			3↓			3↓			ns
	Low-level data		3↑			3↓			3↓			3↓			
Input hold time, t_h			2↑			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54S	−55		125	−55		125	−55		125	−55		125	°C
		Series 74S	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'S74			'S112			'S113			'S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	Series 54S	V_{CC} = MIN, V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74S	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	J, K, or D	V_{CC} = MAX, V_I = 2.7 V			50			50			50			50	μA
		Clear				150			100						200	
		Preset				100			100			100			100	
		Clock				100			100			100			200	
I_{IL}	Low-level input current	J, K, or D	V_{CC} = MAX, V_I = 0.5 V			−2			−1.6			−1.6			−1.6	mA
		Clear ★				−6			−7						−14	
		Preset ★				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 1		15	25		15	25		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

★Clear is tested with preset high and preset is tested with clear high.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

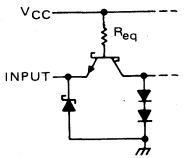
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74			'S112, 'S113, 'S114			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		80	125		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	6		4	7	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			9	13.5		5	7	ns
	Preset or clear (clock low)				5	8		5	7	
t_{PLH}	Clock	Q or $\overline{Q}$			6	9		4	7	ns
t_{PHL}					6	9		5	7	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: *Load circuit and voltage waveforms are shown on page 3-10.*

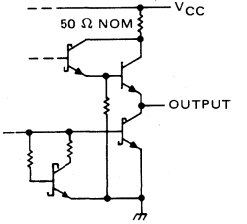
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

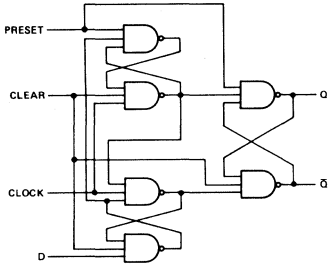


I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω
−7 mA	900 Ω
−8 mA	700 Ω
−14 mA	450 Ω

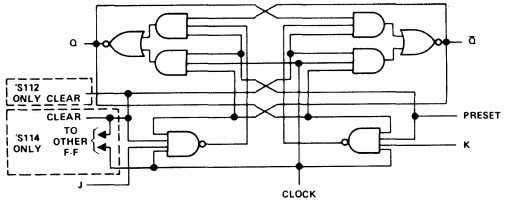
TYPICAL OF ALL OUTPUTS



functional block diagrams



'S74—DUAL D WITH CLEAR AND PRESET



'S112—DUAL J-K WITH CLEAR AND PRESET
'S113—DUAL J-K WITH PRESET
'S114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		54 FAMILY / 74 FAMILY	SN54279 / SN74279			SN54LS279A / SN74LS279A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400	μA
Low-level output current, I_{OL}		54 Family			16			4	mA
		74 Family			16			8	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54279 / SN74279			SN54LS279A / SN74LS279A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level output voltage				2			2			V
V_{IL}	Low-level output voltage			54 Family			0.8			0.7	V
				74 Family			0.8			0.8	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = §					−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{IH} = 2 V	I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4	V
				74 Family		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	Series 74LS					0.35	0.4	
I_I	Input current at maximum input voltage	V_{CC} = MAX		V_I = 5.5 V			1				mA
				V_I = 7 V						0.1	
I_{IH}	High-level input current	V_{CC} = MAX		V_I = 2.4 V			40				μA
				V_I = 2.7 V						20	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V					−1.6			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		54 Family	−18		−55	−20		−100	mA
				74 Family	−18		−57	−20		−100	
I_{CC}	Supply current	V_{CC} = MAX, See note 1				18	30		3.8	7	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS'.
♦Not more than one output should be shorted at a time, and for SN54LS'/SN74LS', duration of the output short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5 V, and all outputs open.

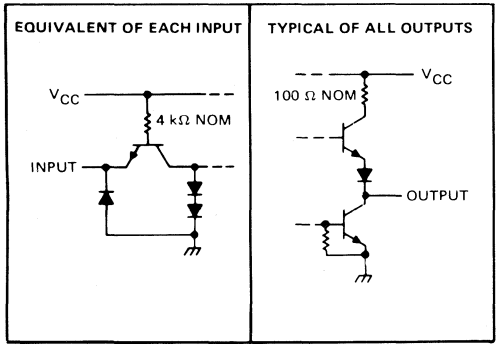
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	279			'LS279			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{S}$ input	C_L = 15 pF, See Notes 2 and 3		12	22		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{S}$ input			9	15		13	21	
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{R}$ input			15	27		15	27	

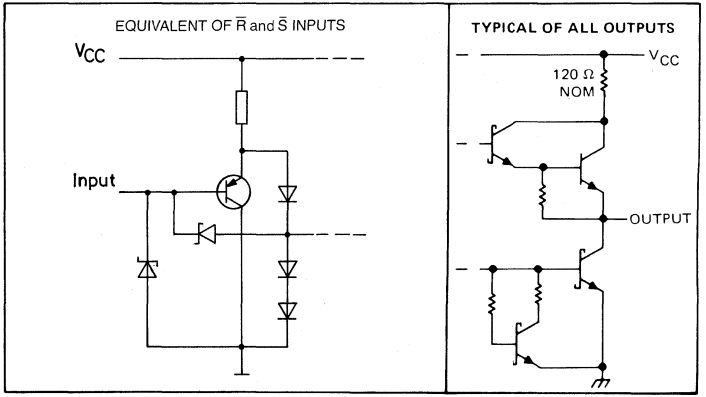
NOTE 2: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.
NOTE 3: R_L = 400 Ω for '279, R_L = 2 kΩ for 'LS279.

schematics of inputs and outputs

'279 CIRCUITS



'LS279 CIRCUITS



TYPES SN54LS18, SN54LS19, SN54LS24, SN74LS18, SN74LS19, SN74LS24 SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

D2627, JANUARY 1981

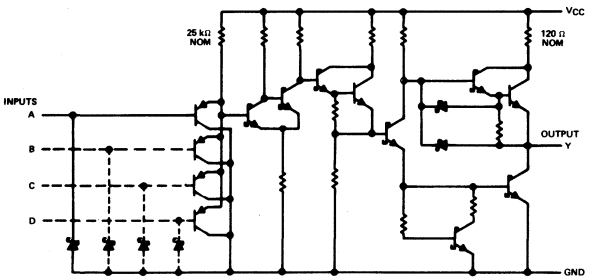
- **Functionally and Mechanically Identical To 'LS13, 'LS14, and 'LS132, Respectively**
- **Improved Line-Receiving Characteristics**
- **P-N-P Inputs Reduce System Loading**
- **Excellent Noise Immunity With Typical Hysteresis of 0.7 V**

description

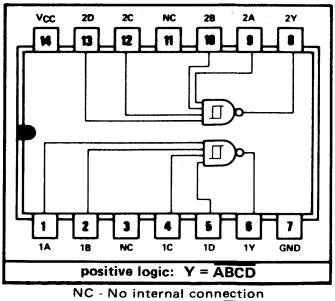
Each circuit functions as a NAND gate or inverter, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals. The hysteresis or backlash, which is the difference between the two threshold levels ($V_{T+} - V_{T-}$), is typically 700 millivolts.

These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

schematic (each gate)



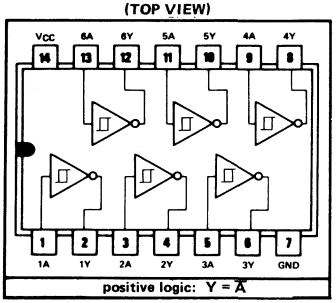
SN54LS18 . . J OR W PACKAGE
SN74LS18 . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{ABCD}$

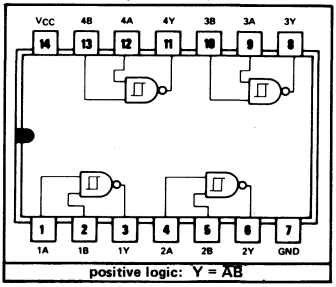
NC - No internal connection

SN54LS19 . . J OR W PACKAGE
SN74LS19 . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A}$

SN54LS24 . . J OR W PACKAGE
SN74LS24 . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54LS'	−55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	V_{CC} = 5 V		1.65	1.85	2.15	1.65	1.85	2.15	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5 V		0.75	1.0	1.25	0.75	1.0	1.25	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5 V		0.4	0.7		0.4	0.7		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = V_{T-min}, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = V_{T+max}	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_{T+}	Input current at positive-going threshold	V_{CC} = 5 V, V_I = V_{T+}			−2	20		−2	20	μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5 V, V_I = V_{T-}			−5	30		−5	30	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.05			−0.05	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = V_O = 0 V		−20		−100	−20		−100	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V	'LS18		3.3	6		3.3	6	mA
			'LS19		9.9	18		9.9	18	
			'LS24		6.6	12		6.6	12	
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 4.5 V	'LS18		5.7	10		5.7	10	mA
			'LS19		17	30		17	30	
			'LS24		11	20		11	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS18			'LS19			'LS24			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Any	Y	R_L = 2 kΩ, C_L = 15 pF		13	20		13	20		13	20	ns
t_{PHL}	Any	Y			33	55		18	30		21	40	ns

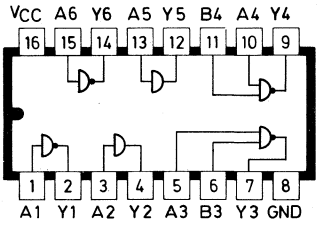
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

TYPES SN54LS31, SN74LS31
DELAY ELEMENTS

- **Delay Elements for Generating Delay Lines**
- **Inverting and Non-Inverting Elements**
- **Buffer NAND Elements Rated at IOL of 12/24 mA**
- **PNP Inputs Reduce Fan-In (IIL = −0.2 mA MAX)**
- **Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Ranges**

SN54LS31...J OR W PACKAGE
SN74LS31...J OR N PACKAGE



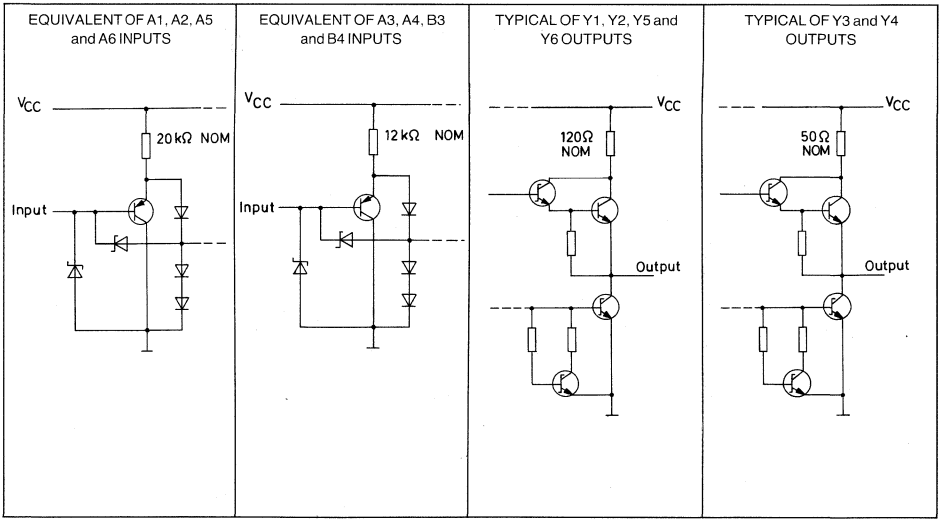
description

These 'LS31 delay elements are intended to provide well-defined delays across both temperature and V_{CC} ranges. Used in cascade, a limitless range of delay gating is possible.

All inputs are PNP with IIL MAX of −0.2 mA. Gates 1, 2, 5, and 6 have standard Low Power Schottky output sink current capability of 4 and 8 mA IOL. Buffers 3 and 4 are rated at 12 and 24 mA.

Delay Element	Logic	Typical Delays TPLH	TPHL	AVG.	Rated IOL
Gates 1 and 6	Inverting	32 ns	23 ns	27.5 ns	4 and 8 mA
Gates 2 and 5	Non-Inverting	45 ns	48 ns	46.5 ns	4 and 8 mA
Buffers 3 and 4	2-Input NAND	6 ns	6 ns	6 ns	12 and 24 mA

schematics of inputs and outputs



Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †			SN54LS31			SN74LS31			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V,	Y3, Y4	I_{OH} = −1.2 mA	2.4	3.1		2.4	3.1		V
		V_{IL} = V_{IL} max	Others	I_{OH} = −400 μA	2.5	3.1		2.7	3.1		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V,	Y3, Y4	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL} max		I_{OL} = 24 mA					0.35	0.5	
			Others	IOL = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V					−0.2			−0.2	mA
I_{CC}	Supply current	I_{CCH}	V_{CC} = MAX, A2, A5 = 4.5 V, all other inputs 0 V			2.3	4		2.3	4	mA
		I_{CCL}	V_{CC} MAX, A2, A5 = 0 V, all other inputs 4.5 V			13	20		13	20	
I_{OS}	Short-circuit output current	V_{CC} = MAX, A3, B4, B4 = 0 V		Y3, Y4	−30		−130	−30		−130	mA
		V_{CC} = MAX, A1, A6 = 0 V, A2, A5 = 4.5 V		Y1, Y2,	−20		−100	−20		−100	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, TA = 25°C.

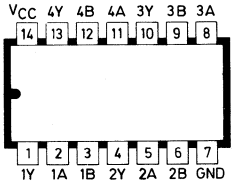
switching characteristics, RL = 667 Ω, CL = 45 pF for Y3 & Y4; RL = 2 KΩ, CL = 15 pF for Y1, Y2, Y5 & Y6.

PARAMETER	FROM (INPUT)	TO OUTPUT)	'LS31 V_{CC} = 5 V TA = 25°C			SN54LS31 V_{CC} = 4.5 V to 5.5 V TA = −55°C to 125°C			SN74LS31 V_{CC} = 4.75 V to 5.25 V TA = 0°C to 70°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TPLH	A1, A6	Y1, Y6		32	50	15		70	22		65	ns
TPHL				23	35	9		50	13		45	ns
TPLH	A2, A5	Y2, Y5		45	70	22		90	31		80	ns
TPHL				48	75	20		105	30		95	ns
TPLH	A3, B3, A4, Y4	Y3, Y4		6	10	2		20	2		15	ns
TPHL				6	10	2		20	2		15	ns

TYPES SN5439, SN7439
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- **Current Sinking Capability up to 80 mA**
- **Guaranteed Fan-Out of 30 Series 54/74 Loads**
- **Package Options Include Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN5439...J PACKAGE
SN7439...N PACKAGE
(TOP VIEW)



SN5439...FC PACKAGE

For chip carrier information, contact the factory.

description

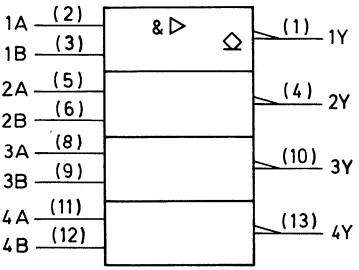
These devices contain four independent 2-input NAND buffers. They perform the boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN5439 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN7439 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

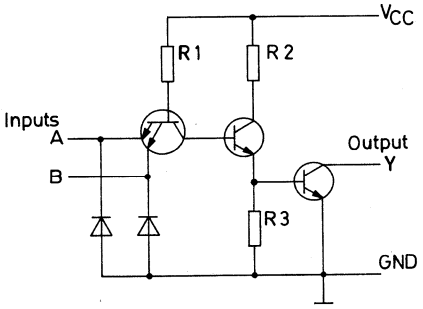
INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic symbol



Pin numbers shown are for J and N packages.

schematics (each gate)



R1	R2	R3
4 kΩ	600 Ω	400 Ω

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN5439 . . . . . −55°C to 125°C
SN7439 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN5439			SN7439			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			48	mA
				60			60	
							80†	
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended limit applies only if V_{CC} is maintained between 4.75 and 5.25 V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN5439			SN7439			UNIT
			MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −12 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			250			250	μA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.4			0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 60 mA			0.5			0.5	
	V_{CC} = 4.75 V,	I_{OL} = 80 mA						0.6	
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−1.6			−1.6	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V			54			54	mA

* All typical values are at V_{CC} = 5 V, T_A = 25°C.

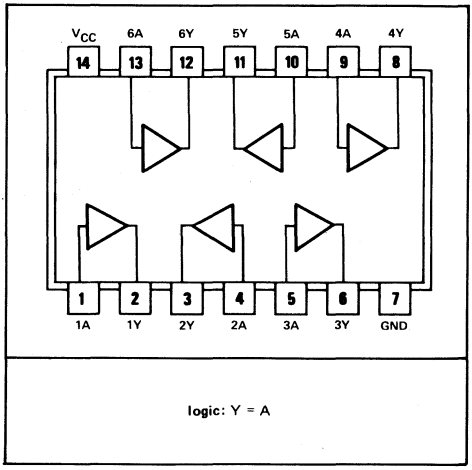
switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 45 pF, R_L = 133 Ω, T_A = 25°C				UNIT
			SN5439		SN7439		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y		22		22	ns
t_{PHL}				18		18	

NOTE 1: For load circuit and voltage waveforms, see page 3-10.

- Translates low-level input current to low-level output voltage
- Translates high-level input current to high-level output voltage
- Interfaces to PLA's or other logic elements that source current but do not sink current
- Operates from a single 5 V supply
- TTL compatible
- Low power dissipation . . .40 mW typical

SN54LS63 . . . J OR W PACKAGE
SN74LS63 . . . J OR N PACKAGE



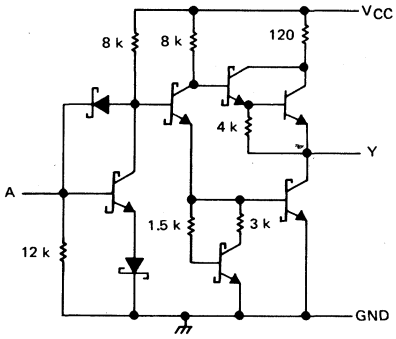
logic: Y = A

description

Each of these Schotty-clamped interface gates is able to discriminate between low-level ($\leq$ 50 μA) and high-level ($\geq$ 200 μA) input currents.

The outputs are fabricated with standard Low-Power Schottky design rules and are compatible with all TTL families.

schematic (each gate)



Resistor values shown are nominal and in ohms.

recommended operating conditions

	SN54LS63			SN74LS63			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			4			8	mA
Input current, I_I			1			1	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS63			SN74LS63			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_I	Input voltage	I_I = 50 μA,	V_{CC} = MIN		0.35	1.05	1.75	0.6	1.05	1.6	V
		I_I = 200 μA,	V_{CC} = MAX		0.6	1.30	2	0.85	1.30	1.8	
V_{OH}	High-level output voltage	V_{CC} = MAX	I_I = 200 μA	I_{OH} = −400 μA,	3.5	3.4		3.2	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_I = 50 μA	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	I_I = 600 μA		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 1			8	16		8	16	mA

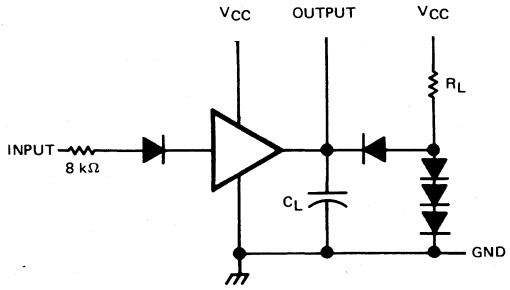
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of output short circuit should not exceed one second.
NOTE 1: I_{CC} is measured with inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propogation delay time, low-to-high-level output	C_L = 15 pF,		27	45	ns
t_{PHL}	Propogation delay time, high-to-low-level output	R_L = 2 kΩ		15	25	ns

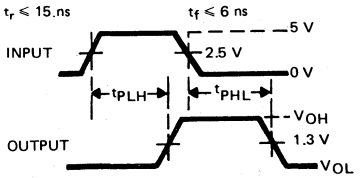
6

PARAMETER MEASUREMENT INFORMATION



NOTES: a. C_L includes probe and jig capacitance
b. All diodes are 1N916 or 1N3064

TEST CIRCUIT



VOLTAGE WAVEFORMS

CIRCUIT TYPES SN54104, SN54105, SN74104, SN74105
GATED J-K MASTER-SLAVE FLIP-FLOPS

featuring

- Buffered Clock Input
- Direct Preset and Clear
- Common JK Gate Input

logic

TRUTH TABLE

INPUT AT t_n			OUTPUT AT t_{n+1}	
JK	J†	K†	Q	$\overline{Q}$
L*	X	X	Q_n	$\overline{Q}_n$
H	L*	L*	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

† SN54104/SN74104: $J = J1 \cdot J2 \cdot J3$,
$K = K1 \cdot K2 \cdot K3$
SN54105/SN74105: $J = J1 \cdot \overline{J2} \cdot J3$,
$K = K1 \cdot \overline{K2} \cdot K3$

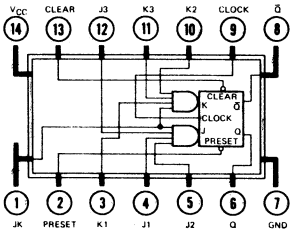
* These low levels must be maintained while the clock is low.

NOTES:
A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
C. H = high, L = low, X = irrelevant.

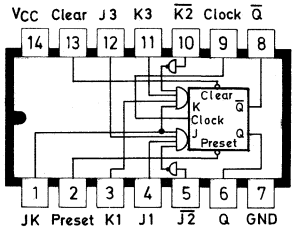
W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

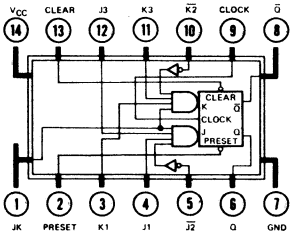
SN54104/SN74104



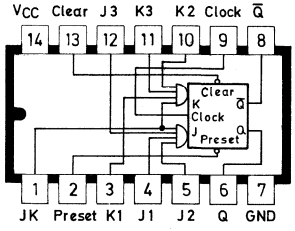
SN54104/SN74104



SN54105/SN74105



SN54105/SN74105



asynchronous inputs: Low input to preset sets Q to the high level.
Low input to clear sets Q to the high level.
Preset and clear are independent of clock.

description

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during the clock-line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

The SN54104/SN74104 includes internal capacitive loading on the J and K input gates and, as the input setup and hold times are lengthened, this circuit displays improved performance in systems where appreciable clock skew is anticipated.

The SN54105/SN74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates than the SN54104/SN74104.

These TTL circuits feature one-volt typical d-c noise margins and are compatible for use with most TTL and DTL families. Full fan-out to 10 normalized Series 54/74 loads is available from the outputs. The SN54104 and SN54105 circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74104 and SN74105 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 8 V
Input voltage (See Note 1) . . . . . −1.5 V to 5.5 V
Voltage applied to any output (See Note 2) . . . . . −0.5 V to V_{CC}
Operating free-air temperature range: SN54104, SN54105 Circuits . . . . . −55°C to 125°C
SN74104, SN74105 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (See Note 1)	SN54104, SN54105		4.5	5	5.5	V
	SN74104, SN74105		4.75	5	5.25	
Operating free-air temperature range	SN54104, SN54105		−55	25	125	°C
	SN74104, SN74105		0	25	70	
Width of low-level clock pulse, $t_{w(clock)}$ (See Figure 112)			15†			ns
Width of preset and clear pulse, $t_{w(preset)}$ and $t_{w(clear)}$			20†			ns
Input release time for low-level data, $t_{(release(L)}$ (See Note 3 and Figure 113)	SN54104, SN74104				10†	ns
	SN54105, SN74105				1†	
Input setup time for high-level data, $t_{setup(H)}$ (See Note 4 and Figure 113)	SN54104, SN74104		35†			ns
	SN54105, SN74105		10†			

NOTES 1. Voltage values are with respect to network ground terminal.
2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.
3. Release time for low-level data is an interval between the release of low-level data and the positive-going edge of the clock pulse; this interval being sufficiently short to ensure recognition of the low-level data.
4. Setup time for high-level data is an interval between the arrival of the high-level data and the positive-going edge of the clock pulse; this interval being sufficiently long to ensure recognition of the high-level data.

† These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

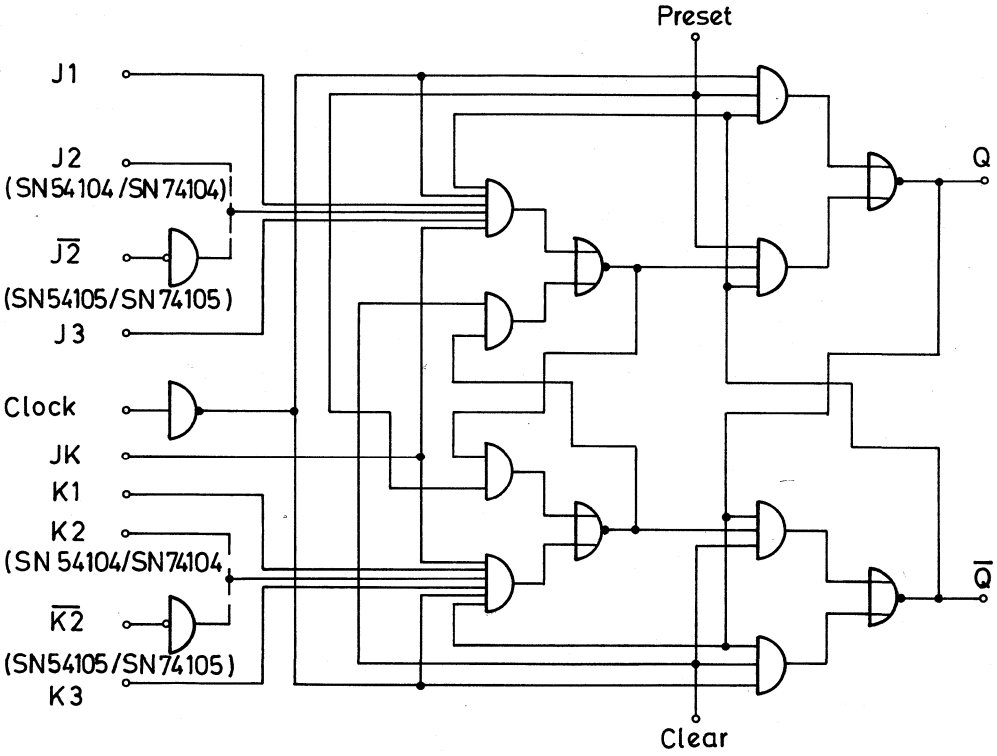
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP*	MAX	UNIT
V_{IH}	High-level input voltage	107 and 108		T_A = MIN	2			V
				T_A = 25°C	1.7			
				T_A = MAX	1.4			
V_{IL}	Low-level input voltage	107 and 108		T_A = MIN			0.8	V
				T_A = 25°C			0.9	
				T_A = MAX			0.8	
V_{OH}	High-level output voltage	107	V_{CC} = MIN,	I_{OH} = −1 mA	2.4	2.7		V
V_{OL}	Low-level output voltage	107	V_{CC} = MAX,	I_{OL} = 17.7 mA		0.2	0.4	V
			V_{CC} = MIN,	I_{OL} = 16 mA		0.2	0.4	
I_{IH}	High-level input current into any input except JK, preset or clear	109	V_{CC} = MIN,	T_A = 25°C		2	40	µA
			V_{CC} = MIN,	T_A = MAX			40	
I_{IH}	High-level input current into JK	109	V_{CC} = MAX,	T_A = 25°C		4	80	µA
			V_I V	T_A = MAX			80	
I_{IH}	High-level input current into preset or clear	109	V_{CC} = MAX,	T_A = 25°C		8	120	µA
			V_I = 4.5 V	T_A = MAX			120	
I_{IL}	Low-level input current into any input except JK, preset, or clear	110	V_{CC} = MAX,	V_I = 0.4 V		−1.1	−1.6	mA
			V_{CC} = MIN,	V_I = 0.4 V		−0.9	−1.45	
I_{IL}	Low-level input current into JK	110	V_{CC} = MAX,	V_I = 0.4 V		−2.2	−3.2	mA
			V_{CC} = MIN,	V_I = 0.4 V		−1.8	−2.9	
I_{IL}	Low-level input current into preset or clear	110	V_{CC} = MAX,	V_I = 0.4 V		−3	−4.75	mA
			V_{CC} = MIN,	V_I = 0.4 V		−2.5	−3.9	
I_{CC}	Supply current	111	V_{CC} = 5 V	SN54104, SN74104		15	24	mA
				SN54105, SN74105		17	28	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

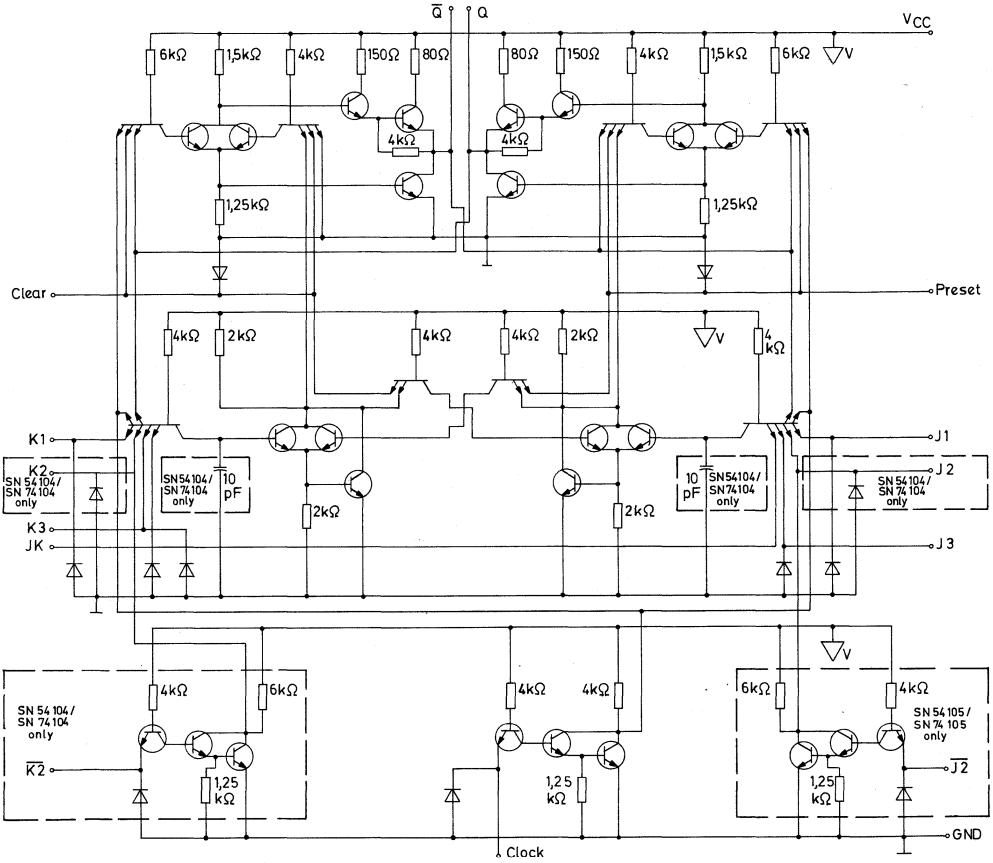
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		16	25	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



schematic



Component values shown are nominal.

▽ . . . V_{CC} bus

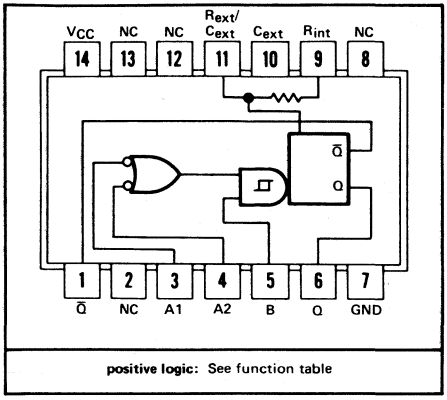
- Programmable Output Pulse Width
  With R_{int} . . . 35 ns Typ
  With R_{ext}/C_{ext} . . . 40 ns to 28 Seconds
- Internal Compensation for Virtual Temperature Independence
- Jitter-Free Operation up to 90% Duty Cycle
- Inhibit Capability

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

For explanation of function table symbols, see page 3-8.

SN54121 . . . J OR W PACKAGE
SN74121 . . . J OR N PACKAGE



positive logic: See function table

NC—No internal connection

NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}.
2. To use the internal timing resistor, connect R_{int} to V_{CC}. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

6

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

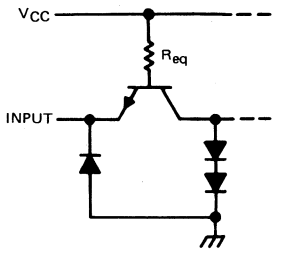
Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN 54121 and 2 kΩ to 40 kΩ for the SN74121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_{ext} R_T \ln 2 \approx 0.7\, C_{ext} R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extented if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

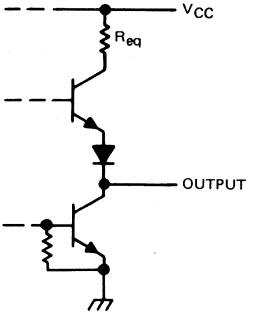
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM '121
A1	4 kΩ
A2	4 kΩ
B	2 kΩ

TYPICAL OF BOTH OUTPUTS



'121: R_{eq} = 130 Ω NOM

recommended operating conditions

		54 FAMILY / 74 FAMILY	SN54121 / SN74121 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	V
		74 Family	4.75	5	5.25	
High-level output current, I_{OH}					−400	μA
Low-level output current, I_{OL}					16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B		1			V/s
	Logic inputs, A1, A2		1			V/μs
Input pulse width, $t_{w(in)}$			50			ns
External timing resistance, R_{ext}		54 Family	1.4		30	kΩ
		74 Family	1.4		40	
External timing capacitance, C_{ext}			0		1000	μF
Duty cycle	R_T = 2 kΩ				67	%
	R_T = MAX R_{ext}				90	
Operating free-air temperature, T_A		54 Family	−55		125	°C
		74 Family	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54121 SN74121			UNIT
				MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	A1 or A2			40	μA
			B			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	A1 or A2			−1.6	mA
			B			−3.2	
I_{OS}	Short-circuit output current◆	V_{CC} = MAX	54 Family	−20		−55	mA
			74 Family	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		13	25	mA
			Triggered		23	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'121 MIN	'121 TYP	'121 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	C_L = 15 pF, R_L = 400 Ω for '121, See Note 3	C_{ext} = 80 pF, R_{int} to V_{CC}		45	70	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input				35	55	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from either A input				50	80	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from B input				40	65	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor		C_{ext} = 80 pF, R_{int} to V_{CC}	70	110	150	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		C_{ext} = 0, R_{int} to V_{CC}		30	50	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_{ext} = 100 pF, R_T = 10 kΩ	600	700	800	ns
			C_{ext} = 1 μF, R_T = 10 kΩ	6	7	8	ms

NOTE 3: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

TYPICAL CHARACTERISTICS§

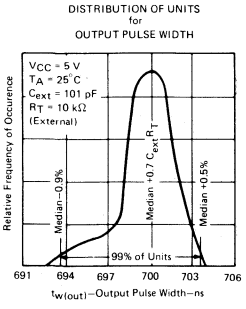


FIGURE 1

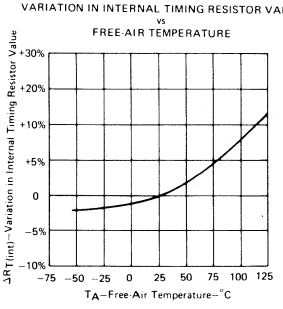


FIGURE 2

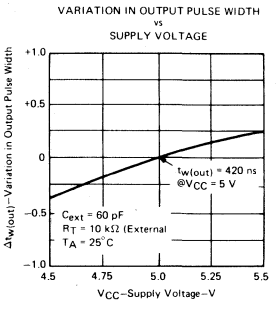


FIGURE 3

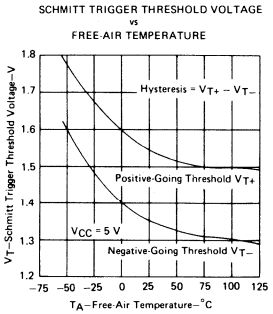


FIGURE 4

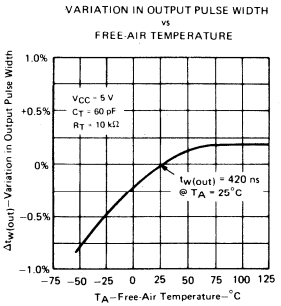


FIGURE 5

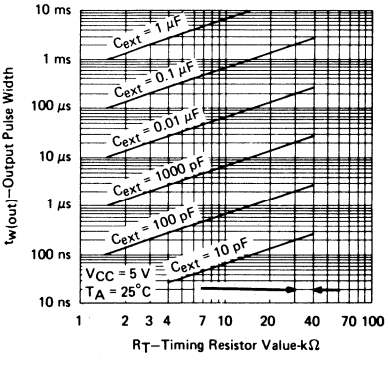


FIGURE 6

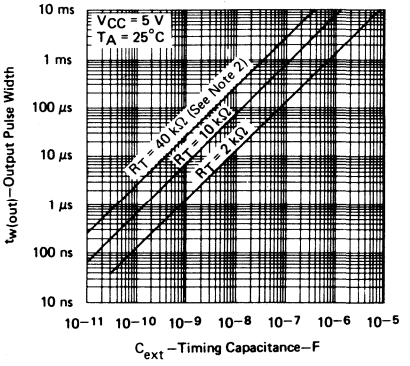


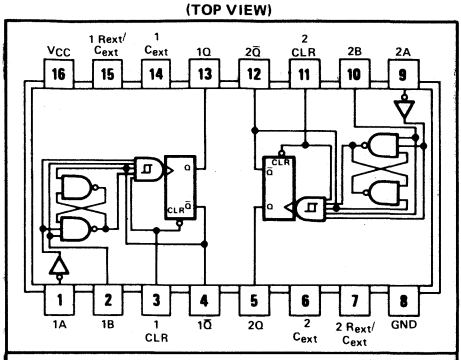
FIGURE 7

§ Data for temperatures below 0°C and above 70°C are applicable for SN54121

- SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots
- Pin-Out Is Identical to the SN54123 SN74123, SN54LS123, SN74LS123
- Overriding Clear Terminates Output Pulse

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	28 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is

FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍
Also see description and switching characteristics				

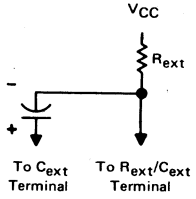
See explanation of function tables on page 3-8.

description (continued)

held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

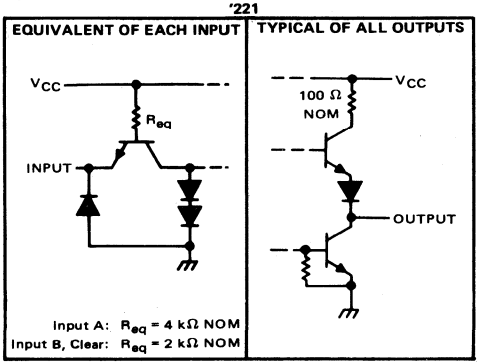
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.



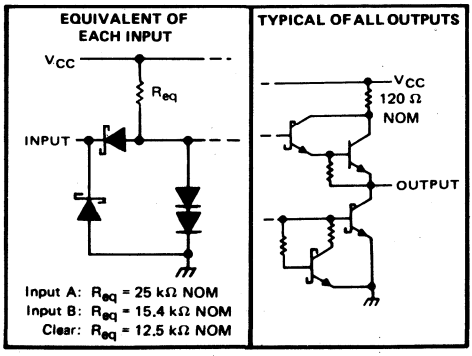
TIMING COMPONENT CONNECTIONS

schematics of inputs and outputs

'221



'LS221



recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_{ext} = 2 kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54221	−20		−55	mA
			SN74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Note 2	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	$\overline{Q}$					40	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	110	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	30	50	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	650	700	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6.5	7	7.5	ms

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width
NOTE 2: Load circuit is shown on page 3-10.

recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			50			50	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive=going threshold voltage at B input	V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, Input A	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Low-level input current, Input B					−0.8			−0.8	
	Low-level input current, Clear					−0.8			−0.8	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
			Triggered		19	27		19	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

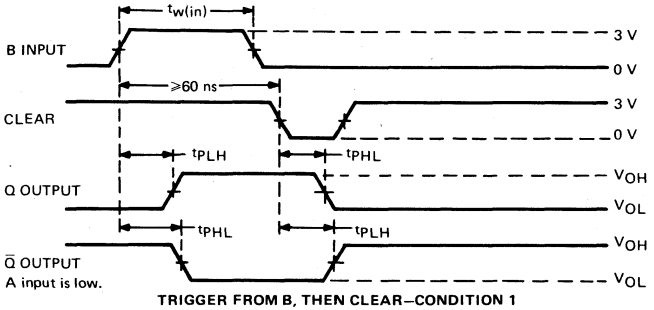
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1 and Note 3	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				35	55	ns
t_{PLH}	Clear	$\overline{Q}$				44	65	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	120	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	47	70	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	600	670	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6	6.7	7.5	ms

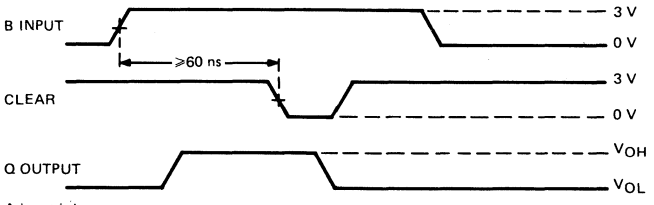
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width

NOTE 3: Load circuit is shown on page 3-11.

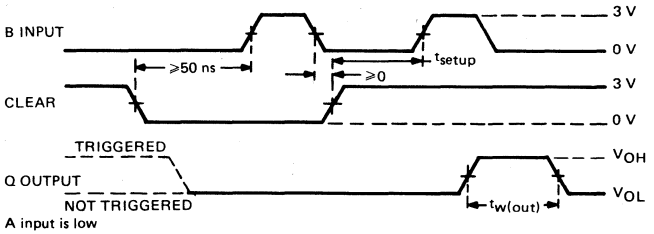
PARAMETER MEASUREMENT INFORMATION



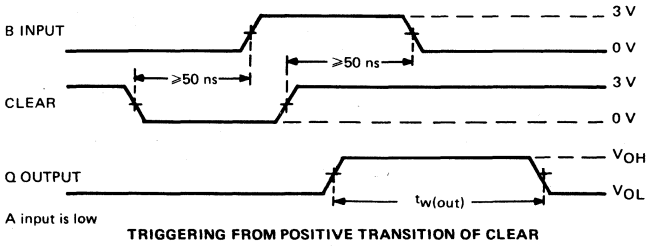
TRIGGER FROM B, THEN CLEAR–CONDITION 1



TRIGGER FROM B, THEN CLEAR–CONDITION 2



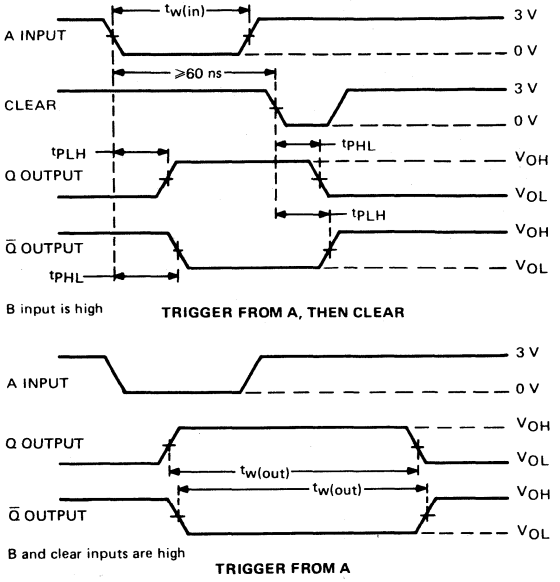
CLEAR OVERRIDING B, THEN TRIGGER FROM B



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR

FIGURE 1–SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$; for '221, $t_r \leq 7$ ns, $t_f \leq 7$ ns, for 'LS221, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

FIGURE 1–SWITCHING CHARACTERISTICS (CONTINUED)

TYPICAL CHARACTERISTICS ('221 ONLY)†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

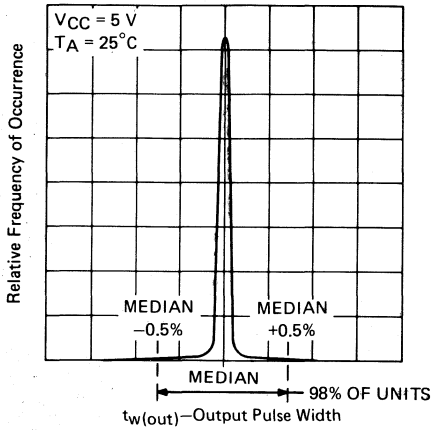


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

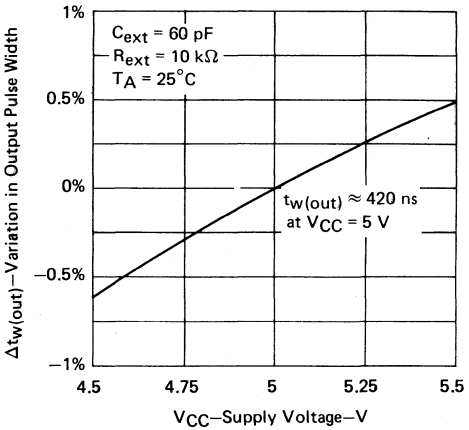


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

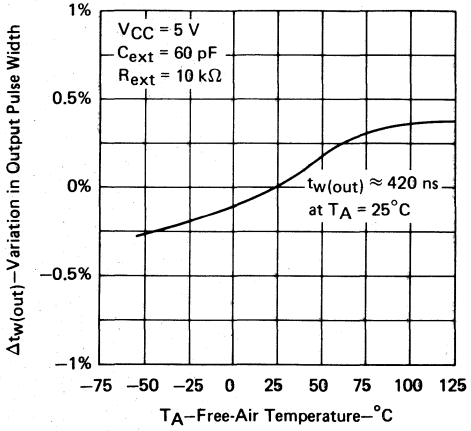


FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

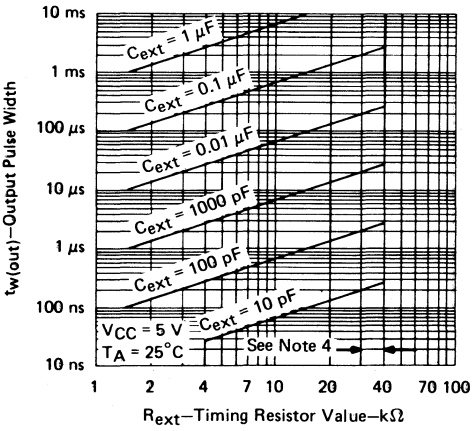


FIGURE 5

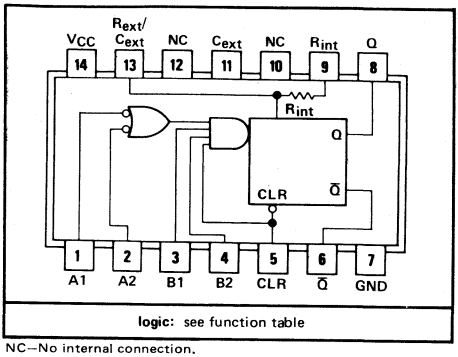
NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

†Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

REVISED OCTOBER 1983

- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Compensated for V_{CC} and Temperature Variations
- '122, 'LS122 Have Internal Timing Resistors

SN54122, SN54LS122 . . . J OR W
SN74122, SN74LS122 . . . J OR N
(TOP VIEW) (SEE NOTES 1 THRU 4)



NC—No internal connection.

'122, 'LS122
FUNCTION TABLE

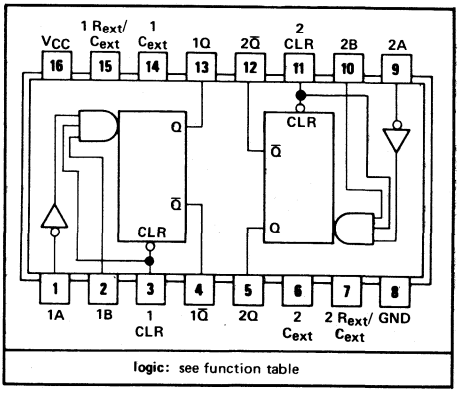
INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	Q̄
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

'123, 'LS123, '130
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See explanation of function tables on page 3-8.

SN54123, SN54LS123, SN54130 . . . J OR W
SN74123, SN74LS123, SN74130 . . . J OR N
(TOP VIEW) SEE NOTES 1 THRU 4)



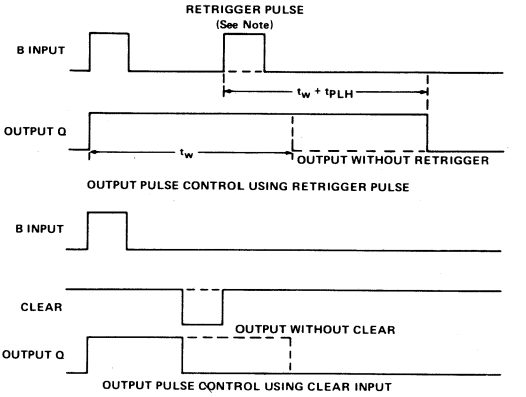
description

These d-c triggered multivibrators feature output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The '122, and 'LS122 have internal timing resistors that allow the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS122 and 'LS123 are provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of '122 or 'LS122, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open circuited.
4. To obtain variable pulse widths, connect and external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

description (continued)



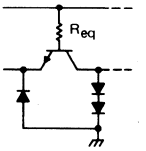
NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs

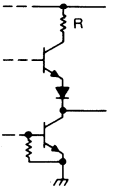
'122, '123 CIRCUITS

EQUIVALENT OF EACH INPUT



Clear inputs of '122, '123: R_{eq} = 2 kΩ NOM
Other inputs of '122, '123: R_{eq} = 4 kΩ NOM

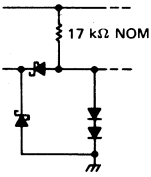
TYPICAL OF ALL OUTPUTS



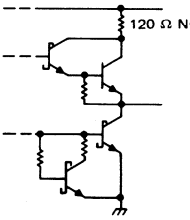
'122, '123: R = 100 Ω NOM

'LS122, 'LS123 CIRCUITS

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		25	5		50	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended free-air operating temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'122			'123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA, See Note 1		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Clear input				80			80	
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Clear input				−3.2			−3.2	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX, See Note 5	−10		−40	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7		23	36		46	66	mA

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦ Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 8

PARAMETER ¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'122			'123, '130			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF, R_{ext} = 5 kΩ, R_L = 400 Ω		22	33		22	33	ns
	B				19	28		19	28	
t_{PHL}	A	$\overline{Q}$			30	40		30	40	ns
	B				27	36		27	36	
t_{PHL}	Clear	Q			18	27		18	27	ns
t_{PLH}		$\overline{Q}$			30	40		30	40	
t_{wQ} (min)	A or B	Q			45	65		45	65	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω	3.08	3.42	3.76	2.76	3.03	3.37	μs
							3.08	3.42	3.76	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q

NOTE 8: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, $V_{IL} = V_{IL}$max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, $V_{IL} = V_{IL}$max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current◆	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 13	'LS122		6	11		6	11	mA
				'LS123		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
◆Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 12. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
13. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 14

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
NOTE 14: Load circuit and voltage waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA FOR '122, '123, '130

For pulse widths when $C_{ext} \leq 1000$ pF, See Figures 4 and 5.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

K is 0.32 for '122, 0.28 for '123,

R_T is in kΩ (internal or external timing resistance.

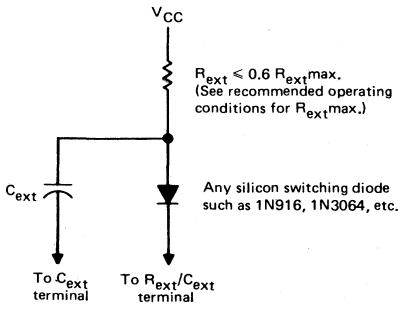
C_{ext} is in pF

t_w is in nanoseconds

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure 2 be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

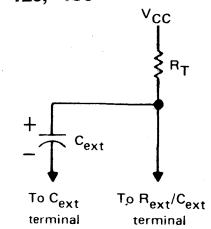
$$t_w = K_D \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

K_D is 0.28 for '122, 0.25 for '123,



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} > 1000$ pF AND CLEAR IS USED
FIGURE 2

Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with the '121.



TIMING COMPONENT CONNECTIONS
FIGURE 3

'122, '123, '130
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

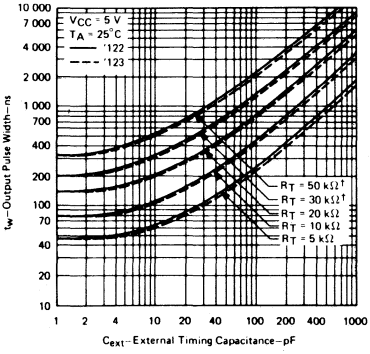


FIGURE 4

† These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' circuits.

TYPICAL APPLICATION DATA FOR 'LS122, 'LS123

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq$ 1000 pF, see Figure 8.

When $C_{ext} >$ 1000 pF, the output pulse width is defined as:

$t_W = 0.45 \cdot R_T \cdot C_{ext}$ ('LS122)
$t_W = K^* \cdot R_T \cdot C_{ext}$ ('LS123)

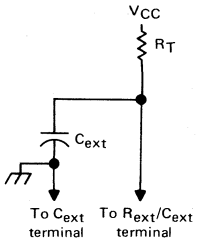
where

R_T is in kΩ (internal or external timing resistance.)

C_{ext} is in pF

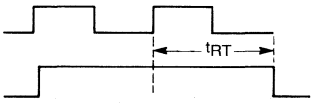
t_W is in nanoseconds

For best results, system ground should be applied to the C_{ext} terminal. The switching diode is not needed for electrolytic capacitance applications.
* See Figure 9.



TIMING COMPONENT CONNECTIONS

FIGURE 6

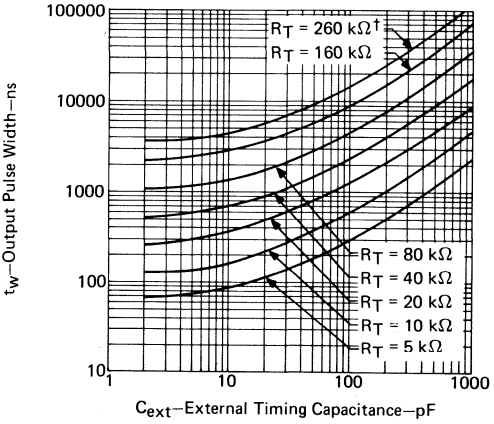


$t_{RT} = t_W + t_{PLH} = K^* \cdot R_{ext} \cdot C_{ext} + t_{PHL}$

RETRIGGER PULSE WIDTH CALCULATION

FIGURE 7

'LS122, 'LS123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 8

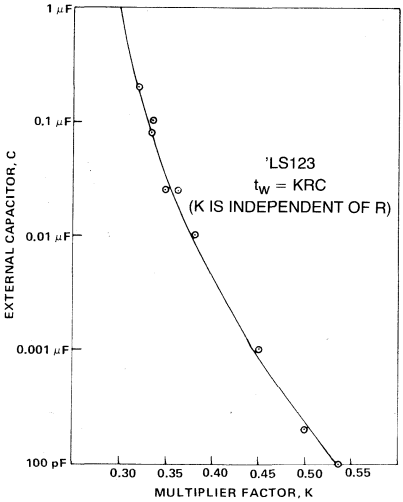


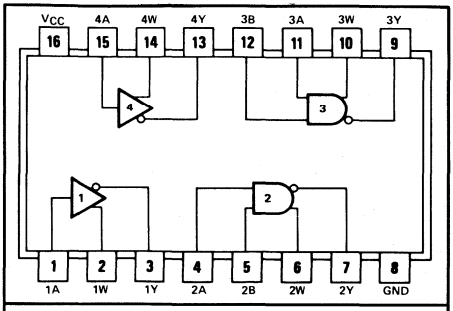
FIGURE 9

A 0.001 to 0.01 μF by-pass capacitor between V_{CC} and ground as close as possible is recommended.

FOR SYMMETRICAL GENERATION OF COMPLEMENTARY TTL SIGNALS

- **Switching Time Skew of the Complementary Outputs Is Typically 0.5 ns . . . Guaranteed to be No More than 3 ns at Rated Loading**
- **Full Fan-Out to 20 High-Level and 10 Low-Level 54/74 Loads**
- **Active Pull-Down Provides Square Transfer Characteristic**

SN54265 . . . J OR W PACKAGE
SN74265 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:

ELEMENTS 1 AND 4	ELEMENTS 2 AND 3
$Y = \overline{A}$	$Y = \overline{AB}$
$W = A$	$W = AB$

description

The SN54265 and SN74265 circuits feature complementary outputs from each logic element, which have virtually symmetrical switching time delays from the triggering input. They are designed specifically for use in applications such as:

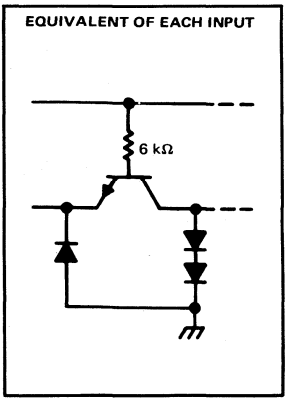
- Symmetrical clock/$\overline{\text{clock}}$ generators
- Complementary input circuit for decoders and code converters
- Switch debouncing
- Differential line driver

Examples of these four functions are illustrated in the typical application data.

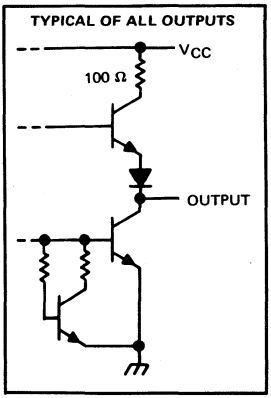
The SN54265 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74265 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN54265			SN74265			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	SN54265	−20		−57	mA
			SN74265	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		25	34	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(W)}$	A or B	W	R_L = 400 Ω, C_L = 15 pF, See Note 4		11.6	18	ns
$t_{PHL(Y)}$	(as applicable)	Y			11.3	18	
$t_{PHL(W)}$	A or B	W			9.8	18	ns
$t_{PLH(Y)}$	(as applicable)	Y			10.2	18	
$t_{PLH(W)}-t_{PHL(Y)}$	A or B	W with respect to Y			+0.3	±3	ns
$t_{PHL(W)}-t_{PLH(Y)}$	(as applicable)				−0.4	±3	

t_{PLH} ≡ Propagation delay time, low-to-high-level output.
t_{PHL} ≡ Propagation delay time, high-to-low-level output.
$t_{PXX(W)}-t_{PXX(Y)}$ ≡ Difference in indicated propagation delay times at the W and Y outputs, respectively.
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

TYPICAL CHARACTERISTICS†

PROPAGATION DELAY TIME DIFFERENCE
vs
FREE-AIR TEMPERATURE

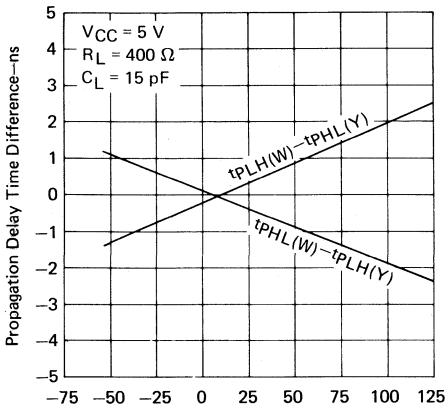


FIGURE 1

PROPAGATION DELAY TIME DIFFERENCE
vs
SUPPLY VOLTAGE

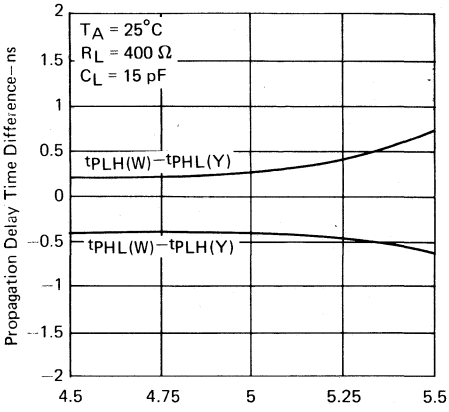


FIGURE 2

PROPAGATION DELAY TIME DIFFERENCE vs LOAD CAPACITANCE

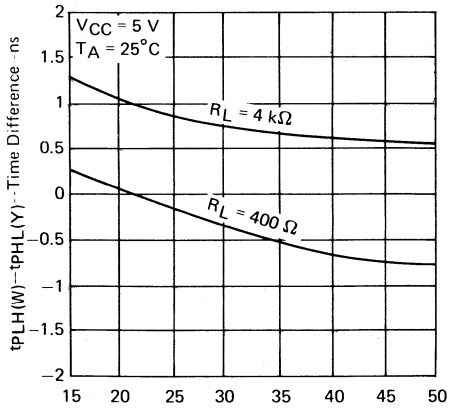


FIGURE 3

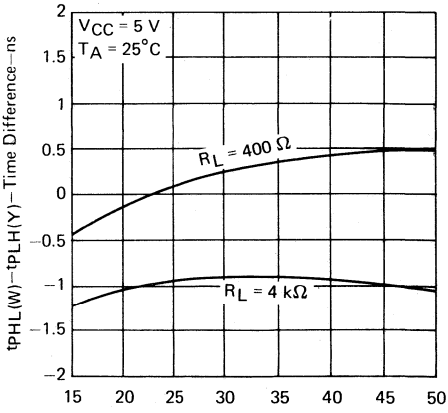


FIGURE 4

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54265 only.

TYPICAL APPLICATION DATA

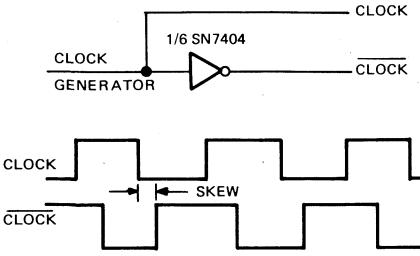


FIGURE A – TYPICAL CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

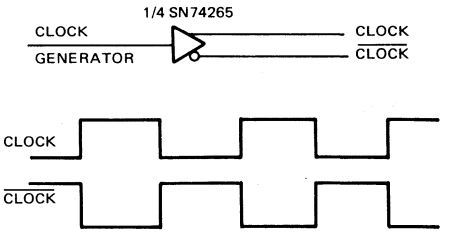


FIGURE B – SKEWLESS CLOCK/$\overline{\text{CLOCK}}$ GENERATOR CIRCUIT

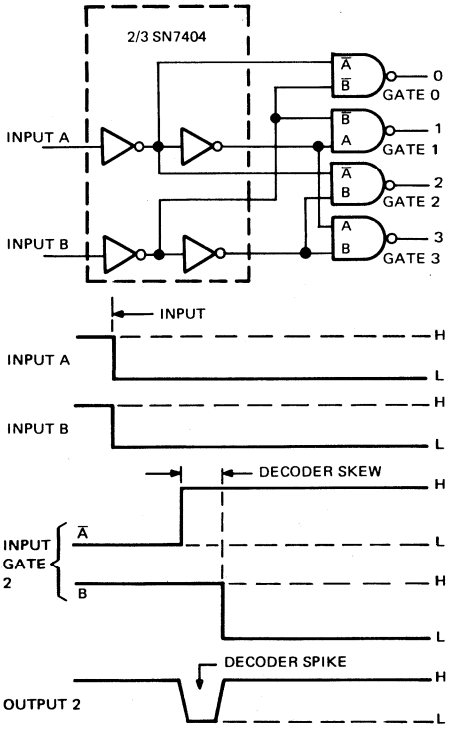


FIGURE C – TYPICAL DECODER/CODE CONVERTER

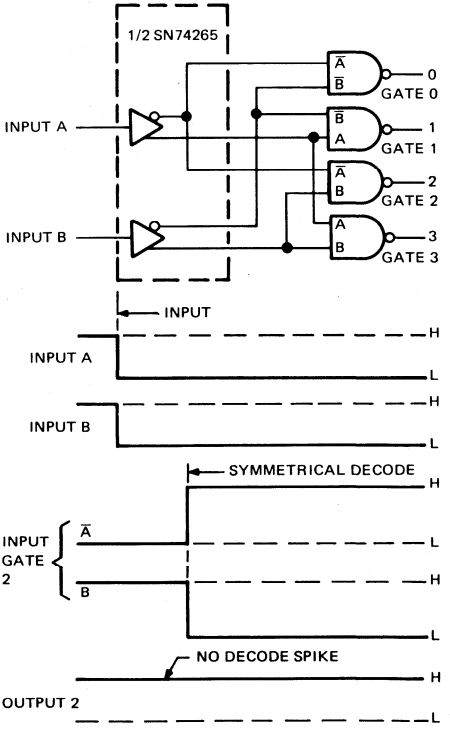


FIGURE D – SYMMETRICAL DECODER/CODE CONVERTER

TYPICAL APPLICATION DATA

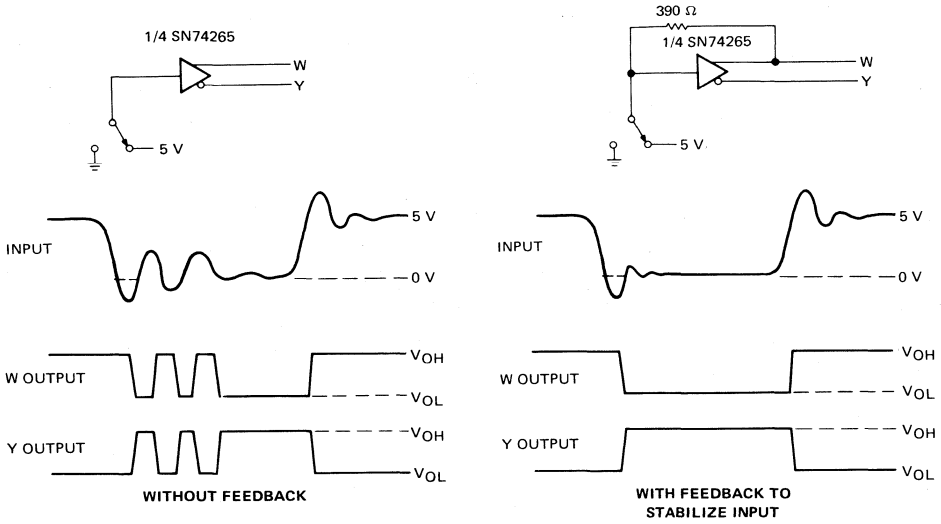
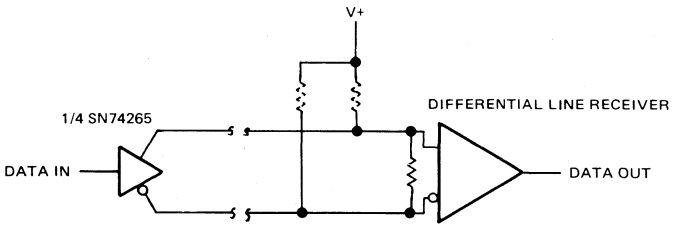


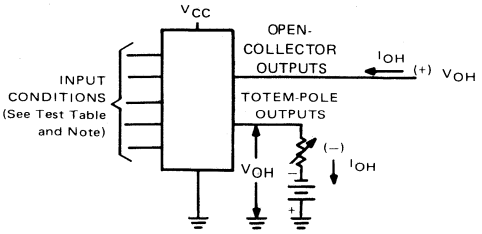
FIGURE E – SWITCH DEBOUNCER



Noise immunity typically 3 V
for either high level or low level data

FIGURE F – DIFFERENTIAL LINE DRIVER

PARAMETER MEASUREMENT INFORMATION

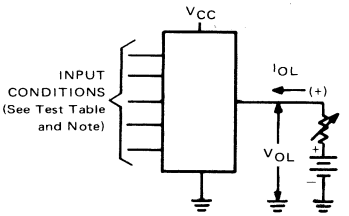


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR-INVERT	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND

FIGURE 1–V_{IH}, V_{IL}, V_{OH}, I_{OH}

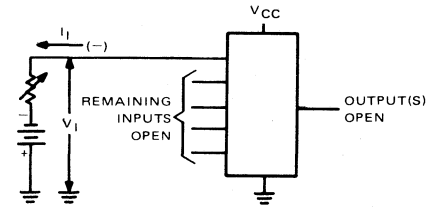


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

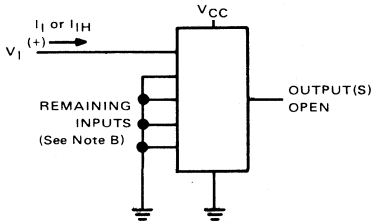
FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR-INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



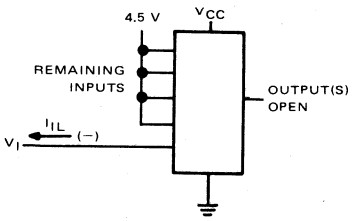
NOTE: Each input is tested separately.

FIGURE 3–V_I



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_I and grounded when testing I_{IH}.

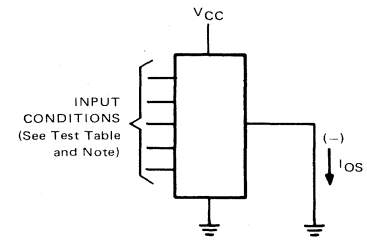
FIGURE 4–I_I, I_{IH}



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open.

FIGURE 5–I_{IL}

PARAMETER MEASUREMENT INFORMATION

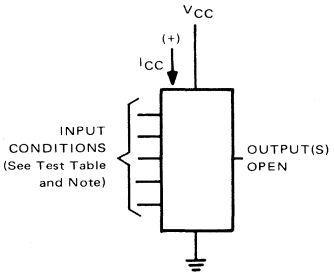


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at GND
AND-OR	All inputs at 4.5 V

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 6–I_{OS}



TEST TABLE

FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V, all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4.5 V, all others at GND	All inputs at GND

NOTE 1: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations:

$$I_{CC},\ I_{CCH},\ \text{or}\ I_{CCL}\ \text{(average per gate or flip-flop)} = \frac{\text{total } I_{CC},\ I_{CCH},\ \text{or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC}\ \text{(average per gate, 50\% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2\ \text{(number of gates in package)}}$$

NOTE 2: For certain synchronous devices where state commutation can be caused by the shorted output, an equivalent 1/2 I_{OS} test will be performed using 2.25 V and 2.125 V for the V_O condition for series 54 LS and series 74 LS respectively and halving both the min and max limits.

FIGURE 7–I_{CC}

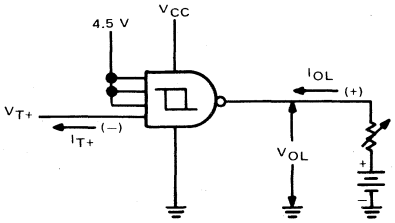


FIGURE 8–V_{T+}, I_{T+}, V_{OL} (FOR NAND SCHMITT TRIGGERS)

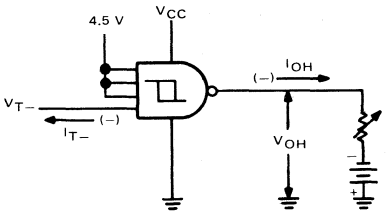
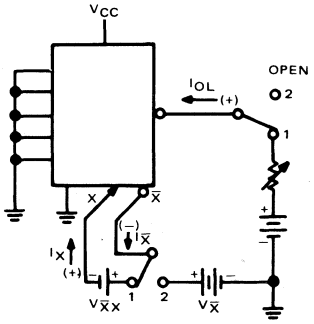


FIGURE 9–V_{T-}, I_{T-}, V_{OH} (FOR NAND SCHMITT TRIGGERS)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Switches are in position 1 for SN54'/SN74', position 2 for SN54H'/SN74H'.

B. The $I_{\overline{X}}$ limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The $V_{\overline{X}X}$ source is replaced by a resistor in parallel with a voltmeter between the X and $\overline{X}$ pins. If the measured voltage, $V_{\overline{X}X}$, is less than 0.4 V, the specified limit for $I_{\overline{X}}$ is met.

RESISTANCE VALUE TABLE

SN5423	114 Ω
SN5450, SN5453	138 Ω
SN7423	105 Ω
SN7450, SN7453	130 Ω

FIGURE 10–$I_{\overline{X}}$ (FOR EXPANDABLE GATES)

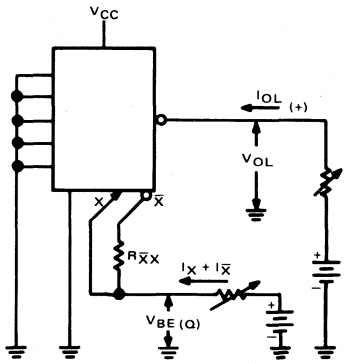


FIGURE 11–$V_{BE(Q)}$ (FOR EXPANDABLE GATES)

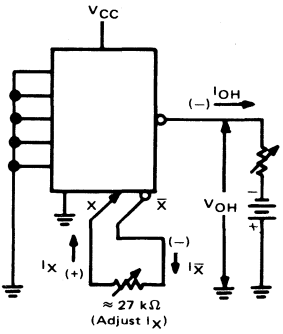


FIGURE 12–V_{OH} (FOR EXPANDABLE GATES)

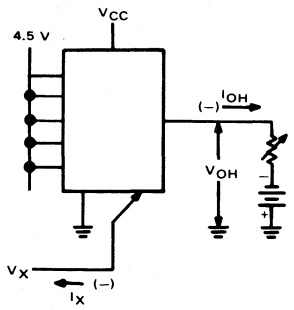


FIGURE 13–V_{OH} (FOR EXPANDABLE GATES)

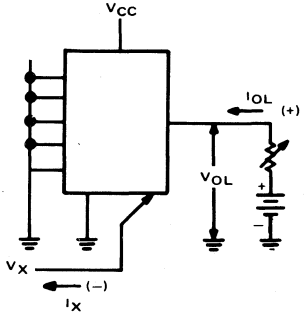


FIGURE 14–V_{OL} (FOR EXPANDABLE GATES)

PARAMETER MEASUREMENT INFORMATION

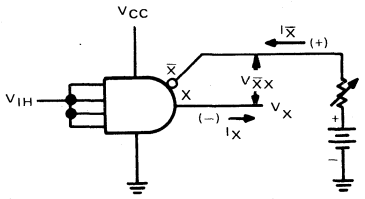


FIGURE 15—ON-STATE CHARACTERISTICS FOR EXPANDERS

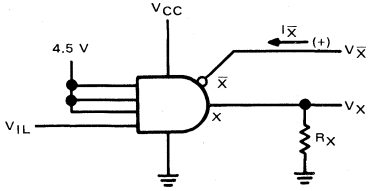


FIGURE 16—OFF-STATE CHARACTERISTICS FOR EXPANDERS

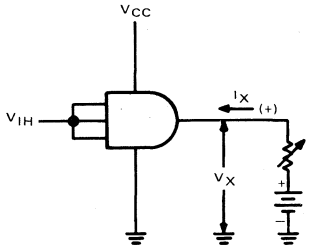


FIGURE 17—ON-STATE CHARACTERISTICS FOR EXPANDERS

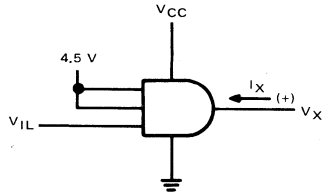
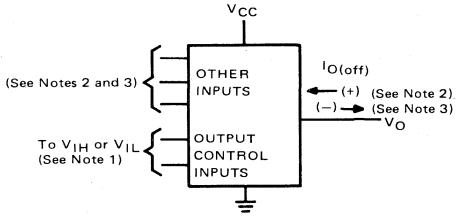


FIGURE 18—OFF-STATE CHARACTERISTICS FOR EXPANDERS



NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

FIGURE 19—$I_{O(off)}$ (THREE-STATE OUTPUTS)

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

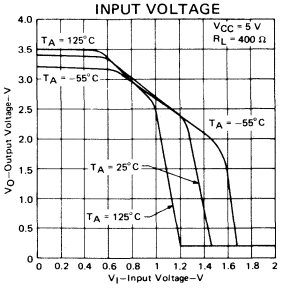


FIGURE A1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

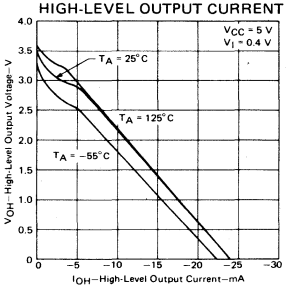


FIGURE A2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

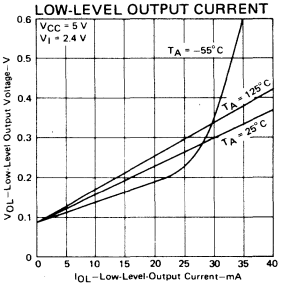


FIGURE A3

AVERAGE PROPAGATION DELAY TIME,
vs
FREE-AIR TEMPERATURE

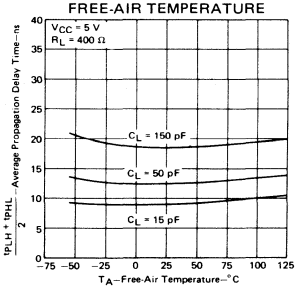


FIGURE A4

PROPAGATION DELAY TIME,
LOW-TO-HIGH LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

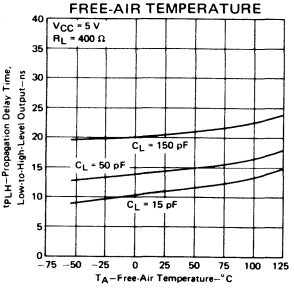


FIGURE A5

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

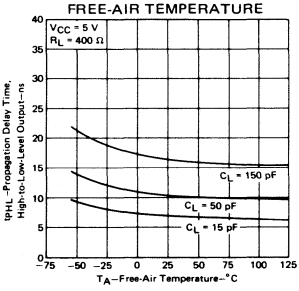


FIGURE A6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

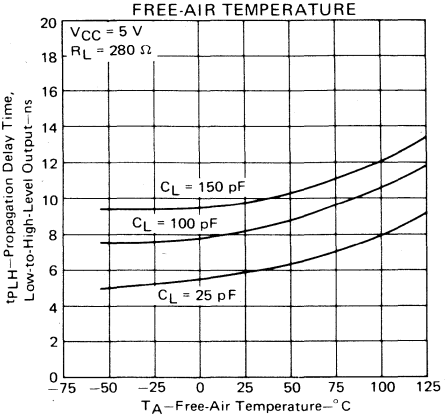


FIGURE B1

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

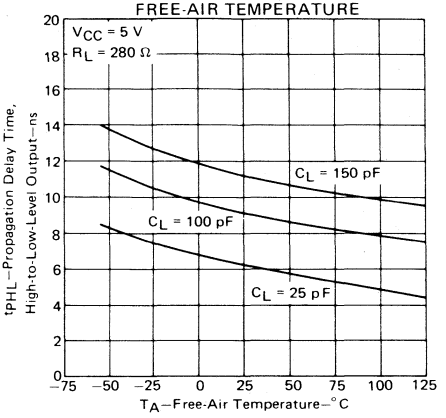


FIGURE B2

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

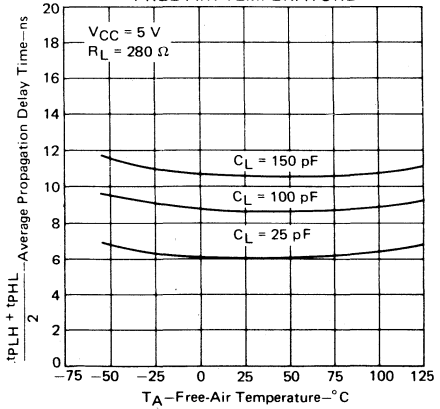


FIGURE B3

† Data for temperatures below 0°C and above 70°C are applicable for Series 54H circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

Phased out types!

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

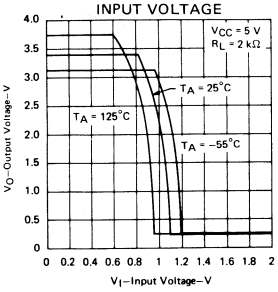


FIGURE D1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

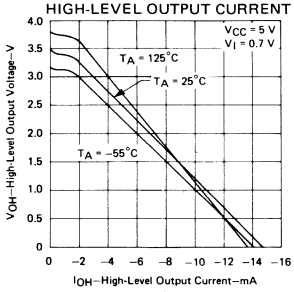


FIGURE D2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

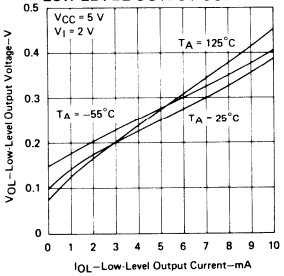


FIGURE D3

POWER DISSIPATION PER GATE
vs
FREQUENCY

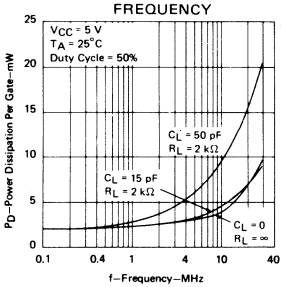


FIGURE D4

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

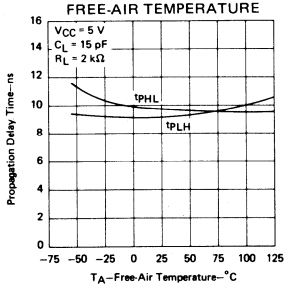


FIGURE D5

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

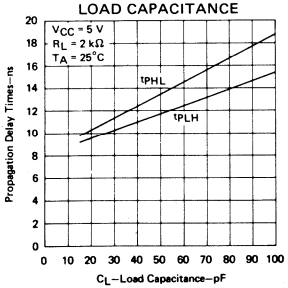


FIGURE D6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

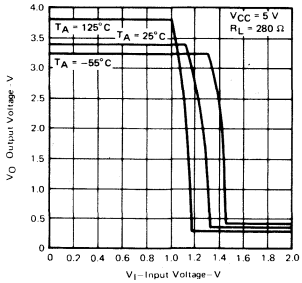


FIGURE E1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

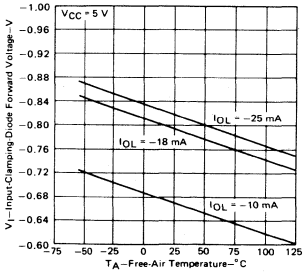


FIGURE E2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

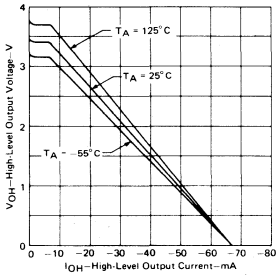


FIGURE E3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

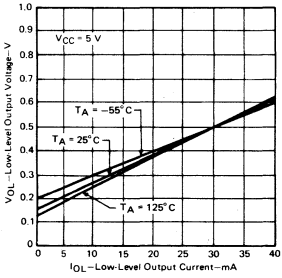


FIGURE E4

INPUT CURRENT
vs
INPUT VOLTAGE

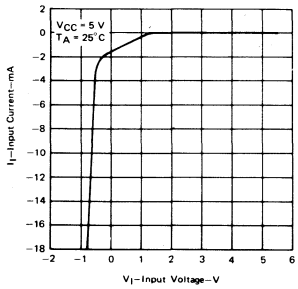


FIGURE E5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

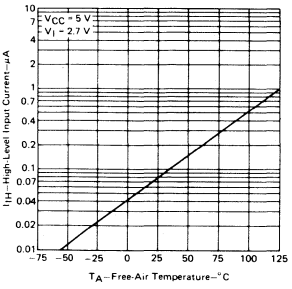


FIGURE E6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

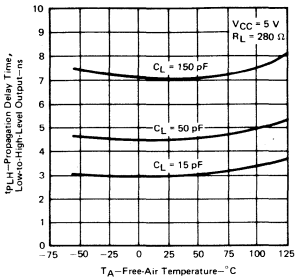


FIGURE E7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

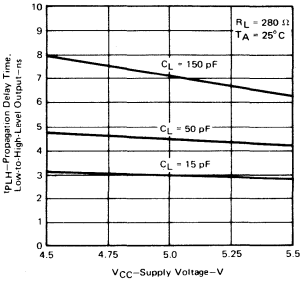


FIGURE E8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

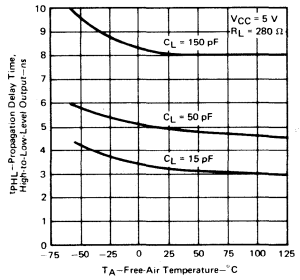


FIGURE E9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

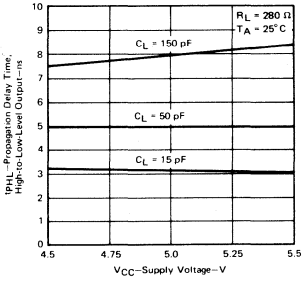


FIGURE E10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

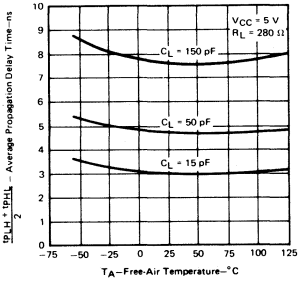


FIGURE E11

POWER DISSIPATION PER GATE
vs
FREQUENCY

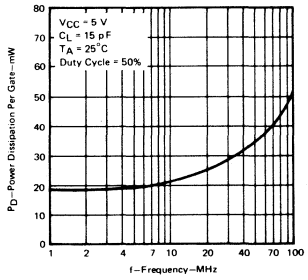


FIGURE E12

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS FOR FLIP-FLOPS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

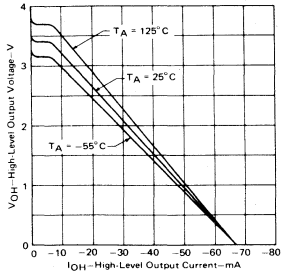


FIGURE E13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

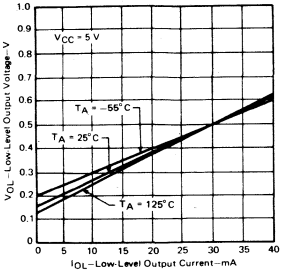


FIGURE E14

'S112, 'S113
INPUT CURRENT
vs
INPUT VOLTAGE

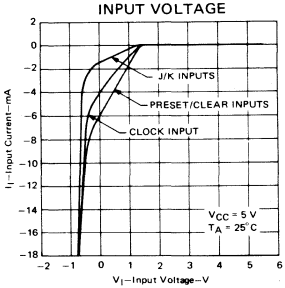


FIGURE E15

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

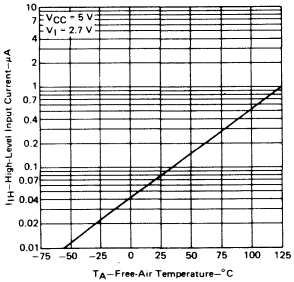


FIGURE E16

'S112, 'S113. 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

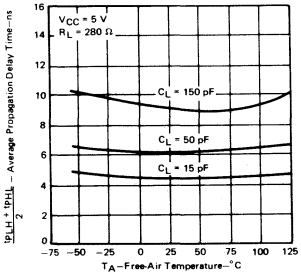


FIGURE E17

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

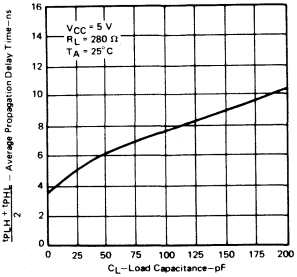


FIGURE E18

† Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.

54/74 Family
MSI/LSI Circuits

TYPES SN5442A THRU SN5444A, SN54LS42, SN7442A THRU SN7444A, SN74LS42
4-LINE-TO-10-LINE DECODERS (1-OF-10)

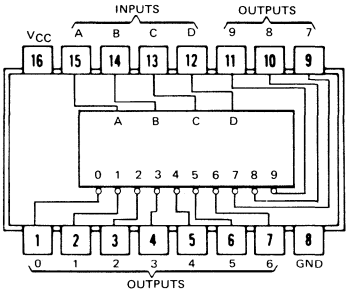
BULLETIN NO. DL-S 7611861, MARCH 1974—REVISED OCTOBER 1976

'42A, 'LS42...BCD-TO-DECIMAL
'43A...EXCESS-3-TO-DECIMAL
'44A...EXCESS-3-GRAY-TO-DECIMAL

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'LS42	35 mW	17 ns

SN5442A THRU SN5444A, SN54LS42...J OR W PACKAGE
SN7442A THRU SN7444A,
SN74LS42...J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'LS42 BCD-to-decimal decoders, the '43A excess-3-to-decimal decoders, and the '44A excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

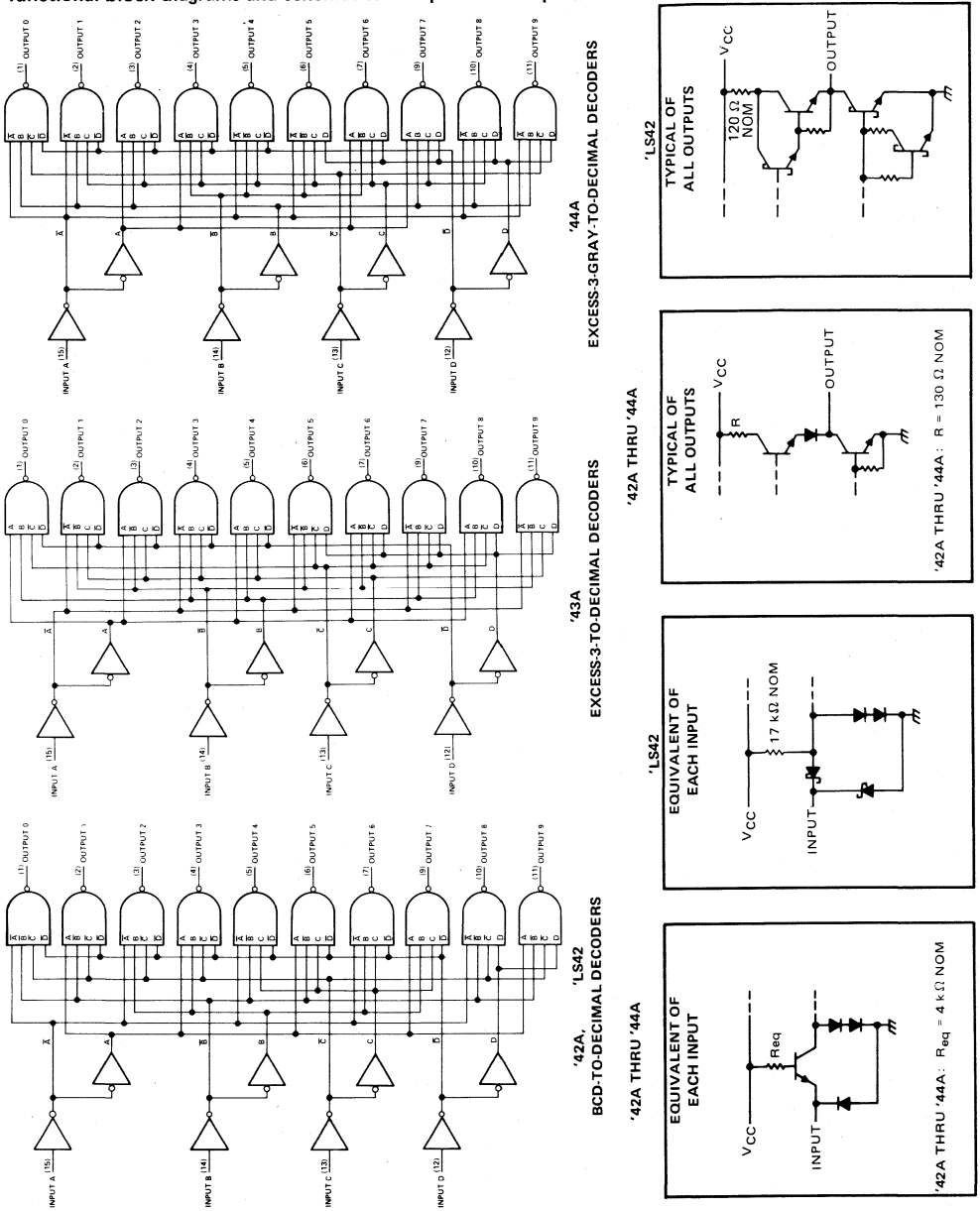
Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

NO.	'42A, 'LS42 BCD INPUT				'43A EXCESS-3 INPUT				'44A EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

functional block diagrams and schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5442A, SN5443A, SN5444A			SN7442A, SN7443A, SN7444A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5442A, SN5443A, SN5444A			SN7442A, SN7443A, SN7444A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		28	41		28	56	mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: Load circuits and waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS42 . . . . . −55°C to 125°C
SN74LS42 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS42			SN74LS42			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS42			SN74LS42			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2. I_{CC} is measured with all outputs open and inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 2 kΩ, See Note 4		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			15	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			20	30	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN5445, SN7445
BCD-TO-DECIMAL DECODERS/DRIVERS

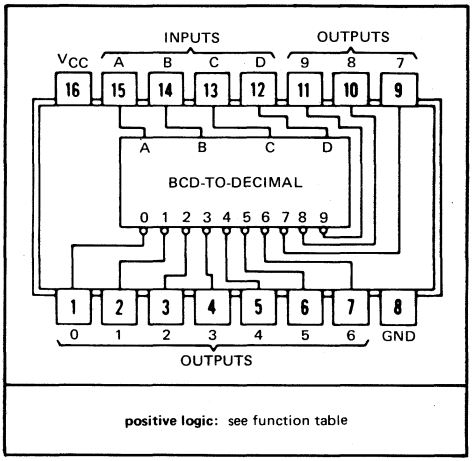
BULLETIN NO. DL-S 7211816, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

SN5445 . . . J OR W PACKAGE
SN7445 . . . J OR N PACKAGE
(TOP VIEW)



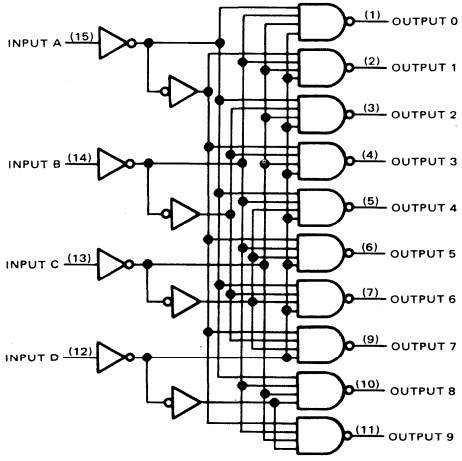
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN5445 Circuits . . . . . −55°C to 125°C
SN7445 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = 30 V				250	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN5445		43	62	mA
			SN7445		43	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

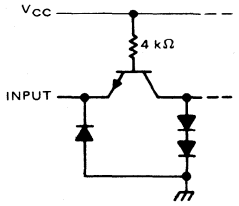
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

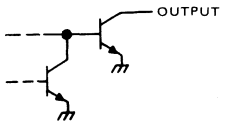
NOTE 3: Load circuit and waveforms are shown on page 3-10.

schematics of inputs and outputs

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



'46A, '47A, 'LS47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'48, 'LS48 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

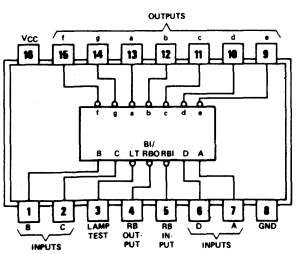
'49, 'LS49 feature

- Open-Collector Outputs
- Blanking Input

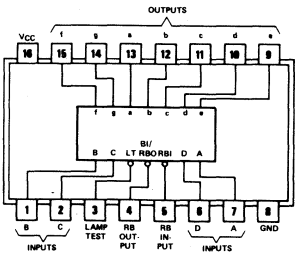
- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN5446A	low	open-collector	40 mA	30 V	320 mW	J, W
SN5447A	low	open-collector	40 mA	15 V	320 mW	J, W
SN5448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN5449	high	open-collector	10 mA	5.5 V	165 mW	W
SN54LS47	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS48	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS49	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN7446A	low	open-collector	40 mA	30 V	320 mW	J, N
SN7447A	low	open-collector	40 mA	15 V	320 mW	J, N
SN7448	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74LS47	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS48	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS49	high	open-collector	8 mA	5.5 V	40 mW	J, N

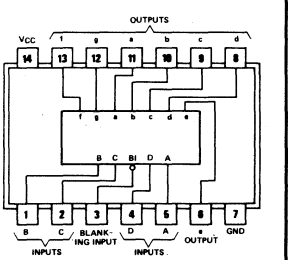
'46A, '47A, 'LS47 (TOP VIEW)



'48, 'LS48 (TOP VIEW)



'49, 'LS49 (TOP VIEW)



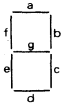
positive logic: see function tables

description

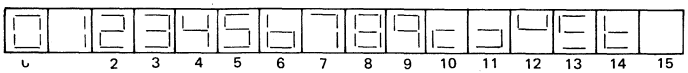
The '46A, and 'LS47 feature active-low outputs designed for driving common-anode VLEDs or incandescent indicators directly, and the '48, '49, 'LS48, 'LS49 feature active-high outputs for driving lamp buffers or common-catholde VLEDs. All of the circuits except '49 and 'LS49 have full ripple-blanking input/output controls and a lamp test input. The '49 and 'LS49 circuits incorporate a direct blanking input. Segment identification and resultant displays are schown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

The '46A, '47A, '48, 'LS47, and 'LS48 circuits incorporate automatic leading and/or trailling-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types (including the '49 and 'LS49) contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

The SN54246/SN74246 through '249 and the SN54LS247/SN74LS247 through 'LS249 compose the 6 and the 9 with tails and have been designed to offer the designer a choice between two indicator fonts. The SN54249/SN74249 and SN54LS249/SN74LS249 are 16-pin versions of the 14-pin SN5449 and 'LS49. Included in the '249 circuit and 'LS249 circuits are the full functional capability for lamp test and ripple blanking, which is not available in the '49 or 'LS49 circuit.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'LS47 FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'48, 'LS48
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'49, 'LS49
FUNCTION TABLE

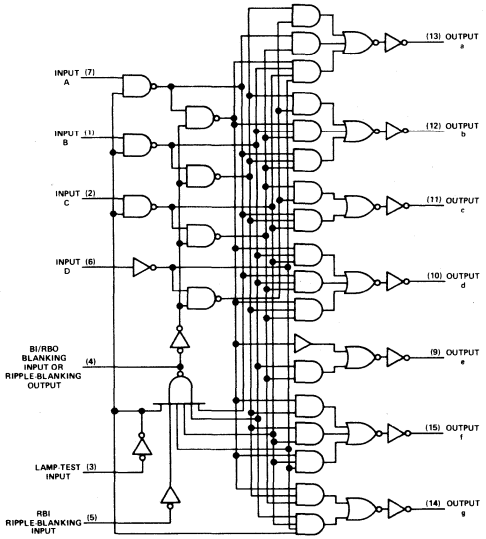
DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

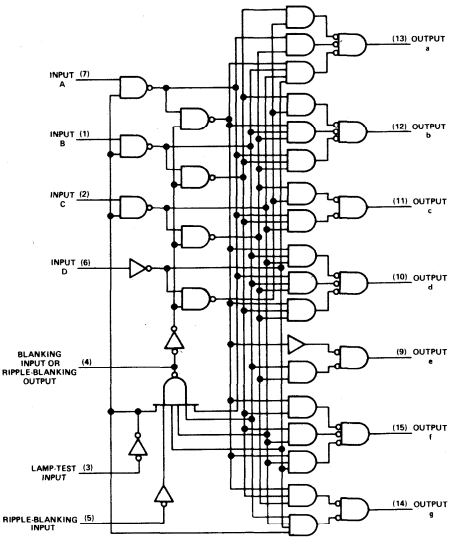
NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

functional block diagrams

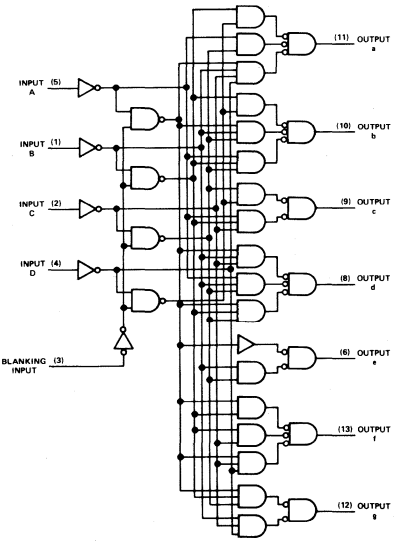
'46A, '47A, 'LS47



'48, 'LS48



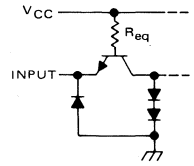
'49, 'LS49



schematics of inputs and outputs

'46A, '47A, '48, '49

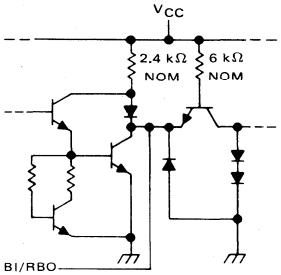
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



SN54'/SN74': R_{eq} = 6 kΩ NOM

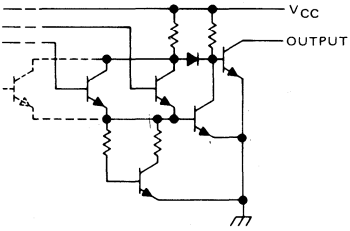
'46A, '47A, '48

EQUIVALENT OF BI/RBO



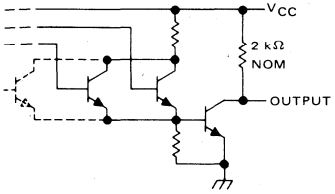
'46A, '47A

TYPICAL OF OUTPUTS a THRU g



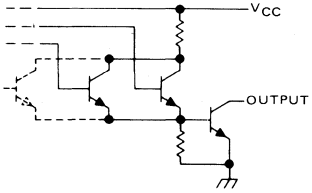
'48

TYPICAL OF OUTPUTS a THRU g



'49

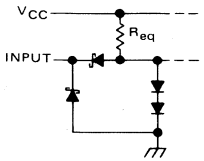
TYPICAL OF ALL OUTPUTS



schematics of inputs and outputs

'LS47, 'LS48, 'LS49

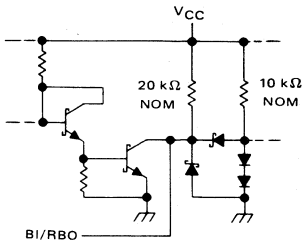
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



LT and RBI ('LS47, 'LS48): R_{eq} = 20 kΩ NOM
BI ('LS49): R_{eq} = 20 kΩ NOM
A, B, C, and D: R_{eq} = 25 kΩ NOM

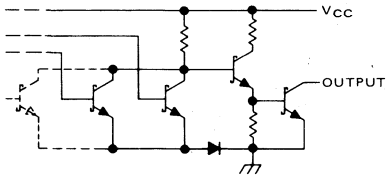
'LS47, 'LS48, 'LS49

EQUIVALENT OF BI/RBO



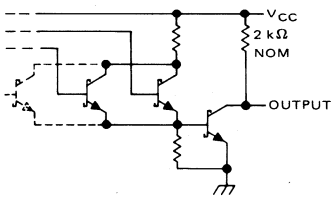
'LS47

TYPICAL OF OUTPUTS a THRU g



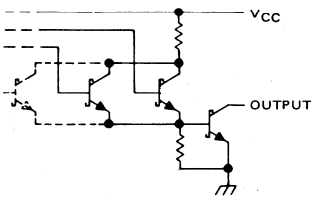
'LS48

TYPICAL OF OUTPUTS a THRU g



'LS49

TYPICAL OF OUTPUTS a THRU g



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN5446A, SN5447A . . . . . −55°C to 125°C
SN7446A, SN7447A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	BI/RBO			−200			−200			−200			−200	μA
Low-level output current, I_{OL}	BI/RBO			8			8			8			8	mA
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA		2.4	3.7		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.27	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 40 mA			0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		BI/RBO					−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN54′		64	85	mA
				SN74′		64	103	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 120 Ω, See Note 3			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS47 . . . . . −55°C to 125°C
SN74LS47 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS47			SN74LS47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			15			15	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS47			SN74LS47			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 15 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5448 . . . . . −55°C to 125°C
SN7448 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5448			SN7448			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			−400			−400	μA
	BI/RBO			−200			−200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V,		2.4	4.2		V
		BI/RBO	V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.7		
I_O	Output current	a thru g	V_{CC} = MIN, V_O = 0.85 V, Input conditions as for V_{OH}		−1.3	−2		mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		BI/RBO					−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−4	mA
I_{CC}	Supply current		V_{CC} = MIN, See Note 2	SN5448		53	76	mA
				SN7448		53	90	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 1 kΩ, See Note 5			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS48 . . . . . −55°C to 125°C
SN74LS48 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS48			SN74LS48			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			−100			−100	μA
	BI/RBO			−50			−50	
Low-level output current, I_{OL}	a thru g			2			6	mA
	BI/RBO			1.6			3.2	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS48			SN74LS48			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	a thru g and BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	2.4	4.2		2.4	4.2		V
I_O	Output current	a thru g	V_{CC} = MIN, Input conditions as for V_{OH}	V_O = 0.85 V,	−1.3	−2		−1.3	−2		mA
V_{OL}	Low-level output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 2 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 6 mA					0.35	0.5	
		BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any input except BI/BRO	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		25	38		25	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 4 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	C_L = 15 pF, R_L = 6 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 6: Load circuit and voltage waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5449			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			10	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5449			UNIT
			MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.6	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −10 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 10 mA		0.27	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		33	47	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 667 Ω, See Note 5			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS49 . . . . . −55°C to 125°C
SN74LS49 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS49			SN74LS49			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS49			SN74LS49			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		8	15		8	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

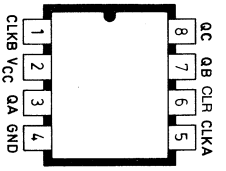
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 2 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	C_L = 15 pF, R_L = 6 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 6: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS56, SN54LS57, SN74LS56, SN74LS57
FREQUENCY DIVIDERS

- **'LS56 Performs 50 to 1 Frequency Division (5 to 1, 5 to 1, and 10 to 1)**
- **'LS57 Performs 60 to 1 Frequency Division (6 to 1, 5 to 1, and 10 to 1)**
- **Available in P or JG Package (Two P or JG Packages fit in a Single 16-pin Socket)**
- **Maximum Clock Frequency 25 MHz Typical**

SN54LS56, SN54LS57 . . . JG PACKAGE
SN74LS56, SN74LS57 . . . JG OR P PACKAGE
(TOP VIEW)



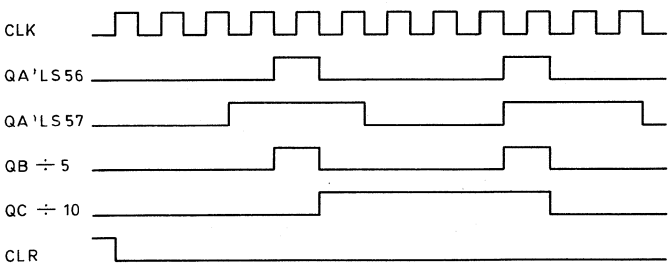
description

These frequency dividers are particularly useful in generating one second or one hour timing pulses from 50 Hz (European standard frequency) or 60 Hz (United States standard frequency). 50 to 1 frequency division is accomplished in the 'LS56 by tying output QA to input CLKB. 60 to 1 frequency division in the 'LS57 is accomplished in the same way. More universal capabilities are evidenced by the 25 MHZ typical f max and the almost limitless frequency division possibilities when used in cascade. Two 'LS56 packages may be interconnected to give frequency division of 2500 to 1, 625 to 1, 100 to 1. Two 'LS57 packages can be connected to generate frequency divisions of 3600 to 1, 1800 to 1, 900 to 1.

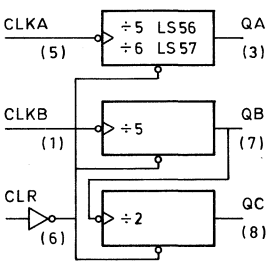
The 'LS56 and 'LS57 frequency dividers consist of three separate counters, A, B, and C, on a single monolithic substrate. The A counter divides by 5 to 1 in the 'LS56 and by 6 to 1 in the 'LS57. The B counter divides by 5 to 1 in both devices and is internally tied to the C counter which divides by 2 to 1. The resulting C counter output is 10 to 1. Both the 'LS56 and 'LS57 feature a clear pin which is common to all three counters, A, B, and C. When the clear pin is low, the counters are anabled. When the clear is high, the counters are disabled and their outputs are set to a low level.

All three counters, A, B, and C trigger on the high-to-low transition of the clock input. All output waveforms are symmetrical except for the 5 to 1 outputs (A and B of the 'LS57). (See the output waveform dravings below.)

input and output waveforms



functional block diagram



switching characteristics, V_{CC} = 5V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS56			'LS57			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f max	CLKA	QA	RL = 1 kΩ, CL = 30 pF	15	25		15	25		MHz
f max	CLKB	QB, QC		15	25		15	25		MHz
TPLH	CLKB	QB			8	15		8	15	ns
TPHL	CLKB	QB			14	25		14	25	ns
TPLH*	CLKB	QC			18	30		18	30	ns
TPHL*	CLKB	QC			24	35		24	35	ns
TPLH	CLKA	QA			12	20		14	25	ns
TPHL	CLKA	QA			14	25		18	30	ns
TPHL	CLR	QA			17	30		17	30	ns
TPHL	CLR	QB			17	30		17	30	ns
TPHL	CLR	QC			17	30		17	30	ns

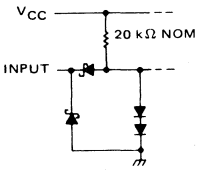
* Times measured from CLKB to output QC are taken with output QB unloaded.

recommended operating conditions

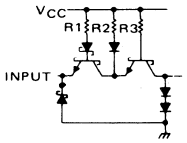
	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1.0			−1.0	mA
Low-level output current, I_{OL}			8			16	mA
Rise and fall time of clock, t_r, t_f			50			50	ns
Pulse width of clock or clear, tw	33			33			ns
Clear inactive state setup time, tsu	25			25			ns
Clock frequency, f_{clock}	0		15	0		15	MHz
Operating free air temperature, T_A	−55		125	0		70	C

schematics of inputs and outputs

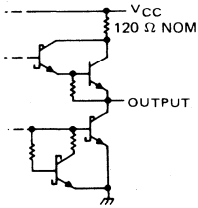
EQUIVALENT OF EACH RESET INPUT



EQUIVALENT OF A AND B INPUTS



TYPICAL OF ALL OUTPUTS



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL}max	I_{OL} = 16 mA					0.35	0.5	V
I_I	Input current at maximum input voltage	CLKA, CLKB	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
		CLR		V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	CLKA, CLKB	V_{CC} = MAX,	V_I = 2.7 V			80			80	μA
		CLR					20			20	μA
I_{IL}	Low-level input current	CLKA, CLKB	V_{CC} = MAX, C_{LR} = 0 V	V_I = 0.4 V			−3.2			−3.2	mA
		CLR					−0.2			−0.2	mA
I_{OS}	Short-circuit output current*		V_{CC} = MAX, C_{LR} = 0 V,	V_O = 0 V	−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 1			17	30		17	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, TA = 25°C.
* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 1: I_{CC} is measured by applying 4.5 V to the C_{LR} pin with all other inputs grounded and the outputs open.

7

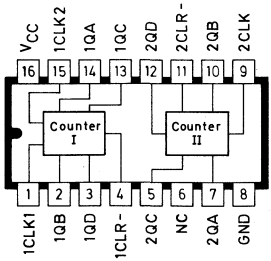
TYPE SN74LS68
DUAL 40 MHZ DECADE COUNTER

Description:

The SN74LS68 is a dual 40 MHz asynchronous decade counter. during the count operation transfer of information to the outputs occurs on the negativegoing edge of the clock pulse.

These counters feature a direct clear which, when taken low, sets all out-puts low regardless of the states of the clocks. Both clear inputs and all outputs are buffered.

The SN74LS68 may be used as a frequency divider 100:1 in either symmetrical mode for frequencies up to 40 MHz (figure 1) or asymmetrical mode for frequencies up to 40 MHz (figure 2).



Truth tables

Decade (see note A)
Counter I or II

COUNT CLOCK 1	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

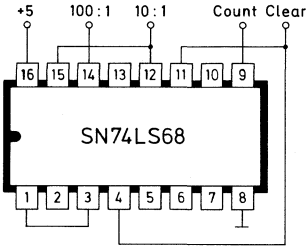
Bi-Quinary (see note B)
Counter I only

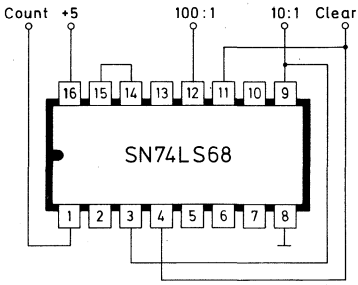
COUNT CLOCK 2	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

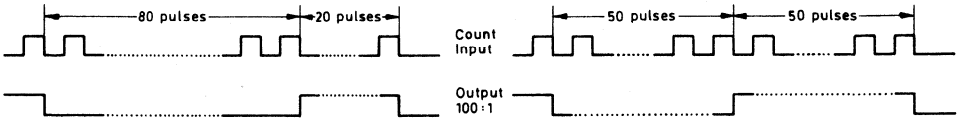
Notes:

A Output Q_A externally connected to clock 2 input for counter I. For counter II this connection has been made internally.

B Output Q_D externally connected to clock 1 input for counter I.







Symmetrical frequency division 100:1

FIGURE 1

Asymmetrical frequency division 100:1

FIGURE 2

Absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . clear inputs 7 V
clock inputs 5.5 V
Operating free-air temperature range SN74LS68 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP*	MAX	UNIT
V_{IH} High input voltage	V_{CC} = 4.75 V		2			V
V_{IL} Low level input voltage	V_{CC} = 4.75 V				0.8	V
V_{IK} Input clamp voltage	V_{CC} = 4.75 V; I_I = −18 mA				−1.5	V
V_{OH} High level output voltage V_{IL} = V_{IL} (MAX)	V_{CC} = 4.75 V; I_{OH} = −1 mA; V_{IH} = 2 V		2.7			V
V_{OL} Low level output voltage V_{IL} = V_{IL} (MAX)	V_{CC} = 4.75 V; I_{OL} = 16 mA; V_{IH} = 2 V			0.35	0.5	V
V_{OL} Low level output voltage V_{IL} = V_{IL} (MAX)	V_{CC} = 4.75 V; I_{OL} = 8 mA; V_{IH} = 2 V			0.25	0.4	V
I_I Input current at max. input voltage	V_{CC} = 5.25 V; V_I = 5.5 V;	CLK			100	µA
	V_I = 7 V	$\overline{CLR}$			100	
I_{IH} High level input current	V_{CC} = 5.25 V	clear			20	µA
	V_{IH} = 2.7 V	clock			40	µA
I_{IL} Low level input current	V_{CC} = 5.25 V	clear			−200	µA
	V_{IL} = 0.4 V	1 clock 1, 2 clock			−2	mA
		1 clock 2			−1.2	mA
I_{OS} Short circuit output current	V_{CC} = 5.25 V, see note 1		−20		−100	mA
I_{CC} Supply current (outputs open)	V_{CC} = 5.25 V, all inputs grounded			36	54	mA

* All typical valuese are at V_{CC} = 5.0 V and T_A = 25°C.

Note 1: Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

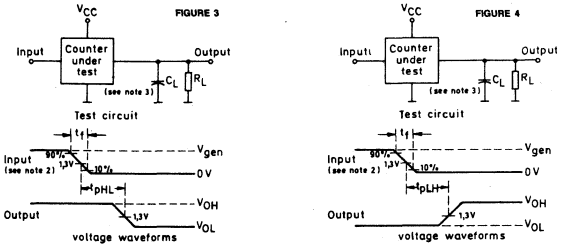
switching characteristics, V_{CC} = 5 V, T_A = 30 pF, R_L = 1 kΩ

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
f_{MAX}	1CLK1	1QA	50	70		MHz
f_{MAX}	1CLK2	1QB, 1QC, 1QD	20	30		MHz
f_{MAX}	2CLK	1QB, 2QB, 2QC, 2QD	40	60		MHz
t_{PLH}	1CLK1	1QA		7	11	ns
t_{PHL}	1CLK1	1QA		14	21	ns
t_{PLH}	1CLK2	1QB		8	12	ns
t_{PHL}	1CLK2	1QB		12	18	ns
t_{PLH}	1CLK2	1QC		15	23	ns
t_{PHL}	1CLK2	1QC		21	32	ns
t_{PLH}	1CLK2	1QD		8	12	ns
t_{PHL}	1CLK2	1QD		13	20	ns
t_{PLH}	2CLK	2QA		7	11	ns
t_{PHL}	2CLK	2QA		14	21	ns
t_{PLH}	2CLK	2QB		16	24	ns
t_{PHL}	2CLK	2QB		19	29	ns
t_{PLH}	2CLK	2QC		23	35	ns
t_{PHL}	2CLK	2QC		27	40	ns
t_{PLH}	2CLK	2QD		16	24	ns
t_{PHL}	2CLK	2QD		19	29	ns
t_{PHL}	any $\overline{CLR}$	any Q		20	30	ns

recommended operating conditions

PARAMETER (T_A = 70 deg C)		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				– 1	mA
Low-level output current, I_{OL}				16	mA
Clear inactive-state setup time		25			ns
Clock frequency, f_{MAX}	1CLK1	0		50	MHz
	1CLK2	0		20	MHz
	2CLK	0		40	MHz
Pulse width, t_w	1CLK1	10			ns
	1CLK2	25			ns
	2CLK	13			ns
	clear inputs	15			ns

PARAMETER MEASUREMENT INFORMATION



Notes: 2. Input pulse has the following characteristics: V_{gen} = 3.0 V, PRR = 10 MHz, t_f < 10 ns.
3. C_L includes probe and jig capacitance.

Description:

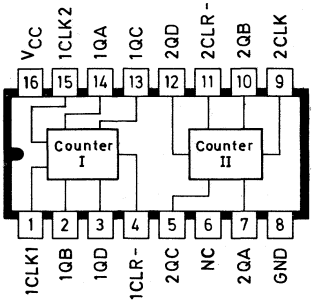
The SN74LS69 is a dual 40 MHz asynchronous 4 Bit Binary Counter. During the count operation transfer of information to the outputs occurs on the negative-going edge of the clock pulse.

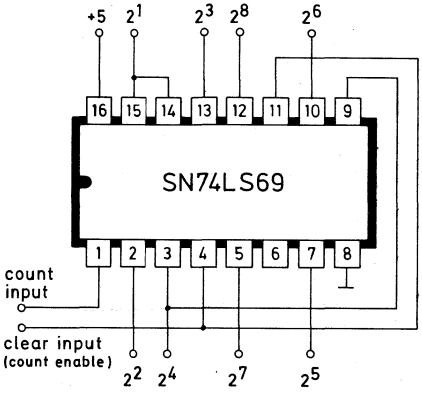
These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks. Both clear inputs and all outputs are buffered. The SN74LS69 may be used as a frequency divider 256:1 by externally connecting pin 15 to pin 16 and pin 3 to pin 9 as shown in figure 1.

Truth table (see note A)

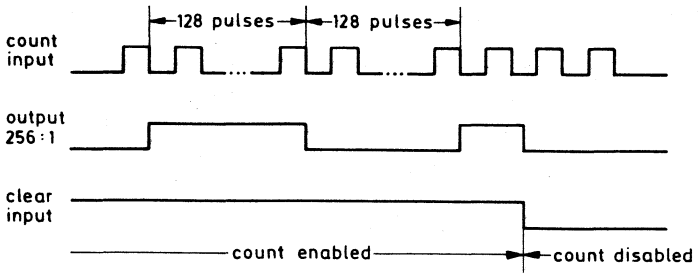
COUNT	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Note A:
Output Q_A externally connected to clock 2 input for counter I. For counter II this connection has been made internally.





Interconnections for frequency division 256 : 1



Input-output waveforms for division 256 : 1 and count inhibit.

FIGURE 1

Absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . clear inputs 7 V
clock inputs 5.5 V
Operating free-air temperature range SN74LS69 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

Electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP*	MAX	UNIT
V_{IH} High level input voltage	V_{CC} = 4.75 V		2			V
V_{IL} Low level input voltage	V_{CC} 4.75 V				0.8	V
V_{IK} Input clamp voltage	V_{CC} 4.75; I_I = −18 mA				−1.5	V
V_{OH} High level output voltage, V_{IL} = VIL MAX	V_{CC} = 4.75 V; I_{OH} = −1 mA; V_{IH} = 2 V		2.7	3.4		V
V_{OL} Low level output voltage, V_{IL} = VIL MAX	V_{CC} = 4.75 V; I = 16 mA; V_{IH} = 2 V			0.35	0.5	V
V_{OL} Low level output voltage, V_{IL} = VIL MAX	V_{CC} = 4.75 V; IOL = 8 mA; V_{IH} = 2 V			0.25	0.4	V
I_I Input current at max. input voltage	V_{CC} = 5.25 V;	OL V_I = 5.5 V; clock			100	μA
		V_I = 7 V; $\overline{\text{clear}}$			100	μA
I_{IH} High level input current	V_{CC} = 5.25 V;	$\overline{\text{clear}}$			20	μA
	V_{IH} = 2.7 V;	clock			40	μA
I_{IL} Low level input current	V_{CC} = 5.25 V;	$\overline{\text{clear}}$			−200	μA
	V_{IL} = 0.4 V;	1 clock 1, 2 clock			−2	mA
		1 clock 2			−1.2	mA
I_{OS} Short circuit output current	V_{CC} = 5.25 V, see note 1		−20		−100	mA
I_{CC} Supply current (outputs open)	V_{CC} = 5.25 V, all inputs grounded			36	54	mA

* All typical values are at V_{CC} = 5.0 V and T_A = 25°C.

Note 1: Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 30 pF, R_L = 1 kΩ

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COND.	MIN	TYP	MAX	UNIT
f_{MAX}	1CLK1	1QA	R_L = 1 K OHM	50	70		MHz
f_{MAX}	1CLK2	1QB, 1QC, 1QD	C_L = 30 pF	25	35		MHz
f_{MAX}	2CLK	1QB, 2QB, 2QC, 2QD		50	70		MHz
t_{PLH}	1CLK1	1QA			7	11	ns
t_{PHL}	1CLK1	1QA			14	21	ns
t_{PLH}	1CLK2	1QB			7	11	ns
t_{PHL}	1CLK2	1QB			14	21	ns
t_{PLH}	1CLK2	1QC			16	24	ns
t_{PHL}	1CLK2	1QC			21	32	ns
t_{PLH}	1CLK2	1QD			25	38	ns
t_{PHL}	1CLK2	1QD			30	45	ns
t_{PLH}	2CLK	2QA			7	11	ns
t_{PHL}	2CLK	2QA			14	21	ns
t_{PLH}	2CLK	2QB			14	21	ns
t_{PHL}	2CLK	2QB			19	29	ns
t_{PLH}	2CLK	2QC			23	35	ns
t_{PHL}	2CLK	2QC			27	40	ns
t_{PLH}	2CLK	2QD	R_L = 1 K OHM		32	48	ns
t_{PHL}	2CLK	2QD	C_L = 30 pF		36	54	ns
t_{PHL}	any $\overline{CLR}$	any Q			20	30	ns

recommended operating conditions

PARAMETER T_A = 0 to 70 °C		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				−1	mA
Low-level output current, I_{OL}				16	mA
Clear inactive-state setup time		25			ns
Clock frequency, f_{MAX}	1CLK1	0		50	MHz
	1CLK2	0		25	MHz
	2CLK	0		50	MHz
Pulse width, t_w	1CLK1	10			ns
	1CLK2	25			ns
	2CLK	13			ns
	clear inputs	15			ns

PARAMETER MEASUREMENT INFORMATION

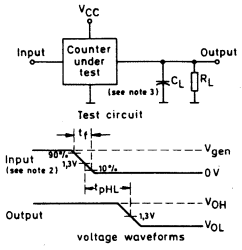


FIGURE 3

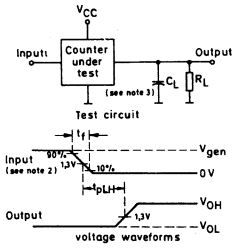


FIGURE 4

Notes: 2. Input pulse has the following characteristics: V_{gen} = 3.0 V, PRR = 10 MHz, t_f < 10 ns.
3. C_L includes probe and jig capacitance.

TYPES SN5475, SN5477, SN54LS75, SN54LS77, SN7475, SN74LS75 4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7611851, MARCH 1974—REVISED OCTOBER 1976

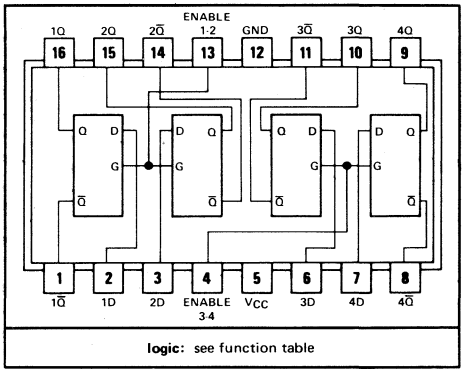
logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

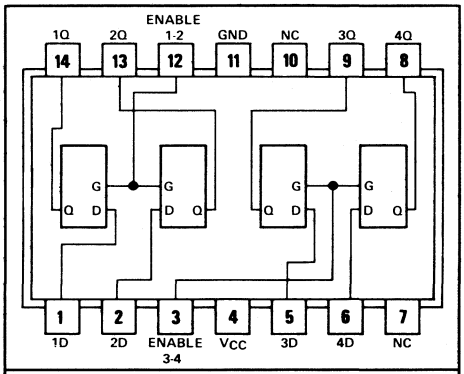
H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

SN5475, SN54LS75 . . . J OR W PACKAGE
SN7475, SN74LS75 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN5477, SN54LS77 . . . W PACKAGE



logic: see function table

NC—No internal connection

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75 and 'LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'LS77 4-bit latches are available in 14-pin flat packages.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS devices are characterized for operation from 0°C to 70°C.

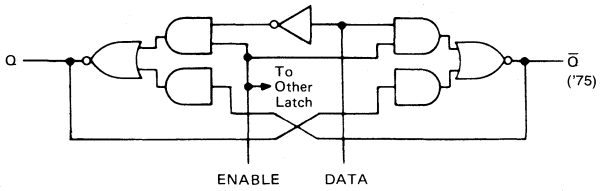
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '75, '77 . . . . . 5.5 V
'LS75, 'LS77 . . . . . 7 V
Intermitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN 74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

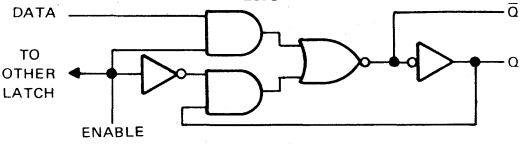
NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

functional block diagrams (each latch)

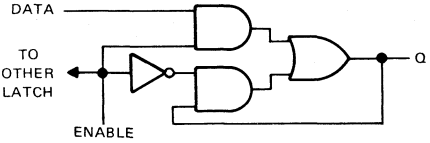
'75, '77



'LS75



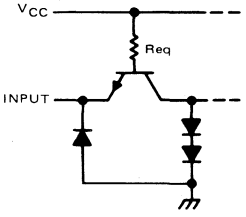
'LS77



schematics of inputs and outputs

'75, '77

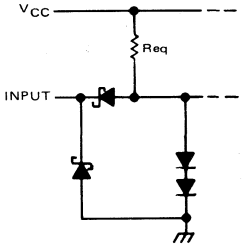
EQUIVALENT OF EACH INPUT



Data: Req = 2 kΩ NOM
Enable: Req = 1 kΩ NOM

'LS75, 'LS77

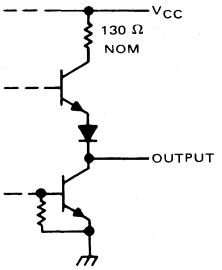
EQUIVALENT OF EACH INPUT



Data: Req = 17 kΩ
Enable: Req = 4.2 kΩ

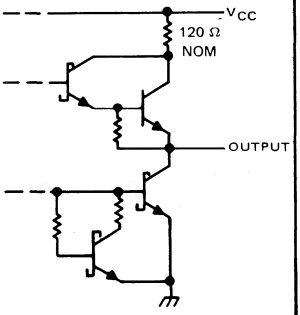
'75, '77

TYPICAL OF ALL OUTPUTS



'LS75, 'LS77

TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		G input					160	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		G input					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54′	−20		−57	mA
				SN74′	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54′		32	46	mA
				SN74′		32	53	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		16	30	ns
t_{PHL}					14	25	
t_{PLH}¶	D	$\overline{Q}$			24	40	ns
t_{PHL}¶					7	15	
t_{PLH}	G	Q			16	30	ns
t_{PHL}					7	15	
t_{PLH}¶	G	$\overline{Q}$			16	30	ns
t_{PHL}¶					7	15	

◇t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
¶These parameters are not applicable for the SN5477.

recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS75 SN54LS77			SN74LS75			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	D input			0.1			0.1	mA
				G input			0.4			0.4	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	D input			20			20	μA
				G input			80			80	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	D input			−0.4			−0.4	mA
				G input			−1.6			−1.6	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	'LS75		6.3	12		6.3	12	mA
				'LS77		6.9	13				

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

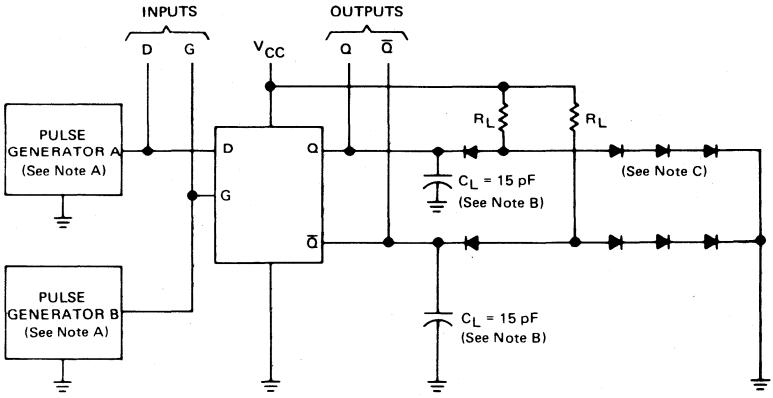
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75			'LS77			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1		15	27		11	19	ns
t_{PHL}					9	17		9	17	
t_{PLH}	D	$\overline{Q}$			12	20				ns
t_{PHL}					7	15				
t_{PLH}	G	Q			15	27		10	18	ns
t_{PHL}					14	25		10	18	
t_{PLH}	G	$\overline{Q}$			16	30				ns
t_{PHL}					7	15				

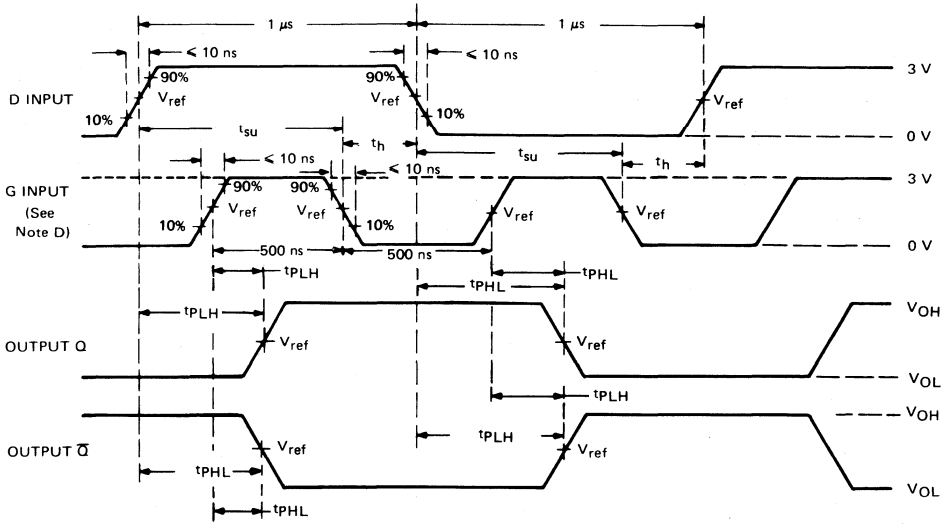
◇t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics Z_{out} = 50 Ω, for pulse generator A, PRR ≤ 500 kHz: for pulse generator B, PPR ≤ 1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. When measuring propagation delay times from the D input, the corresponding G input must be held high.
E. For '75, '77, V_{ref} = 1.5 V; for 'LS75 and 'LS77, V_{ref} = 1.3 V.

† Complementary $\overline{Q}$ outputs are on the '75 and 'LS75 only.

FIGURE 1

TYPES SN5480, SN7480
GATED FULL ADDERS

BULLETIN NO. DL-S 7211809, DECEMBER 1972

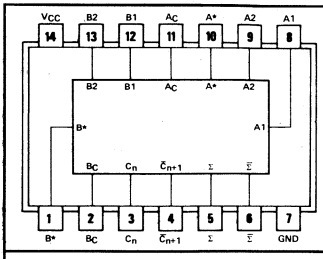
logic

FUNCTION TABLE
(See Notes 1, 2, and 3)

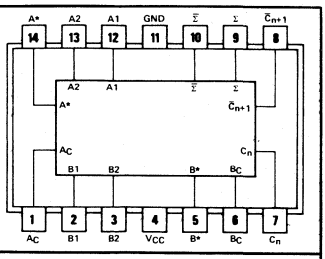
INPUTS			OUTPUTS		
C_n	B	A	$\overline{C}_{n+1}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = high level, L = low level

SN5480 . . . J PACKAGE
SN7480 . . . J OR N PACKAGE
(TOP VIEW)



SN5480 . . . W PACKAGE
(TOP VIEW)



positive logic: see function table

NOTES: 1. $A = \overline{A}_C + \overline{A}* + A1 \cdot A2$, $B = \overline{B}_C + \overline{B}* + B1 \cdot B2$.
2. When A* is used as an input, A1 or A2 must be low. When B* is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A* or B*, respectively, must be open or used to perform dot-AND logic.

description

These single-bit, high-speed, binary full adders with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output are designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. These circuits (see schematic) utilize diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs and are entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN5480 Circuits . . . . . −55°C to 125°C
SN7480 Circuits . . . . . 0° to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 4. Voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN5480			SN7480			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Σ or $\overline{\Sigma}$			−400			−400	µA
	$\overline{C}_{n+1}$			−200			−200	
	A* or B*			−120			−120	
Low-level output current, I_{OL}	Σ or $\overline{\Sigma}$			16			16	mA
	$\overline{C}_{n+1}$			8			8	
	A* or B*			4.8			4.8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5480			SN7480			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{OH}	High-level output voltage	Σ or $\overline{\Sigma}$	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
		$\overline{C}_{n+1}$		I_{OH} = −200 μA							
		A* or B*		I_{OH} = −120 μA							
V_{OL}	Low-level output voltage	Σ or $\overline{\Sigma}$	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 16 mA		0.22	0.4		0.22	0.4	V
		$\overline{C}_{n+1}$		I_{OL} = 8 mA							
		A* or B*		I_{OL} = 4.8 mA							
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	A_1, A_2, B_1, B_2, A_C, or B_C	V_{CC} = MAX, V_I = 2.4 V				15			15	μA
		A* or B*				−1.1			−1.1		
		C_n					200			200	
I_{IL}	Low-level input current	A1, A2, B1, B2, A_C, or B_C	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		A* or B*					−2.6			−2.6	
		C_n					−8			−8	
I_{OS}	Short-circuit output-current§	Σ or $\overline{\Sigma}$	V_{CC} = MAX		−20		−57	−18		−57	mA
		$\overline{C}_{n+1}$			−20		−70	−18		−70	
		A* or B*			−0.9		−2.9	−0.9		−2.9	
I_{CC}	Supply current		V_{CC} = MAX, See Note 6			21	31		21	35	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 6: I_{CC} is measured with all inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

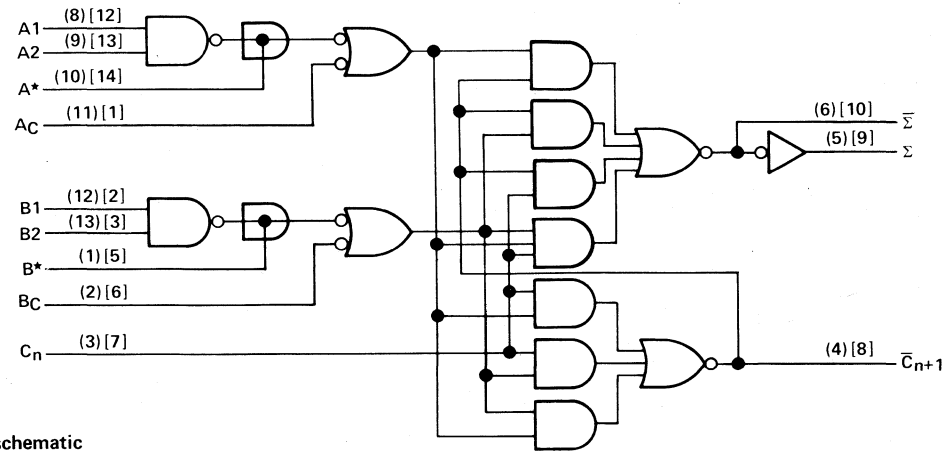
PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	$\overline{C}_{n+1}$	C_L = 15 pF, R_L = 780 Ω, See Note 7		13	17	ns
t_{PHL}					8	12	
t_{PLH}	B_C	$\overline{C}_{n+1}$			18	25	
t_{PHL}					38	55	
t_{PLH}	A_C	Σ	C_L = 15 pF, R_L = 400 Ω, See Note 7		52	70	ns
t_{PHL}					62	80	
t_{PLH}	B_C	$\overline{\Sigma}$			38	55	
t_{PHL}					56	75	
t_{PLH}	A1	A*	C_L = 15 pF, See Note 7		48	65	ns
t_{PHL}					17	25	
t_{PLH}	B1	B*			48	65	
t_{PHL}					17	25	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

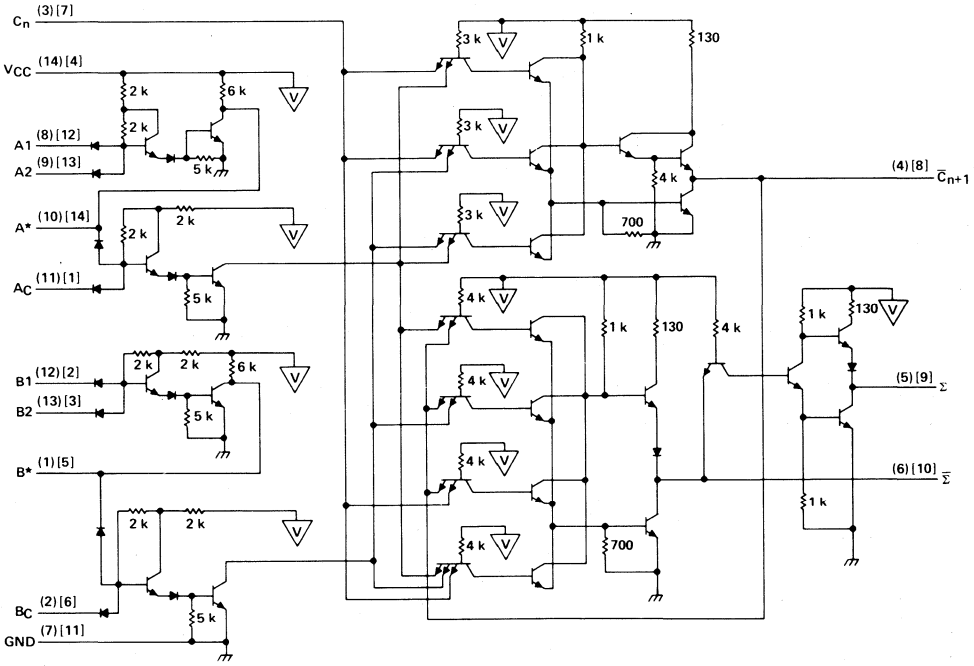
NOTE 7: The load for testing outputs A* and B* consists only of capacitance C_L to ground. The load circuit for the other outputs and voltage waveforms are shown on page 3-10.

functional block diagram

(DUAL-IN-LINE) [FLAT PACKAGE]



schematic



V ... V_{CC} bus

Resistor values shown are nominal and in ohms.

TYPES SN5481A, SN5484A, SN7481A, SN7484A
16-BIT RANDOM-ACCESS MEMORIES

BULLETIN NO. DL-S 7211581, DECEMBER 1972

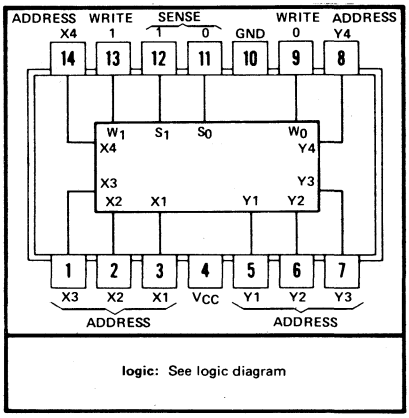
description

Each of these 16-bit active-element memories is a high-speed, monolithic, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to form a scratch-pad memory with direct-address and nondestructive read-out. These devices are interchangeable with and replace SN5481, SN7481, SN5484, and SN7484, but feature diode-clamped inputs, improved switching speeds, and lower supply current requirements.

The flip-flops are arranged in a four-by-four matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled three-emitter transistors, is used to store one bit. To determine if a logic 1 or logic 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logic 1 sensing outputs are connected to the sense 1 (S_1) amplifier input and all 16 of the logic 0 sensing outputs are connected to the sense 0 (S_0) amplifier input. The two remaining emitters of each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low and currents from all conducting flip-flop transistors flow out of these address lines.

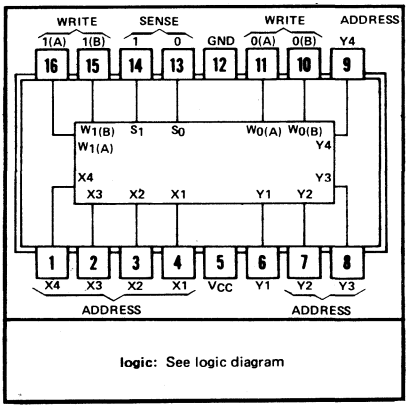
To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a high level. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a low level and no change will occur in those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense 1 amplifier or the sense 0 amplifier is activated. When this occurs, the output of the activated sense amplifier drops from a high logic level to a low logic level. The memory is nondestructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

SN5481A . . . J OR W PACKAGE
SN7481A . . . J OR N PACKAGE
(TOP VIEW)



logic: See logic diagram

SN5484A . . . J OR W PACKAGE
SN7484A . . . J OR N PACKAGE
(TOP VIEW)



logic: See logic diagram

To store new information in a flip-flop, it is necessary to address it and apply a high-level voltage to the appropriate write amplifier. (The SN5484A and SN7484A have gated write-amplifier inputs). The output of the write amplifier responds by dropping to a low logic level. Since all Sense 0 lines are connected to the output of the write 0 amplifier and all sense 1 lines are connected to the output of the write 1 amplifier, a low level at the output of a write amplifier

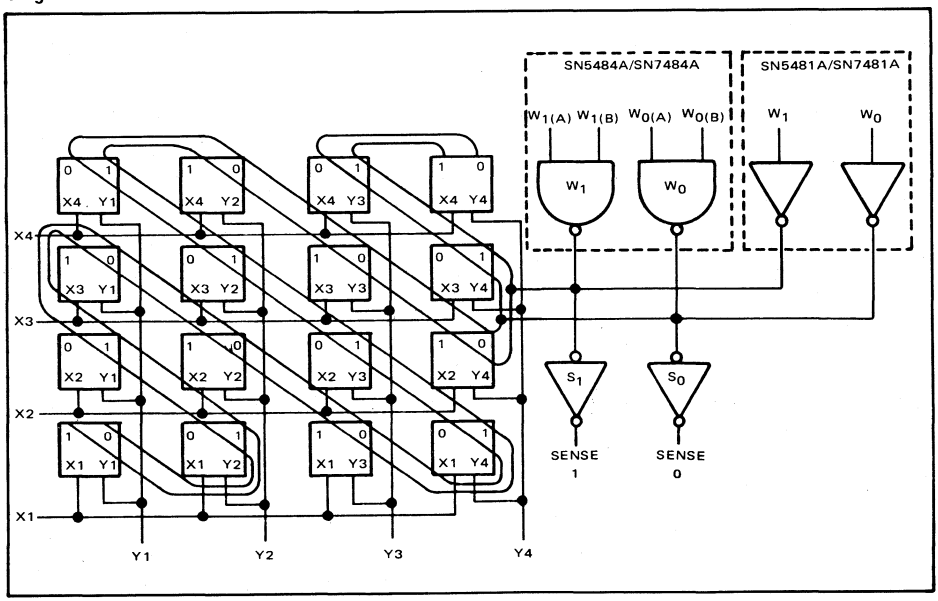
description (continued)

will cause the emitters of all flip-flop transistors connected to that amplifier to go low. In all the flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. Two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. If the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

A number of active-element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). All inputs and outputs are compatible with most DTL and TTL circuits. Average power dissipation is typically 225 milliwatts, and the open-collector outputs may be wire-AND connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 12 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance. The SN5481A and SN5484A circuits are designed for operation over the full military temperature range of −55°C to 125°C; the SN7481A circuits are designed for operation from 0°C to 70°C.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
High-level output voltage . . . . . 5.5 V
Operating free-air temperature range: SN5481A, SN5484A Circuits . . . . . −55°C to 125°C
SN7481A, SN7484A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to any X input in conjunction with any Y input.

recommended operating conditions

	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			40	mA
Width of write pulse, $t_{w(write)}$ (see Figure 1)	20			20			ns
Address input setup time, t_{su} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level voltage at any input			2			2			V
V_{IL}	Low-level voltage at address inputs	to prevent writing				0.8			0.8	V
		to prevent sensing				1			1	
V_{IL}	Low-level voltage at write inputs					0.8			1	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX			0.4			0.4	V
I_I	Input current at maximum input voltage	Write	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		Address				3			3	
I_{IH}	High-level input current	Write	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Address	V_{CC} = MAX, V_I = 4.5 V			400			400	
I_{IL}	Low-level input current	Write	V_{CC} MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Address				−11			−11	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 0 V			70			65	mA
			V_{CC} = 5 V, All inputs at 0 V		45	60		45	60	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

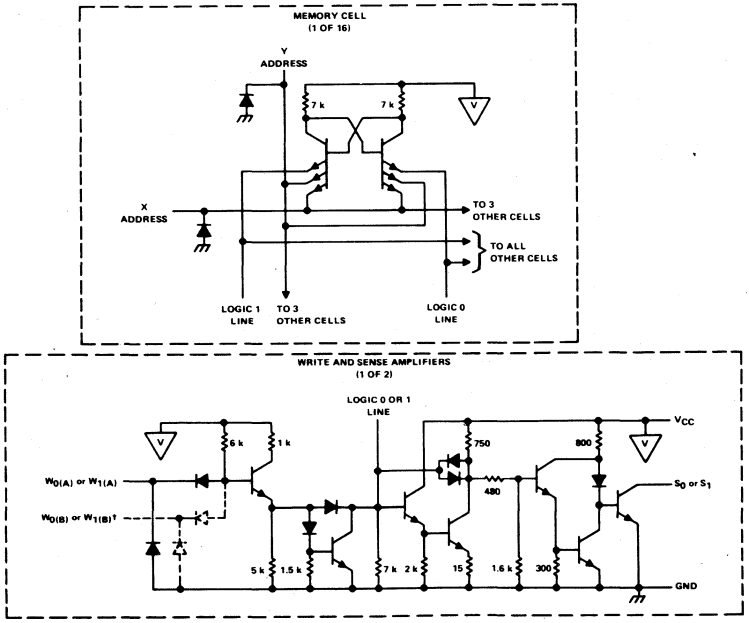
switching characteristics, V_{CC} = 5 V, I_{OL} = MAX†, T_A = 25°C, see figure 1

PARAMETER§	LOCATION ADDRESSED	TEST CONDITIONS	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{SR}	X1 – Y1	C_L = 30 pF		13			13		ns
		C_L = 200 pF		18	30		18	30	
t_{PHL}	X1 – Y1	C_L = 30 pF		11	19		12	20	ns
		C_L = 200 pF		17	26		18	27	
t_{PLH}		C_L = 30 pF		13	20		12	19	
		C_L = 200 pF		27	40		18	27	
t_{PHL}	X1 thru X4 and Y1	C_L = 30 pF		10	18		11	19	ns
		C_L = 200 pF		16	25		17	26	
t_{PLH}		C_L = 30 pF		13	20		13	20	
		C_L = 200 pF		27	40		19	28	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

§ t_{SR} ≡ Sense recovery time after writing
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PLH} ≡ Propagation delay time, low-to-high-level output

schematic

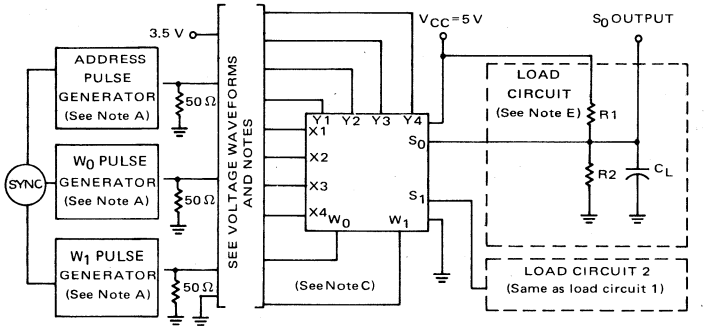


†$W_{0(B)}$ and $W_{1(B)}$ inputs (indicated with dashed lines) are applicable for the SN5484A, SN7484A only.

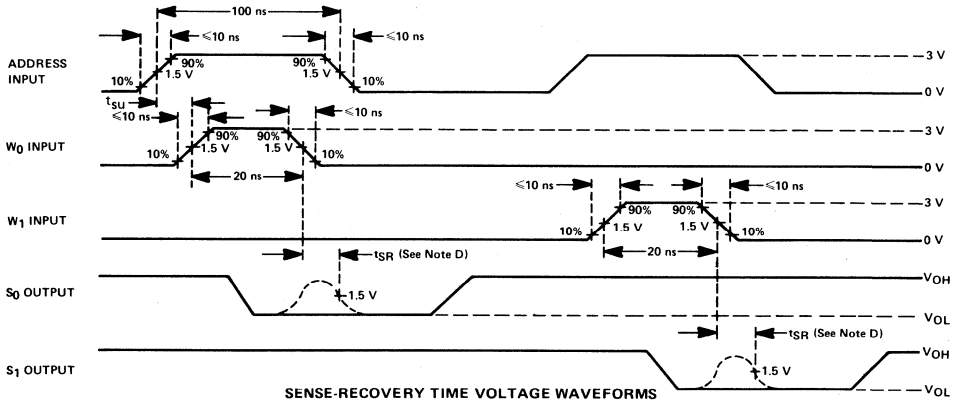
▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

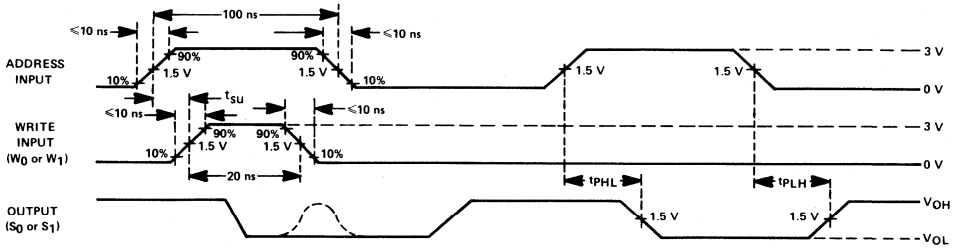
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



SENSE-RECOVERY TIME VOLTAGE WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: for the address pulse generator, PRR = 2 MHz; for the W_0 and W_1 pulse generators, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. For the SN5484A and SN7484A, unused W_0 and W_1 inputs are at 3.5 V.
D. t_{SR} ≡ sense-recovery time
E. For the SN5481A and SN5484A: R1 = 240 Ω and R2 = 560 Ω. For the SN7481A and SN7484A: R1 = 120 Ω and R2 = 330 Ω.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPES SN5482, SN7482
2-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211836, DECEMBER 1972

For applications in:

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

FUNCTION TABLE

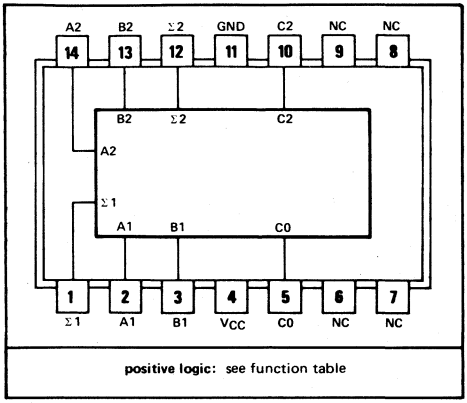
INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

description

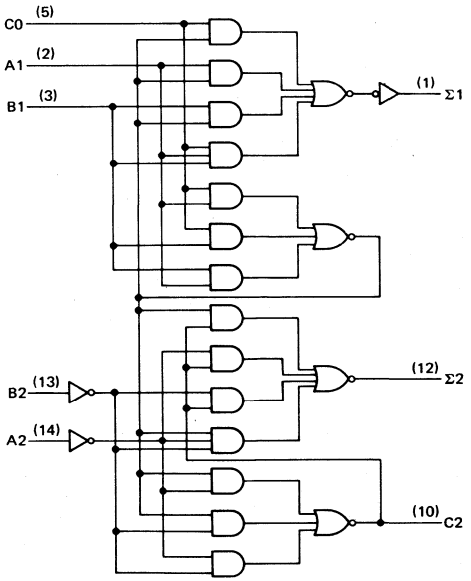
These full adders perform the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, these circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) and are compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

SN5482 . . . J OR W PACKAGE
SN7482 . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5482 Circuits . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN5482			SN7482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Σ1 or Σ2			−400			−400	μA
	C2			−200			−200	
Low-level output current, I_{OL}	Σ1 or Σ2			16			16	mA
	C2			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5482			SN7482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{OH}	High-level output voltage	Σ1 or Σ2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
		C2		I_{OH} = −200 μA							
V_{OL}	Low-level output voltage	Σ1 or Σ2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
		C2		I_{OL} = 8 mA							
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	A1, B1, or C0	V_{CC} = MAX, V_I = 2.4 V				160			160	μA
		A2 or B2					40			40	
I_{IL}	Low-level input current	A1, B1, or C0	V_{CC} = MAX, V_I = 0.4 V				−6.4			−6.4	mA
		A2 or B2					−1.6			−1.6	
I_{OS}	Short-circuit output current§	Σ1 or Σ2	V_{CC} = MAX		−20		−55	−18		−55	mA
		C2			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			35	50		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, B1 and B2 grounded, and 4.5 V applied to A1, A2, and C0.

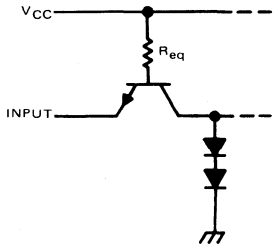
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{PHL}						40	
t_{PLH}	B2	Σ2				40	ns
t_{PHL}						35	
t_{PLH}	C0	Σ2				38	ns
t_{PHL}						42	
t_{PLH}	C0	C2	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{PHL}					17	27	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

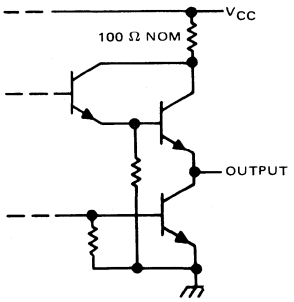
schematics of inputs and outputs

EQUIVALENT OF ALL INPUTS

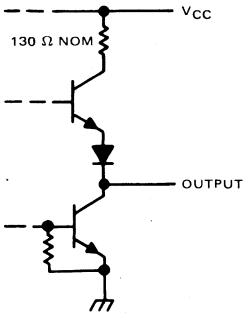


A1, B1, C0: R_{eq} = 1 kΩ NOM
A2, B2: R_{eq} = 4 kΩ NOM

C2 OUTPUT



Σ1 AND Σ2 OUTPUTS



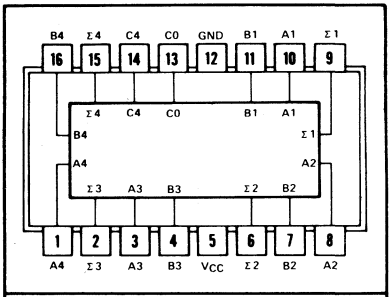
TYPES SN5483A, SN54LS83A, SN7483A, SN74LS83A
4-BIT BINARY FULL ADDERS WITH FAST CARRY

BULLETIN NO. DL-S 7611853, MARCH 1974—REVISED OCTOBER 1976

- **Full-Carry Look-Ahead across the Four Bits**
- **Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry**
- **SN54283/SN74283 and SN54LS283/SN74LS283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout**

TYPE	TYPICAL ADD TIMES: TWO 8-BIT WORDS	TYPICAL ADD TIMES: TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
'83A	23 ns	43 ns	310 mW
'LS83A	25 ns	45 ns	95 mW

SN5483A, SN54LS83A . . . J OR W PACKAGE
SN7483A, SN74LS83A . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These improved full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Designed for medium-speed applications, the circuits utilize transistor-transistor logic that is compatible with most other TTL families and other saturated low-level logic families.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L			OUTPUT: WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

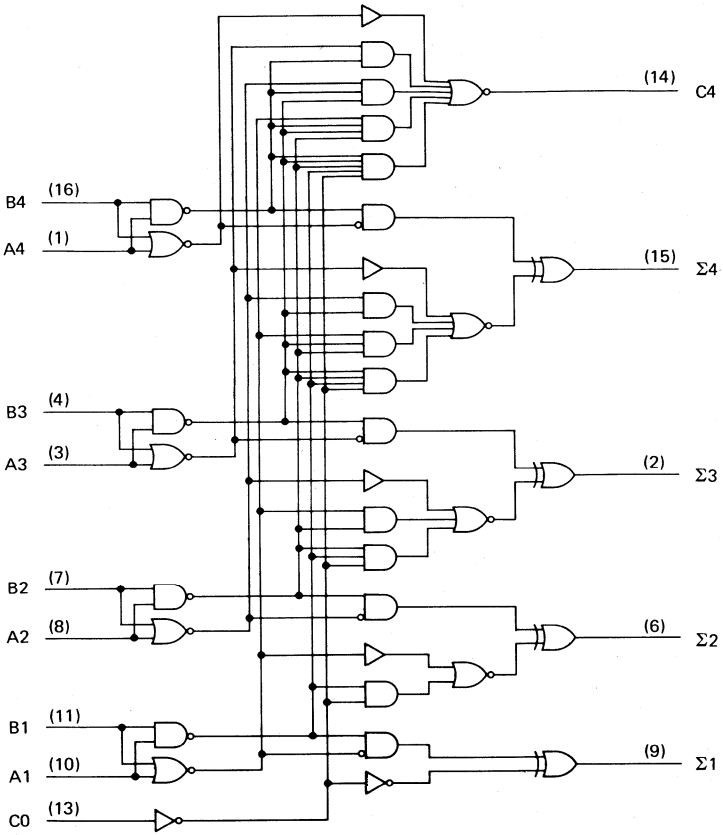
NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '83A	5.5 V
'LS83A	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5483A, SN54LS83A	−55°C to 125°C
SN7483A, SN74LS83A	0°C to 70°C
Storage temperature range	−65°C to 150°C

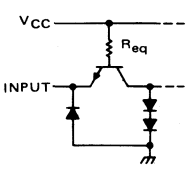
NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '83A only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

functional block diagram



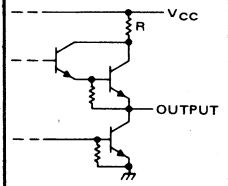
schematics of inputs and outputs

'83A
EQUIVALENT OF EACH INPUT



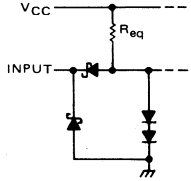
C0 input: R_{eq} = 4 kΩ NOM
Any A or B: R_{eq} = 3.5 kΩ NOM

'83A
TYPICAL OF ALL OUTPUTS



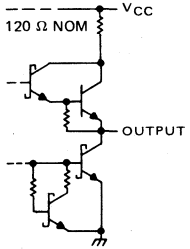
C4 output: R = 100 Ω NOM
Any Σ: R = 120 Ω NOM

'LS83A
EQUIVALENT OF EACH INPUT



C0 input: R_{eq} = 17 kΩ NOM
Any A or B: R_{eq} = 8.5 kΩ NOM

'LS83A
TYPICAL OF ALL OUTPUTS



recommended operating conditions

		SN5483A			SN7483A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−800			−800	μA
	Output C4			−400			−400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5483A			SN7483A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−20		−55	−18		−55	mA
		Output C4			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
				All inputs at 4.5 V		66	99		66	110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 780 Ω, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS83A			SN74LS83A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS83A			SN74LS83A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any A or B	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
		C0					0.1			0.1	
I_{IH}	High-level input current	Any A or B	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		C0					20			20	
I_{IL}	Low-level input current	Any A or B	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		C0					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All inputs grounded		22	39		22	39	mA
				All B low, other inputs at 4.5 V		19	34		19	34	
				All inputs at 4.5 V		19	34		19	34	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 2 kΩ, See Note 4		16	24	ns
t_{PHL}					15	24	
t_{PLH}	A_i or B_i	Σ_i			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					15	22	
t_{PLH}	A_i or B_i	C4			11	17	ns
t_{PHL}					12	17	

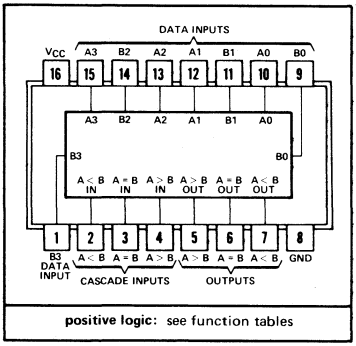
¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
Note 4: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN5485, SN54LS85, SN54S85, SN7485, SN74LS85, SN74S85 4-BIT MAGNITUDE COMPARATORS

BULLETIN NO. DL-S 7611810, MARCH 1974—REVISED OCTOBER 1976

TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'LS85	52 mW	24 ns
'S85	365 mW	11 ns

SN5485, SN54LS85, SN54S85 . . . J OR W PACKAGE
SN7485, SN74LS85, SN74S85 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths of the '85, 'LS85, and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long word. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

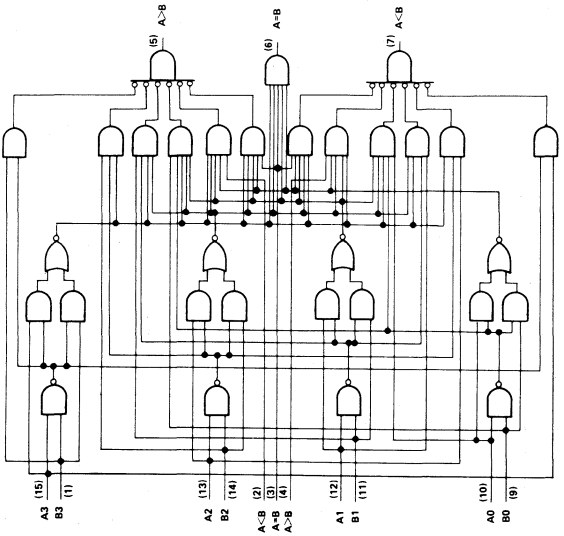
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'LS85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

functional block diagrams

'85, 'LS85, 'S85



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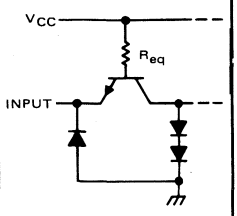
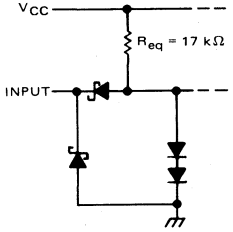
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT FOR '85

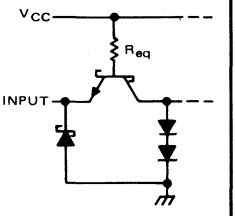


A = B, Any A or B:
R_{eq} = 1.67 kΩ NOM
A > B, A < B:
R_{eq} = 4 kΩ NOM

EQUIVALENT OF EACH INPUT FOR 'LS85

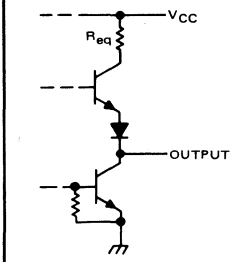


EQUIVALENT OF EACH INPUT FOR 'S85



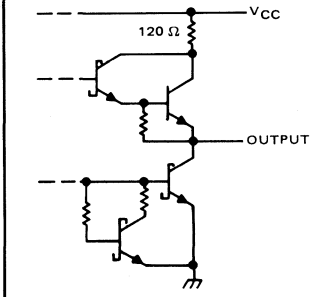
A = B, Any A or B:
R_{eq} = 933 Ω NOM
A > B, A < B:
R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS FOR '85

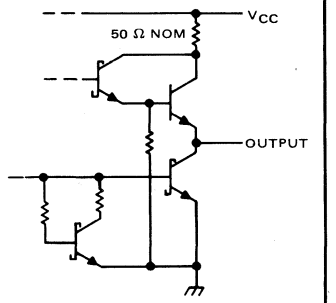


'85: R_{eq} = 100 Ω NOM
'L85: R_{eq} = 500 Ω NOM

TYPICAL OF ALL OUTPUTS FOR 'LS85



TYPICAL OF ALL OUTPUTS FOR 'S85



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54' SN54S'		SN54LS'	SN74' SN74S'		SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7		7	7		7	V
Input voltage	5.5		7	5.5		7	V
Interemitter voltage (see Note 2)	5.5			5.5			V
Operating free-air temperature range	−55 to 125			0 to 70			°C
Storage temperature range	−65 to 150			−65 to 150			°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input of the '85 and 'S85.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		all other inputs					120	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		all other inputs					−4.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0	SN5485	−20		−55	mA
				SN7485	−18		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			55	88	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Note 5		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS85			SN74LS85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS85			SN74LS85			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A < B, A > B inputs	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		all other inputs					0.3			0.3	
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		all other inputs					60			60	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		all other inputs					−1.2			−1.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 4		10.4	20		10.4	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 2 kΩ, See Note 7		14		ns
			2			19		
			3			24	36	
		A = B	4			27	45	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			23	45	
t_{PLH}	A < B or A = B	A > B	1			14	22	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			13	26	ns
t_{PLH}	A > B or A = B	A < B	1			14	22	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S85	2.5	3.4		V
				SN74S85	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 2.7 V				50	μA
		all other inputs					150	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 0.5 V				−2	mA
		all other inputs					−6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			73	115	mA
			V_{CC} = MAX, T_A = 125°C, See Note 4	SN54S85W			110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 280 Ω, See Note 5		5		ns
			2			7.5		
			3			10.5	16	
		A = B	4			12	18	
t_{PHL}	Any A or B data input	A < B, A > B	1			5.5		ns
			2			7		
			3			11	16.5	
		A = B	4			11	16.5	
t_{PLH}	A < B or A = B	A > B	1			5	7.5	ns
t_{PHL}	A < B or A = B	A > B	1			5.5	8.5	ns
t_{PLH}	A = B	A = B	2			7	10.5	ns
t_{PHL}	A = B	A = B	2			5	7.5	ns
t_{PLH}	A > B or A = B	A < B	1			5	7.5	ns
t_{PHL}	A > B or A = B	A < B	1			5.5	8.5	ns

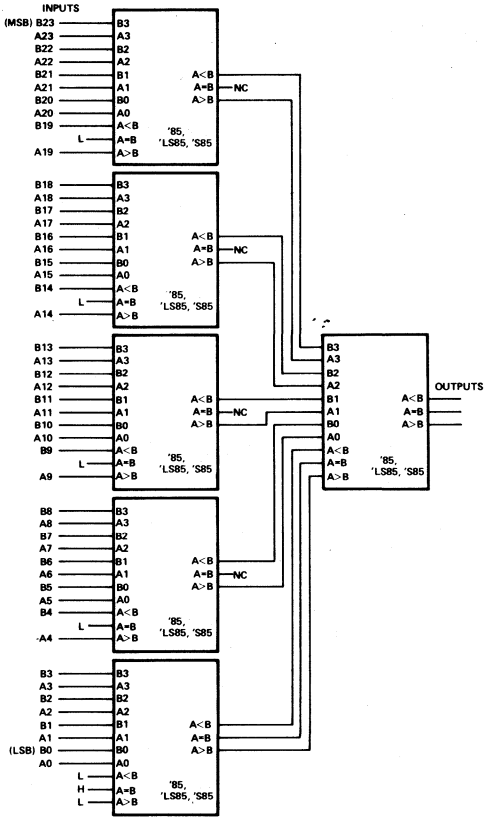
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

TYPICAL APPLICATION DATA

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the design is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'LS85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'LS85	'S85
1-4 bits	1	23 ns	24 ns	11 ns
5-24 bits	2-6	46 ns	48 ns	22 ns
25-120 bits	8-31	69 ns	72 ns	33 ns

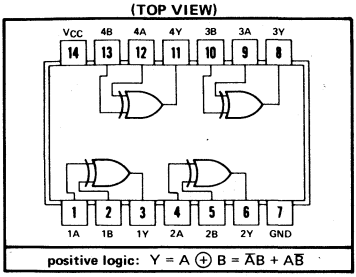


COMPARISON OF TWO 24-BIT WORDS

TYPES SN5486, SN54LS86A, SN54S86, SN7486, SN74LS86A, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

BULLETIN NO. DL-S 7611825, DECEMBER 1972 – REVISED JANUARY 1978

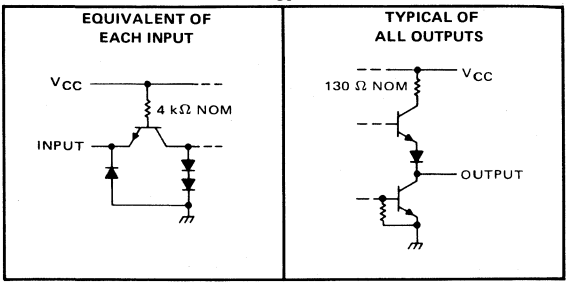
SN54', SN54LS', SN54S' . . . J OR W PACKAGE
SN74', SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)



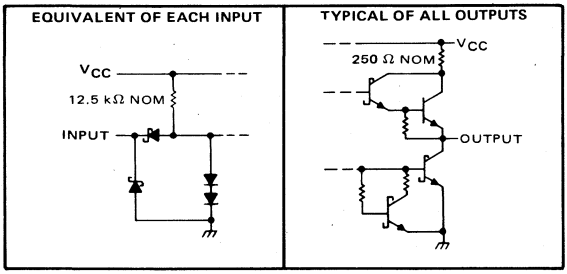
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

schematics of inputs and outputs

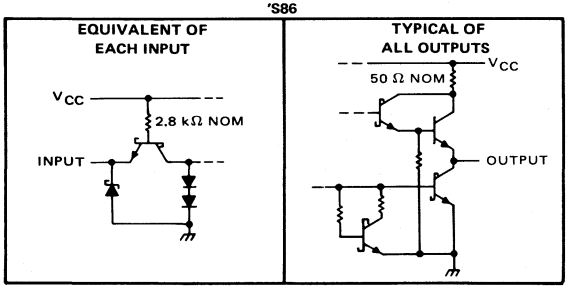
'86



'LS86A



'S86



FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'LS86A	10 ns	30.5 mW
'S86	7 ns	250 mW

7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5486 . . . . . −55°C to 125°C
SN7486 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5486			SN7486			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5486			SN7486			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		30	43		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 400 Ω, See Note 3		15	23	ns
t_{PHL}					11	17	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					13	22	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS86 A . . . . . −55°C to 125°C
SN74LS86 A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS86A			SN74LS86A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS86A			SN74LS86A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 7		12	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			20	30	ns
t_{PHL}					13	22	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S86 . . . . . −55°C to 125°C
SN74S86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S86			SN74S86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		50	75		50	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

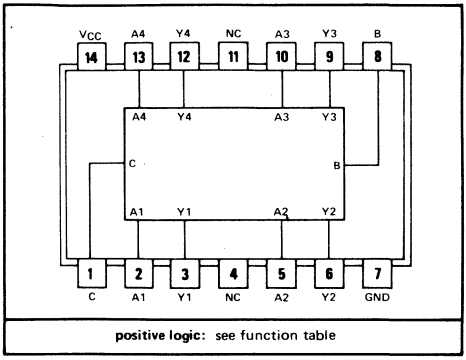
PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 280 Ω, See Note 3		7	10.5	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	Other input high			7	10.5	ns
t_{PHL}					6.5	10	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54H87, SN74H87
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENTS

BULLETIN NO. DL-S 7211837, DECEMBER 1972

SN54H87 . . . J OR W PACKAGE
SN74H87 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

description

Operation of these monolithic 4-bit true/complement elements is controlled by the B and C inputs. With the B input low, the 4-bit binary input (A) is transferred to the output (Y) in either complementary form (with C low) or true form (with C high). When the B input is high, the output will be at the complementary level of the C input regardless of the levels of the data inputs.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the low-level condition.

Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

The SN54H87 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H87 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level
A1, A2, A3, A4 = the level of the respective A input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54H87 Circuits . . . . . −55°C to 125°C
SN74H87 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54H87			SN74H87			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

Phased out types!

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54H87		54	78	mA
			SN74H87		54	89	

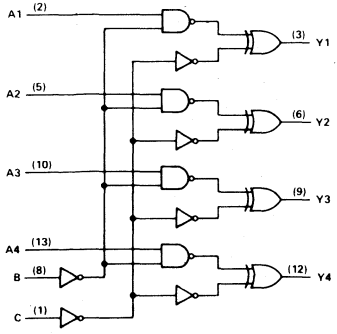
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed 1 second.
NOTE 2: I_{CC} is measured for the following conditions:
a. All A inputs are at 4.5 V, B and C inputs are grounded, and all outputs are open.
b. B and C inputs are at 4.5 V, all A inputs are grounded, and all outputs are open.

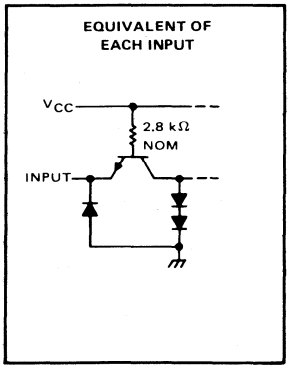
switching characteristics, V_{CC} = 5 V, T_A = 25°C

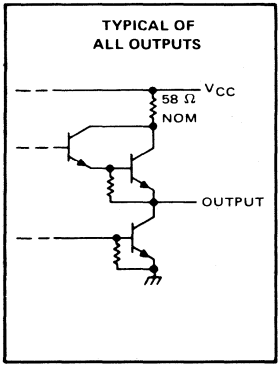
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MAX
t_{PLH}	Propagation delay time, low-to-high-level output from any A input	C_L = 25 pF, R_L = 280 Ω, See Note 3		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any A input			13	19	ns
t_{PLH}	Propagation delay time, low-to-high-level output from B or C inputs			17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from B or C inputs			17	25	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagram and schematics of inputs and outputs







Phased out types!

TYPES SN5490A, SN5492A, SN5493A, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74LS90, SN74LS92, SN74LS93
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

BULLETIN NO. DL-S 7611807, MARCH 1974—REVISED OCTOBER 1976

'90A, 'LS90... DECADE COUNTERS

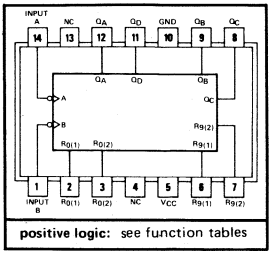
'92A, 'LS92... DIVIDE-BY-TWELVE COUNTERS

'93A, 'LS93... 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW

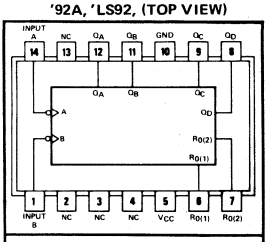
SN54', SN54LS'... J OR W PACKAGE
SN54', SN74LS'... J OR N PACKAGE

'90A, 'LS90 (TOP VIEW)



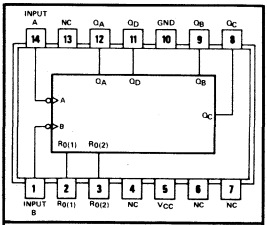
positive logic: see function tables

'92A, 'LS92, (TOP VIEW)



positive logic: see function tables

'93A, 'LS93 (TOP VIEW)



positive logic: see function tables

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A and 'LS93.

All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

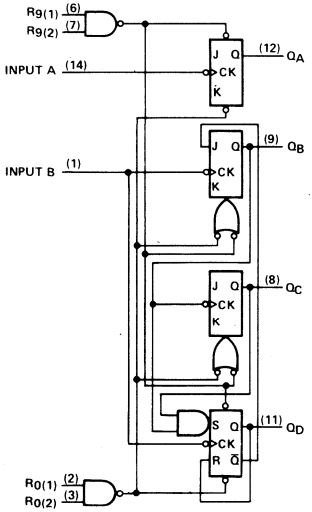
'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

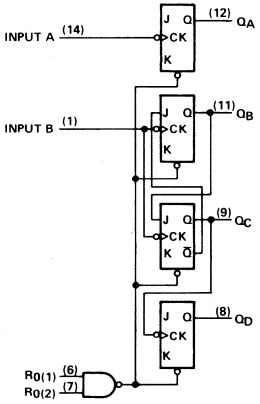
NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagrams

'90A, 'LS90

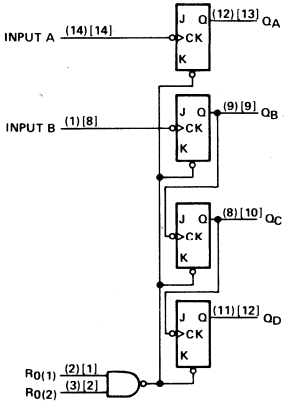


'92A, 'LS92



'93A, 'LS93

('93A) ['L93]

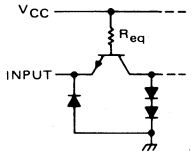


The J and K inputs shown without connection are for reference only and are functionally at a high level.

schematics of inputs and outputs

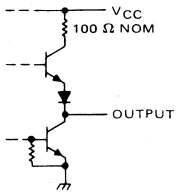
'90A, '92A, '93A

EQUIVALENT OF EACH INPUT



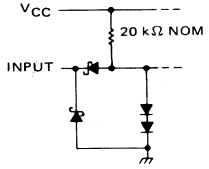
INPUT	R_{eq} NOM
A	2.5 kΩ
B ('90A, '92A)	1.25 kΩ
B ('93A)	2.5 kΩ
All resets	6 kΩ

TYPICAL OF ALL OUTPUTS

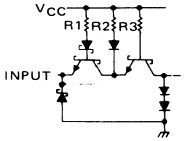


'LS90, 'LS92, 'LS93

EQUIVALENT OF EACH RESET INPUT

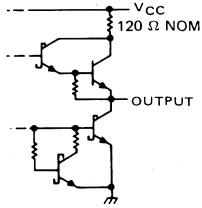


EQUIVALENT OF A AND B INPUTS



INPUT	NOMINAL VALUES R1	R2	R3
A	10 kΩ	10 kΩ	10 kΩ
B ('LS90, 'LS92)	6.7 kΩ	6.7 kΩ	5 kΩ
B ('LS93)	15 kΩ	15 kΩ	10 kΩ

TYPICAL OF ALL OUTPUTS



7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A, SN5493A			SN7490A, SN7492A, SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'90A			'92A			'93A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current, Any reset	V_{CC} = MAX, V_I = 2.4 V				40			40			40	μA
	High-level input current, A input					80			80			80	
	High-level input current, B input					120			120			80	
I_{IL}	Low-level input current, Any reset	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6			−1.6	mA
	Low-level input current, A input					−3.2			−3.2			−3.2	
	Low-level input current, B input					−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
			SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	B	Q_B		16			16			16			
t_{PLH}	A	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	A	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	B	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	B	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage: R inputs . . . . . 7 V
A and B inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 4: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA¶					0.35	0.5	
I_I Input current at maximum input voltage	Any reset	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
	A input	V_{CC} = MAX, V_I = 5.5 V				0.2			0.2	
	B input					0.4			0.4	
I_{IH} High-level input current	Any reset	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
	A input					40			40	
	B input					80			80	
I_{IL} Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	A input					−2.4			−2.4	
	B input					−3.2			−3.2	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 3	'LS90		9	15		9	15	mA
			'LS92		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A Outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS93			SN74LS93			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		A or B input	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		A or B input						40			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		A input						−2.4			−2.4	
		B input						−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			9	15		9	15	mA

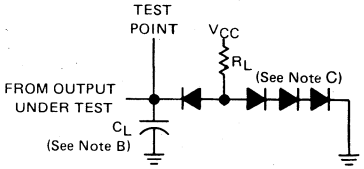
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

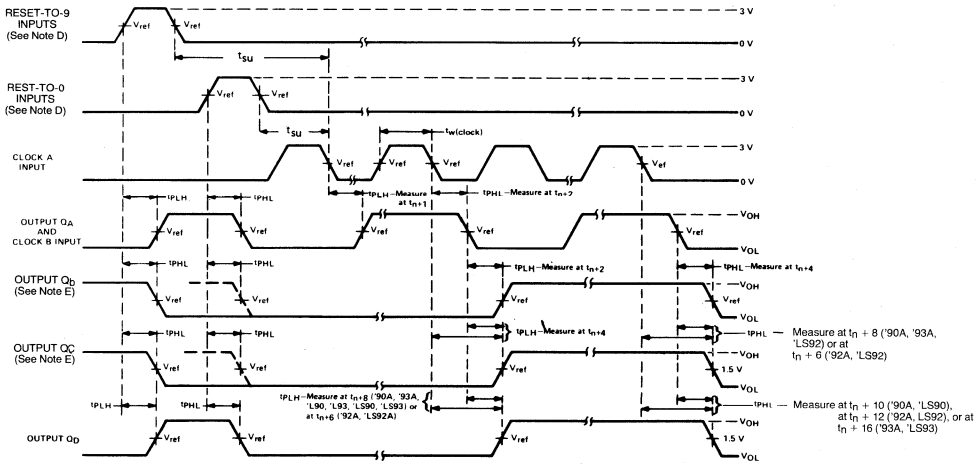
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90			'LS92			'LS93			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	32	42		32	42		32	42		MHz
	B	Q_B		16			16			16			
t_{PLH}	A	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	A	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	B	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	B	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

¶f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or 1 N3064.

D. Each reset input is tested separately with the other reset at 4.5 V.

E. Reference waveforms are shown with dashed lines.

F. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'LS90, 'LS92, and 'LS93; V_{ref} = 1.3 V.

FIGURE 1

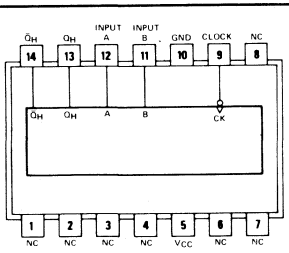
TYPES SN5491A, SN54LS91, SN7491A, SN74LS91
8-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7611854, MARCH 1974—REVISED OCTOBER 1976

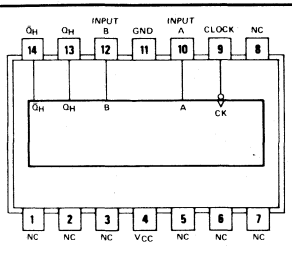
MSI TTL SHIFT REGISTERS
for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

SN5491A, SN54LS91 . . . J PACKAGE
SN7491A, SN74LS91 . . . J OR N PACKAGE
DUAL-IN-LINE PACKAGE (TOP VIEW)



SN5491A, SN54LS91 . . . W PACKAGE
FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

FUNCTION TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q_H	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

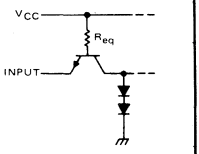
H = high, L = low,
X = irrelevant
t_n = Reference bit time, clock low
t_{n+8} = Bit time after 8 low-to-high clock transitions.

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'91A	18 MHz	175 mW
'LS91	18 MHz	60 mW

schematics of inputs and outputs

'91A

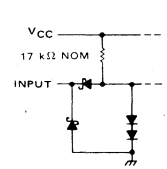
EQUIVALENT OF EACH INPUT



'91A: R_{eq} = 4 kΩ NOM
'L91: R_{eq} = 40 kΩ NOM

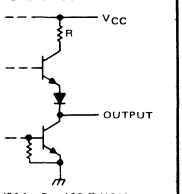
'LS91

EQUIVALENT OF EACH INPUT



'91A

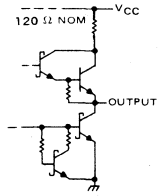
TYPICAL OF BOTH OUTPUTS



'91A: R = 130 Ω NOM
'L91: R = 500 Ω NOM

'LS91

TYPICAL OF BOTH OUTPUTS

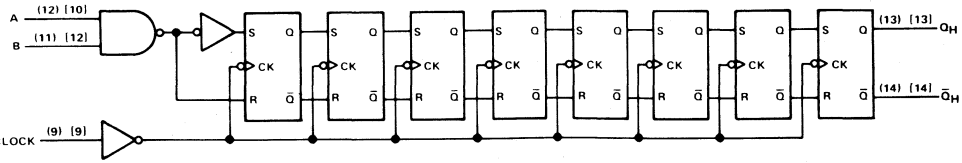


description

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

functional block diagram

(DUAL-IN-LINE) (FLAT PACKAGE)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5491A . . . . . −55°C to 125°C
SN7491A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5491A			SN7491A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{su} (see Figure 1)	25			25			ns
Hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5491A			SN7491A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		35	50		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	10	18		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			24	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output			27	40	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS91 . . . . . −55°C to 125°C
SN74LS91 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS91			SN74LS91			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{su} (see Figure 1)	25			25			ns
Hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

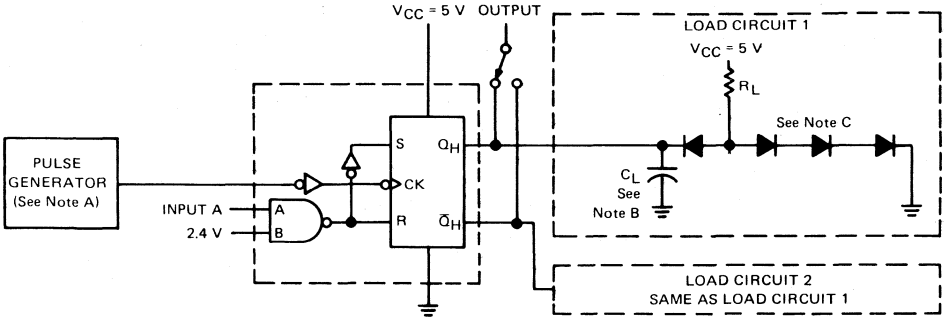
PARAMETER		TEST CONDITIONS†		SN54LS91			SN74LS91			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			12	20		12	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

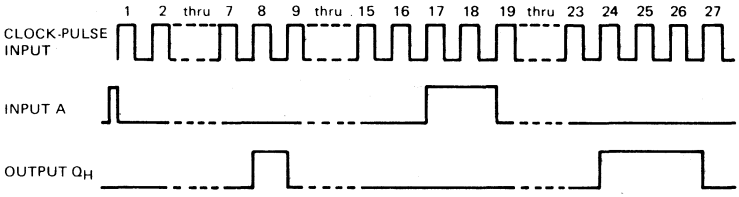
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	10	18		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			24	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output			27	40	ns

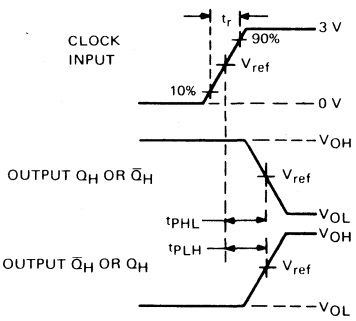
PARAMETER MEASUREMENT INFORMATION



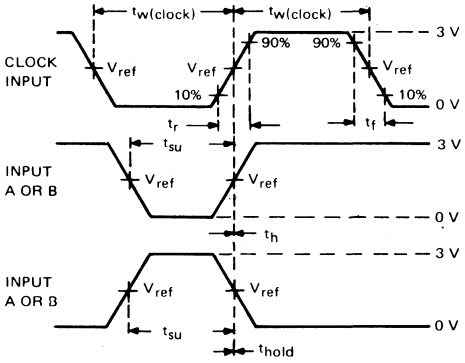
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



SWITCHING TIMES VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: $t_{w(clock)}$ = 500 ns, PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω. For SN5491A/SN7491A, t_r ≤ 10 ns and t_f ≤ 10 ns; and for SN 54LS91/SN74LS91, t_r = 15 ns, and t_f = 6 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. For SN5491A/SN7491A, V_{ref} = 1.5 V; for SN54LS91/SN74LS91, V_{ref} = 1.3 V.

FIGURE 1–SWITCHING TIMES

TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211812, DECEMBER 1972

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS
for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

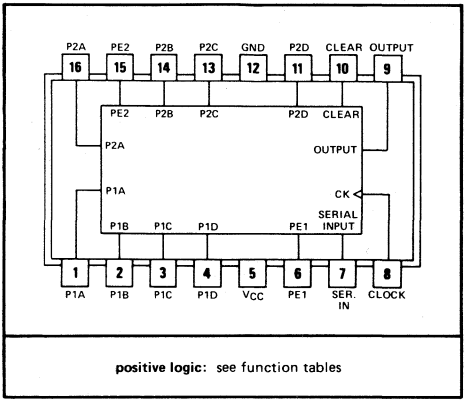
description

These monolithic shift registers which utilize transistor-transistor logic (TTL) circuits in the familiar Series 54/74 configuration, are composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to a low output level by applying a high-level voltage to the clear input while the internal presets are inactive (high). See the preset function table below. Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to either the P1 or P2 inputs of each register stage (A, B, C, and D) with the corresponding preset enable input, PE1 or PE2, high. Presetting, like clearing, is independent of the level of the clock input.

SN5494 . . . J OR W PACKAGE
SN7494 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be setup at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a low level and the internal presets must be inactive (high) when clocking occurs.

PRESET FUNCTION TABLE
(BIT A, TYPICAL OF ALL)

PRESET INPUTS				INTERNAL
PE1	P1A	PE2	P2A	PRESET A
L	X	L	X	H (inactive)
L	X	X	L	H (inactive)
X	L	L	X	H (inactive)
X	L	X	L	H (inactive)
H	H	X	X	L (active)
X	X	H	H	L (active)

REGISTER FUNCTION TABLE

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

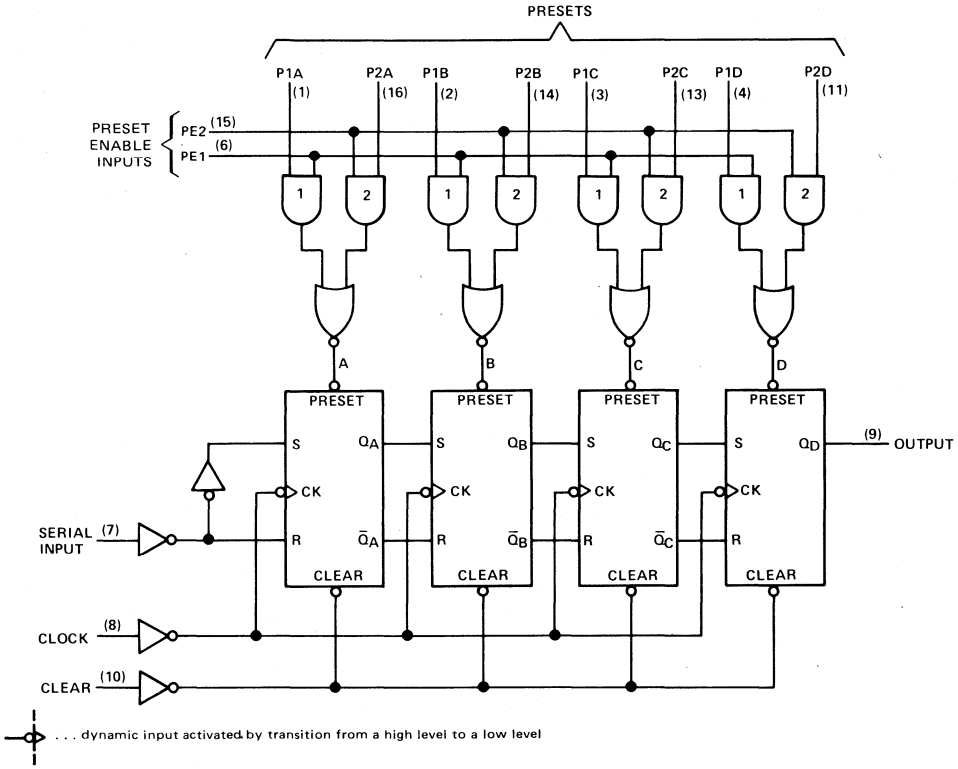
H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

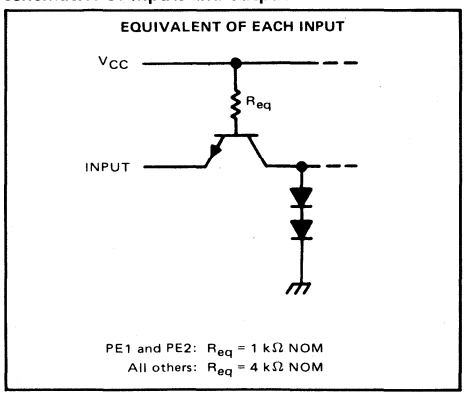
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5494 Circuits . . . . . −55°C to 125°C
SN7494 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

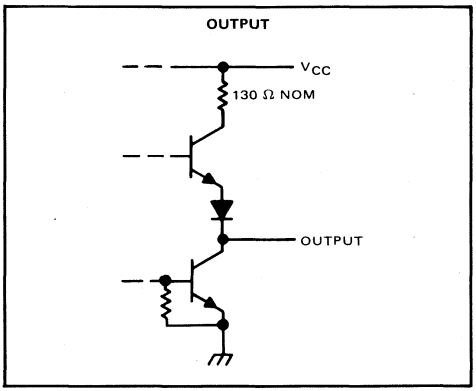
NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

functional block diagram



schematics of inputs and output





recommended operating conditions

		SN5494			SN7494			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, $t_{w(clock)}$		35			35			ns
Width of clear pulse, $t_{w(clear)}$		30			30			ns
Width of preset pulse, $t_{w(preset)}$		30			30			ns
Setup time, t_{su}	High-level data	35			35			ns
	Low-level data	25			25			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5494			SN7494			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 2.4 V			160			160	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 0.4 V			−6.4			−6.4	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		35	50		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the outputs open, clear grounded following momentary application of 4.5 V, both preset-enable inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 4	10			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			25	40	ns
t_{PHL}	Propgaation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset				35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				40	ns

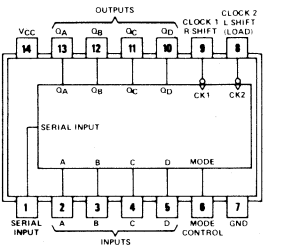
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN5495A, SN54LS95B, SN7495A, SN74LS95B 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7611872, MARCH 1974—REVISED OCTOBER 1976

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'LS95B	36 MHz	65 mW

SN5495A, SN54LS95B . . . J OR W PACKAGE
SN7495A, SN74LS95B . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

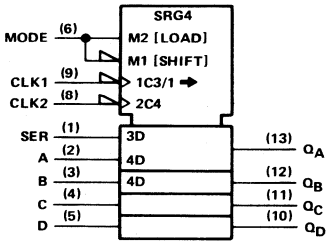
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

logic symbol



FUNCTION TABLE

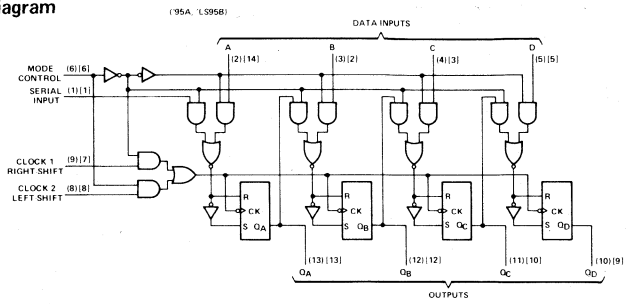
INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

functional block diagram

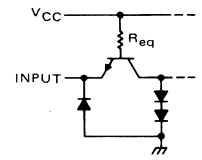
('95A, 'LS95B)



schematics of inputs and outputs

'95A

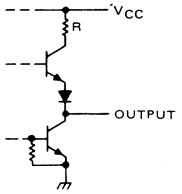
EQUIVALENT OF EACH INPUT



Mode control: R_{eq} = 3 kΩ NOM
Clock inputs: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 6 kΩ NOM

'95A

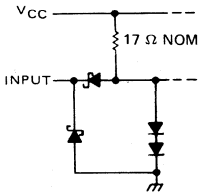
TYPICAL OF ALL OUTPUTS



'95A: R = 100 Ω

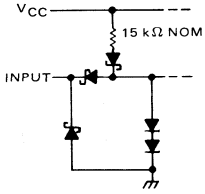
'LS95B

EQUIVALENT OF CLOCK AND MODE CONTROL INPUTS



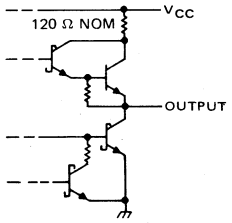
'LS95B

EQUIVALENT OF DATA AND SERIAL INPUTS



'LS95B

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage (see Note 2)	5.5	7	5.5	7	V
Interemitter voltage	5.5		5.5		V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input of the '95A.

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{su} (see Figure 1)	15			15			ns
Hold time, high-level or low-level data, t_h (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	15			15			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	15			15			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	5			5			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5495A			SN7495A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Mode control				80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Mode control				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		39	63		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

recommended operating conditions

	SN54LS95B			SN74LS95B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	25			25			ns
Setup time, high-level or low-level data, t_{su} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_h (see Figure 1)	20			10			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

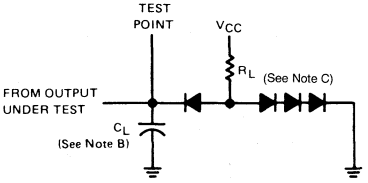
PARAMETER		TEST CONDITIONS†		SN54LS95B			SN74LS95B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4		13	21		13	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

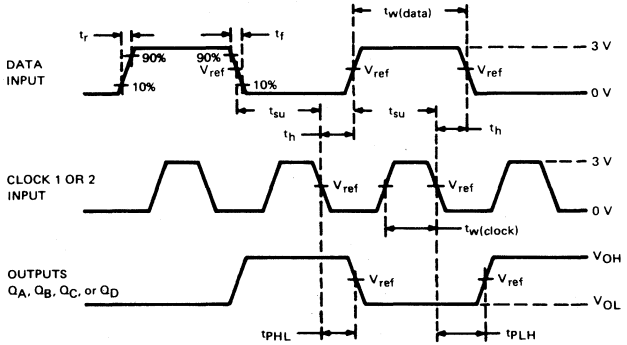
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

PARAMETER MEASUREMENT INFORMATION

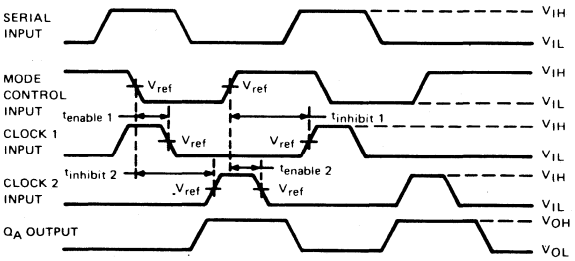


LOAD CIRCUIT



NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing f_{max}, vary PRR. For '95A, $t_{w\ (data)} \geq 20$ ns; $t_{w\ (clock)} \geq 15$ ns. For 'LS95B, $t_{w\ (data)} \geq 20$ ns, $t_{w\ (clock)} \geq 15$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. For '95A, $V_{ref} = 1.5$ V; for 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 1–SWITCHING TIMES



NOTES: A. Input A is at a low level.
B. For '95A, $V_{ref} = 1.5$ V; for 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 2–CLOCK ENABLE/INHIBIT TIMES

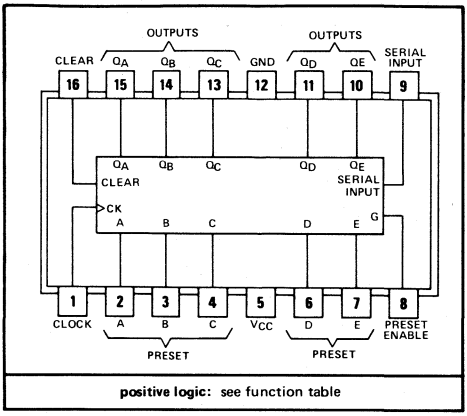
TYPES SN5496, SN54LS96, SN7496, SN74LS96
5-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7611821, MARCH 1974—REVISED OCTOBER 1976

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	TYPICAL PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'96	25 ns	240 mW
'LS96	25 ns	60 mW

SN5496, SN54LS96 . . . J OR W PACKAGE
SN7496, SN74LS96 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

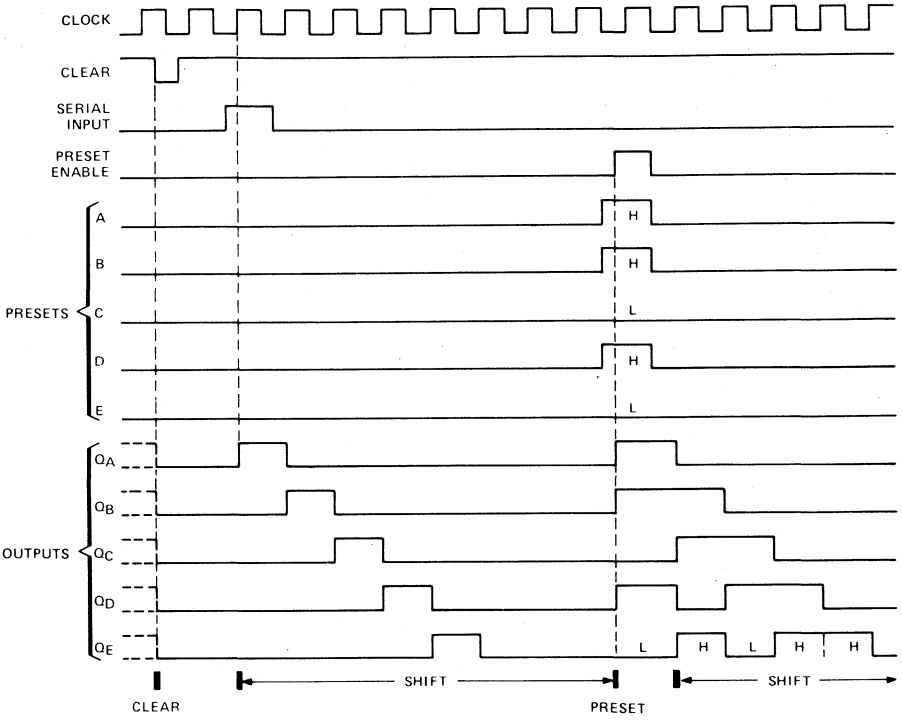
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

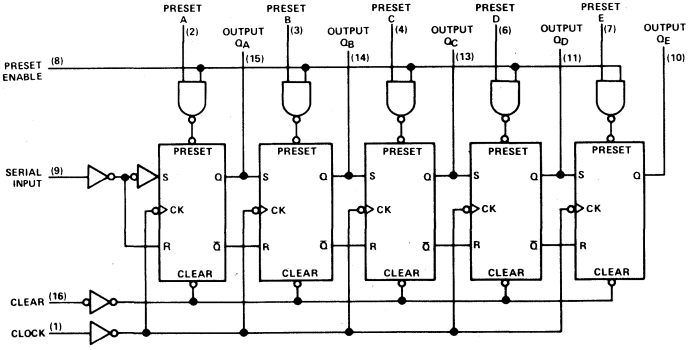
INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	PRESET B	PRESET C	PRESET D	PRESET E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most-recent ↑ transition of the clock.

typical clear, shift, preset, and shift sequences



functional block diagram

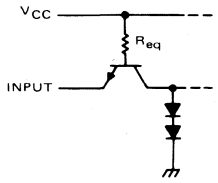


. . . dynamic input activated by transition from a high level to a low level.

schematics of inputs and outputs

'96

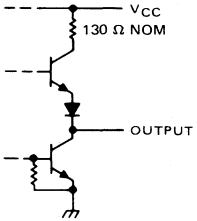
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Preset enable	800 Ω
All others	4 kΩ

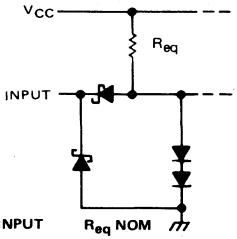
'96

TYPICAL OF ALL OUTPUTS



'LS96

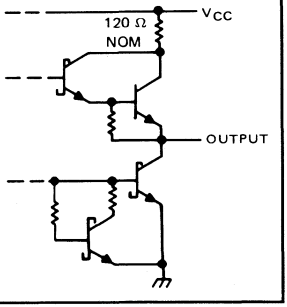
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Serial	25 kΩ
Clock, Clear	17 kΩ
Preset enable	3.4 kΩ

'LS96

TYPICAL OF ALL OUTPUTS



7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5496 . . . . . −55°C to 125°C
SN7496 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_{w(clock)}$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{su} (see Figure 1)	30			30			ns
Serial input hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5496			SN7496			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	any input except preset enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		preset enable				200			200	
I_{IL}	Low-level input current	any input except preset enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		preset enable				−8			−8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		48	68		48	79	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 400 Ω, See Figure 1		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				55	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS96 . . . . . −55°C to 125°C
SN74LS96 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{w(clock)}$	20			20			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

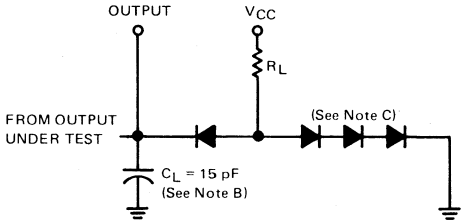
PARAMETER		TEST CONDITIONS†		SN54LS96			SN74LS96			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	Preset enable	V_{CC} = MAX, V_I = 7 V				0.5			0.5	mA
	All others					0.1			0.1	
I_{IH} High-level input current	Preset enable	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
	All others					20			20	
I_{IL} Low-level input current	Preset enable	V_{CC} = MAX, V_I = 0.4 V				−2			−2	mA
	All others					−0.4			−0.4	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 3			12	20		12	20	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

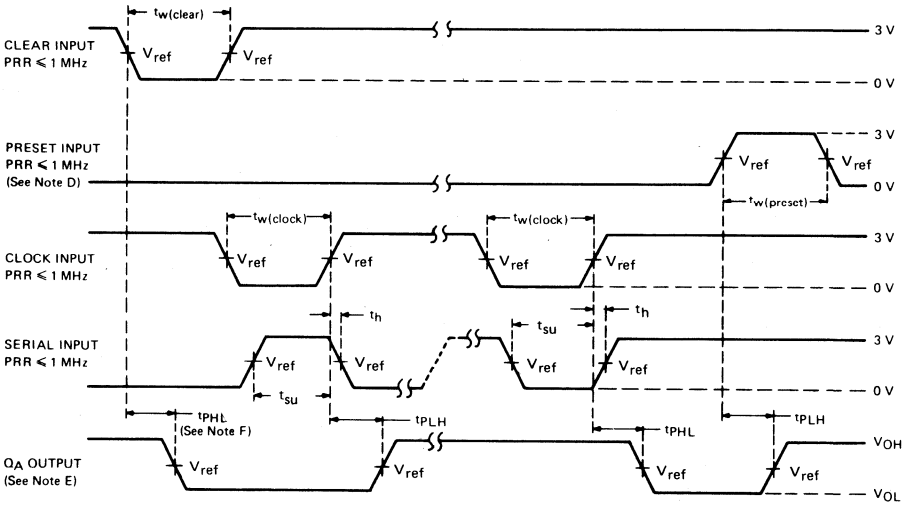
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Figure 1		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '96 and $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS96 $t_r = 15$ ns, $t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
E. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
F. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
G. For '96, $V_{ref} = 1.5$ V; for 'LS96 $V_{ref} = 1.3$ V.

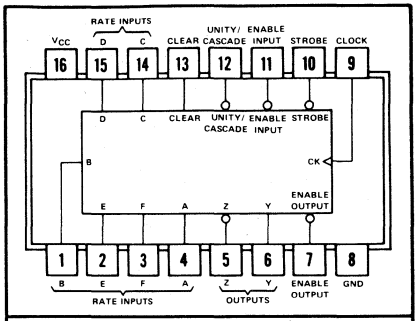
FIGURE 1–SWITCHING TIMES

TYPES SN5497, SN7497
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

BULLETIN NO. DL-S 7611802, DECEMBER 1972—REVISED OCTOBER 1976

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN5497 . . . J OR W PACKAGE
SN7497 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

$$f_{out} = \frac{M \cdot f_{in}}{64}$$

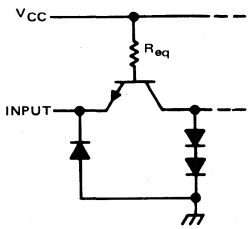
where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

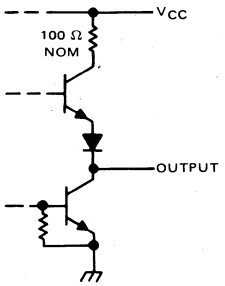
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Clock input: R_{eq} = 2 kΩ NOM
Other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



description (continued)

STATE AND/OR RATE FUNCTION TABLE (See Note A)

INPUTS											OUTPUTS			
			BINARY RATE						NUMBER OF	UNITY/	LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	CLOCK PULSES	CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	D
L	L	L	H	L	H	L	L	L	64	H	40	40	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.

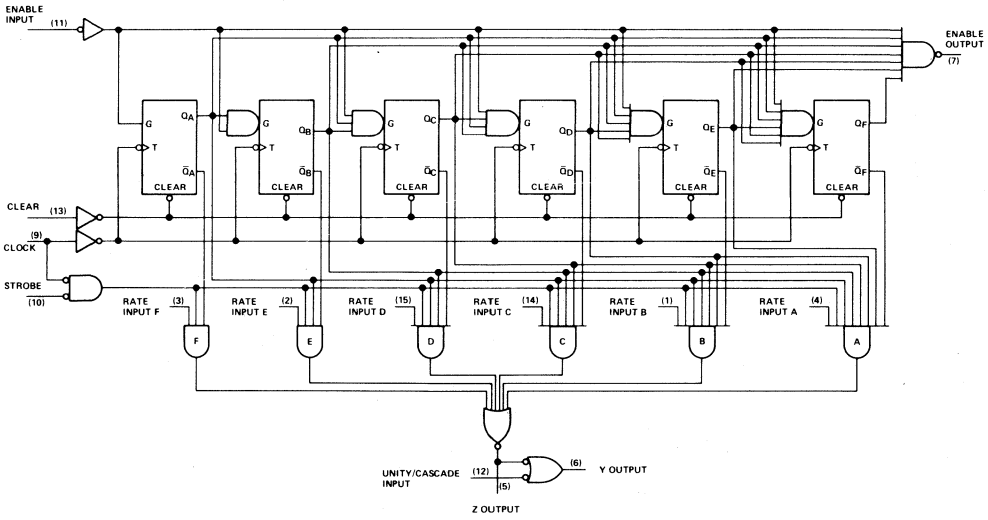
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. Unity/cascade is used to inhibit output Y.

E. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5497 (see Note 2) . . . . . −55°C to 125°C
SN7497 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN5497			SN7494			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Enable setup time, t_{su}: (See Figure 1)							
Before positive-going transition of clock pulse	25			25			ns
Before negative-going transition of previous clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	
Enable hold time, t_h: (See Figure 1)							
After positive-going transition of clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
After negative-going transition of previous clock pulse	20		$t_{cp}-10$	20		$t_{cp}-10$	
Operating free-air temperature, T_A (See Note 2)	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock input	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX,	See Note 3		58		mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX,	See Note 4		80	120	mA

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 1. Voltage values are with respet to network ground terminal.
2. An SN5497 in the W package operating at free-air temperatures above 118°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 55°C/W.
3. I_{CCH} is measured with outputs open and all inputs grounded.
4. I_{CCL} is measured with outputs open and all inputs at 4.5 V.

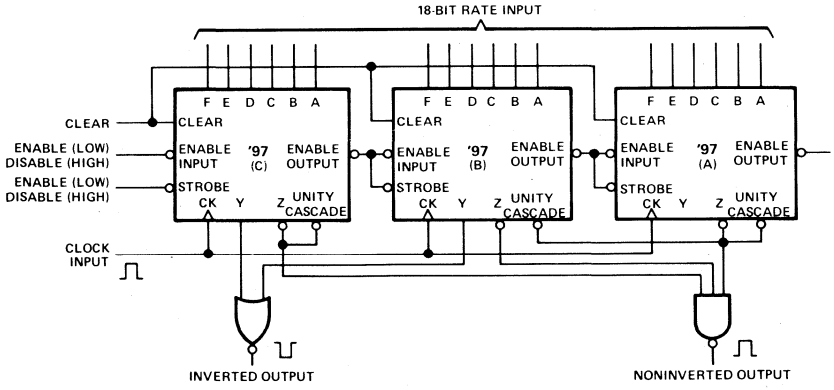
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETERS¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			6	10	ns
t_{PHL}					9	14	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶ f_{max} ≡ maximum clock frequency.
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.

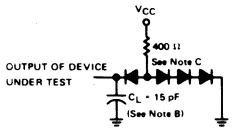
TYPICAL APPLICATION DATA

This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.



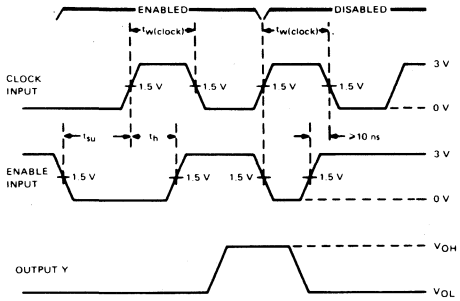
As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.

PARAMETER MEASUREMENT INFORMATION

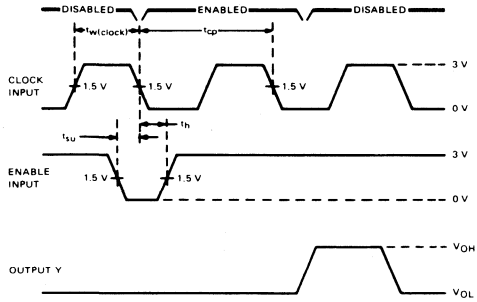


All three outputs are loaded during testing

LOAD CIRCUIT

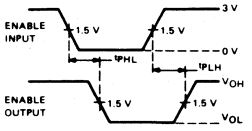


ENABLING FROM POSITIVE-GOING TRANSITION OF CLOCK PULSE



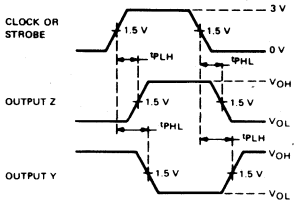
ENABLING FROM NEGATIVE-GOING TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/Cascade and pin 2 (rate input) are high, other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.



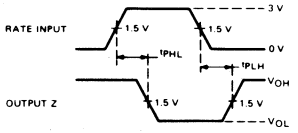
Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT



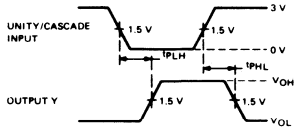
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



Flip-flops are at a count so that all other inputs to the gate under test are high and all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y

NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)}$ = 20 ns, $t_{TLH} \leq$ 10 ns, $t_{THL} \leq$ 10 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

TYPES SN54100, SN74100
8-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7211830, DECEMBER 1972

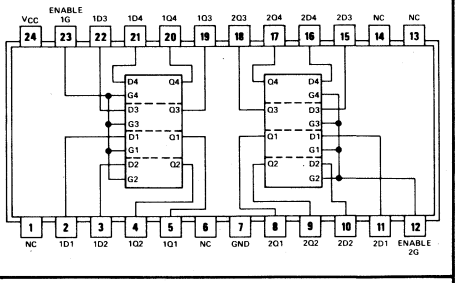
logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

SN54100 . . . J OR W PACKAGE
SN74100 . . . J, N OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

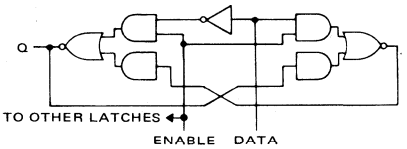
NC—No internal connection

description

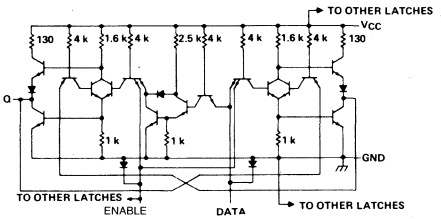
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch. The SN54100 is characterized for operation over the full military temperature range of −55° to 125°C; the SN74100 is characterized for operation from 0°C to 70°C.

functional block diagram (each latch)



schematic (each latch)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Intermitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54100 . . . . . −55°C to 125°C
SN74100 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For this circuit, this rating applies between the enable and D inputs of any latch.

recommended operating conditions

	SN54100			SN74100			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		G input					320	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		G input					−12.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54100	−20		−57	mA
				SN74100	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54100		64	92	mA
				SN74100		64	106	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Note 4		16	30	ns
t_{PHL}					14	25	
t_{PLH}	G	Q			16	30	ns
t_{PHL}					7	15	

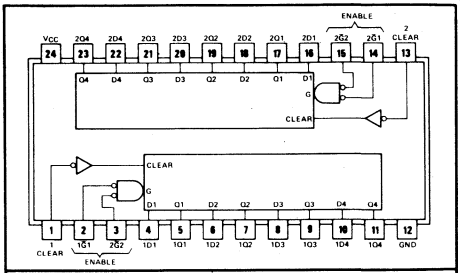
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Test circuit and voltage waveforms are the same as those shown for the '75, '77, on page 7-34.

TYPES SN54116, SN74116
DUAL 4-BIT LATCHES WITH CLEAR

BULLETIN NO. DL-S 7211849, DECEMBER 1972

- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading and Register Implementations
- Compatible for Use with TTL and DTL Circuits
- Input Clamping Diodes Simplify System Design

SN54116 . . . J OR W PACKAGE
SN74116 . . . J, N OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

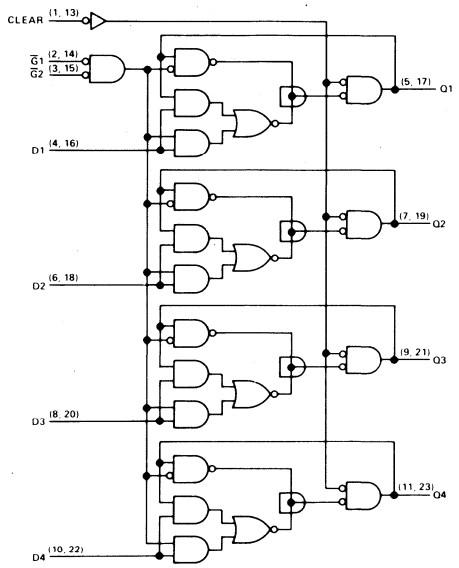
The SN54116 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74116 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{G1}$	ENABLE $\overline{G2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

functional block diagram (each 4-bit latch)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54116 Circuits . . . . . −55°C to 125°C
SN74116 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54116			SN74116			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Input pulse width, t_w	Enable	18			18			ns
	Clear	18			18			
Data setup time, t_{su}	High logic level	8			8			ns
	Low logic level	14			14			
Clear inactive-state setup time, t_{su}		8			8			ns
Data release time, high-level data, $t_{release}$				2			2	ns
Data hold time, low-level data, t_h		8			8			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Any D					60	
I_{IL}	Low-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Any D, initial peak					−2.4	
		Any D, steady-state					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54116	−20		−57	mA
				SN74116	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		60	100	mA
				Condition B		40	70	

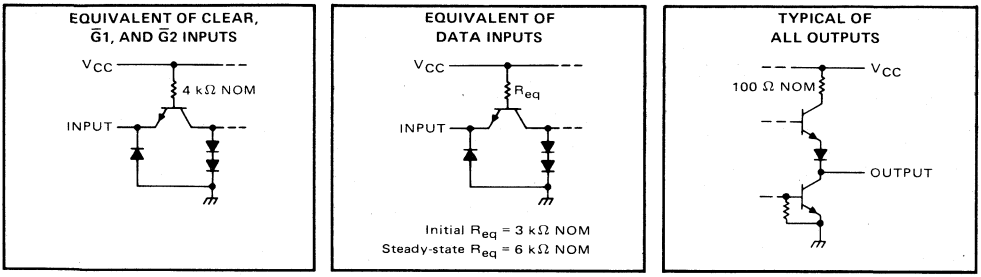
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With outputs open, I_{CC} is measured for the following conditions:
A. All inputs grounded.
B. All $\overline{G}$ inputs are grounded and all other inputs are at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

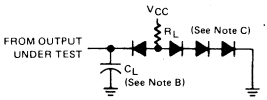
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	Clear	Any Q			15	22	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

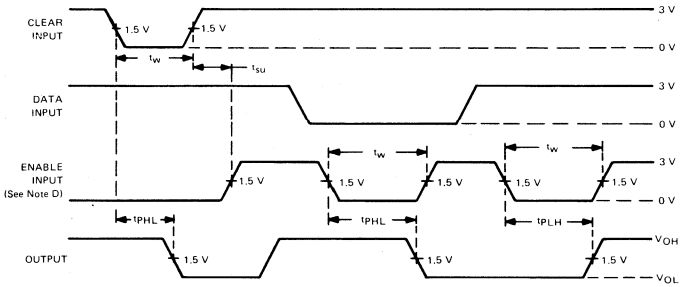
schematics of inputs and outputs



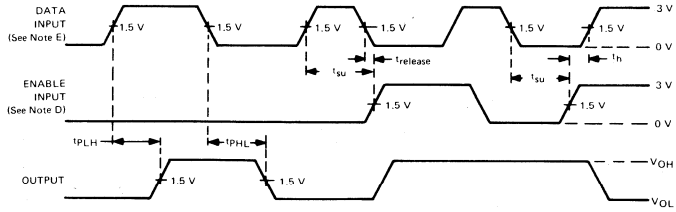
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



SWITCHING TIMES FROM CLEAR AND ENABLE INPUTS



SWITCHING TIMES FROM DATA INPUTS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. The other enable input is low.
E. Clear input is high.

FIGURE 1

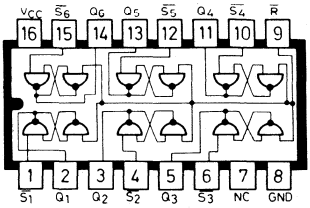
A SERIES 54/74 BISTABLE ELEMENT

for application in – • Digital Computer Systems • Control Systems • Data Handling Systems

LOGIC

TRUTH TABLE (each latch)		
S	Reset	Q
0	X	1
1	0	0
1	1	Store

NOTES: 1. X indicates input may be logical 1 or 0
2. Reset is common to all latches



DESCRIPTION

This monolithic circuit employs standard TTL NAND gates. Cross-coupled to form six set-rest flip-flops in a 16-pin package. Each latch has a set input and a TTL output.

There is also an unbuffered common reset line to facilitate external reset of the complete latch array.

This circuit is ideally suited to event storage and indication in large systems and will reduce the package count needed to produce this function.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{IN} (See Notes 1 & 2)	5.5 V
Operating Free-Air Temperature Range:	
SN 54118N	−55°C to 125°C
SN 74118N	0°C to 70°C
Storage Temperature Range	−55°C to 150°C

Electrical Characteristics (Over Free-Air Temperature Range Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{in} (1) Logical 1 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN V_{out} (0) = 0.4 V	2			V
V_{in} (0) Logical 0 input voltage required at any input terminal to ensure logical 1 level at output.	V_{CC} = MIN V_{out} = 2.4 V			0.8	V
V_{out} (1) Logical 1 output voltage	V_{CC} = MIN I_{LOAD} = −800 μA V_{IN} (set) = 0.8 V V_{IN} (reset) = GND	2.4	3.3		V
V_{out} (0) Logical 0 output voltage	V_{CC} = MIN $I_{S\ INK}$ = 16 mA V_{IN} (set) = 2 V V_{IN} (reset) = 0.8 V	0.22	0.4		V
I_{in} (0) Logical 0 level input current at set/reset inputs	V_{CC} = MAX V_{in} = 0.4 V			−1.6	mA
I_{in} (0) Logical 0 level input current at common reset input	V_{CC} = MAX V_{in} = 0.4 V			− 8	mA
I_{in} (1) Logical 1 level input current at set/reset inputs	V_{CC} = MAX V_{in} = 2.4 V V_{CC} = MAX V_{in} = 5.5 V			40 1	μA mA
I_{in} (1) Logical 1 level input current at common reset input	V_{CC} = MAX V_{in} = 2.4 V V_{CC} = MAX V_{in} = 5.5 V			200 1	μA mA
I_{os} Short circuit output current	V_{CC} = MAX	−18		−55	mA
I_{CC} Total supply current			30	60	mA

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Unit
Supply Voltage V_{CC} (See Note 1)	SN54118N	4.5	5	5.5	V
	SN74118N	4.75	5	5.25	V
Maximum Fan-Out from Each Output (N)			10		

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be ZERO or positive with respect to network ground terminal.

SWITCHING CHARACTERISTICS V_{CC} = 5 V T_A = 25°C N = 10.

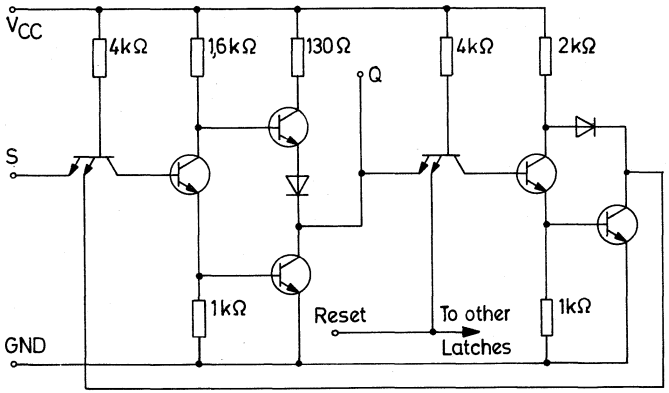
Parameter		Test Conditions	Min	Typ	Max	Unit
t_{pd0}	Propagation delay time to logical 0 level from reset	C_1 = 15 pF N = 10		18	29	ns
t_{pd1}	Propagation delay time to logical 1 level from set	C_1 = 15 pF N = 10		18	29	ns
t_{pd0}	Propagation delay time to logical 0 level from set	C_1 = 15 pF N = 10		10	17	ns

NOTES: + For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time.

SCHEMATIC (Each Latch)



RESISTOR VALUES SHOWN ARE NOMINAL

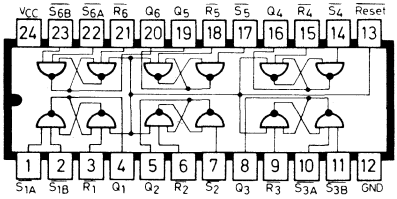
TYPES SN54119/SN74119
HEX SET-RESET LATCH

A SERIES 54/74 BISTABLE ELEMENT

for application in – • Digital Computer Systems • Control Systems • Data Handling Systems

LOGIC

TRUTH TABLE (each latch)				
SA	SB	R	Reset	Q
0	X	X	X	1
X	0	X	X	1
1	1	0	X	0
1	1	X	0	0
1	1	1	1	Store



NOTES: 1. X indicates input may be logical 1 or 0
2. Reset is common to all latches
3. Set B on three latches only

DESCRIPTION

This monolithic circuit employs standard TTL NAND gates, cross-coupled to form six set-rest flip-flops in a 24-pin package. Each latch has one set and one reset input (three latches have two set inputs) and one TTL output.

There is also an unbuffered common reset line to facilitate external reset of the complete latch array.

This circuit is ideally suited to event storage and indication in large systems and will reduce the package count needed to produce this function.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{IN} (See Notes 1 & 2)	5.5 V
Operating Free-Air Temperature Range	
SN 54118N	−55°C to 125°C
SN 74118N	0°C to 70°C
Storage Temperature Range	−55°C to 150°C

Electrical Characteristics (Over Free-Air Temperature Range Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{in} (1) Logical 1 input voltage required at any input terminal to ensure logical 0 level at output	V_{CC} = MIN V_{out} (0) = 0.4 V	2			V
V_{in} (0) Logical 0 input voltage required at any input terminal to ensure logical 1 level at output.	V_{CC} = MIN V_{out} = 2.4 V			0.8	V
V_{out} (1) Logical 1 output voltage	V_{CC} = MIN I_{LOAD} = −800 μA V_{IN} (set) = 0.8 V V_{IN} (reset) = GND	2.4	3.3		V
V_{out} (0) Logical 0 output voltage	V_{CC} = MIN I_S INK = 16 mA V_{IN} (set) = 2 V V_{IN} (reset) = 0.8 V	0.22	0.4		V
I_{in} (0) Logical 0 level input current at set/reset inputs	V_{CC} = MAX V_{in} = 0.4 V			−1.6	mA
I_{in} (0) Logical 0 level input current at common reset input	V_{CC} = MAX V_{in} = 0.4 V			− 8	mA
I_{in} (1) Logical 1 level input current at set/reset inputs	V_{CC} = MAX V_{in} = 2.4 V V_{CC} = MAX V_{in} = 5.5 V			40 1	μA mA
I_{in} (1) Logical 1 level input current at common reset input	V_{CC} = MAX V_{in} = 2.4 V V_{CC} = MAX V_{in} = 5.5 V			200 1	μA mA
I_{os} Short circuit output current	V_{CC} = MAX	−18		−55	mA
I_{CC} Total supply current			30	60	mA

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Unit
Supply Voltage V_{CC} (See Note 1)	SN54119N	4.5	5	5.5	V
	SN74119N	4.75	5	5.25	V
Maximum Fan-Out from Each Output (N)			10		

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be ZERO or positive with respect to network ground terminal.

SWITCHING CHARACTERISTICS V_{CC} = 5 V T_A = 25°C N = 10.

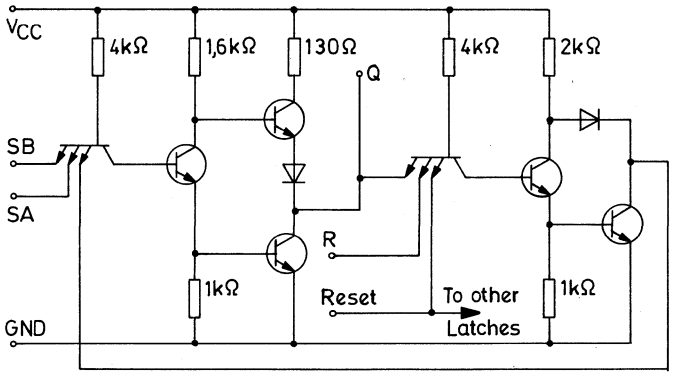
Parameter		Test Conditions	Min	Typ	Max	Unit
t_{pd0}	Propagation delay time to logical 0 level from reset	C_1 = 15 pF N = 10		18	29	ns
t_{pd1}	Propagation delay time to logical 1 level from set	C_1 = 15 pF N = 10		18	29	ns
t_{pd0}	Propagation delay time to logical 0 level from set	C_1 = 15 pF N = 10		10	17	ns

NOTES: + For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time.

SCHEMATIC (Each Latch)



RESISTOR VALUES SHOWN ARE NOMINAL
SB ON THREE LATCHES ONLY.

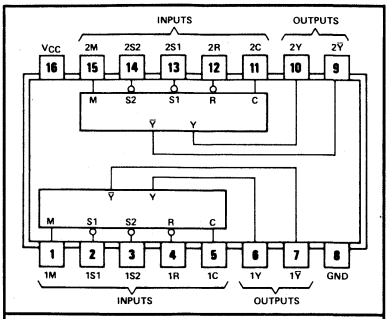
TYPES SN54120, SN74120
DUAL PULSE SYNCHRONIZERS/DRIVERS

BULLETIN NO. DL-S 7211537, SEPTEMBER 1971—REVISED DECEMBER 1972

- Generates Either a Single Pulse or Train of Pulses Synchronized with Control Functions
- Ideal for Implementing Sync-Control Circuits Similar to those Used in Oscilloscopes
- Latched Operation Ensures that Output Pulses Are Not Clipped
- High-Fan-Out Complementary Outputs Drive System Clock Lines Directly
- Internal Input Pull-Up Resistors Eliminate Need for External Components
- Diode-Clamped Inputs Simplify System Design
- Typical Propagation Delays:

  9 Nanoseconds through One Level
  16 Nanoseconds through Two Levels

SN54120 . . . J OR W PACKAGE
SN74120 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These monolithic pulse synchronizers are designed to synchronize an asynchronous or manual signal with a system clock. Reliable response is ensured as the input signals are latched up; therefore duration of logic input is not critical and the adverse effects of contact-bounce of a manual input are eliminated. The ability to pass output pulses is started and stopped by the levels or pulses applied to the latch inputs S1, S2, or R in accordance with the function table. High-speed circuitry is utilized throughout the clock paths to minimize skew with respect to the system clock.

After initiation, the mode control (M) input determines whether a series of pulses or only one pulse is passed. In the absence of a stop command, the clock driver will continue to pass clock pulses as long as the mode control input is low (see Figures 2 through 4). After the mode control input is taken high, only a single clock pulse will be passed (see figure 5).

When the mode control is set to pass a series of pulses, the last pulse out is determined by two general rules:

a. When pulses are terminated by the S or R inputs, conditions meeting the setup times (specified under recommended operating conditions) will dominate.

FUNCTION TABLE

INPUTS			FUNCTION
R	S1	S2	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

H = high level (steady state)
L = low level (steady state)
↓ = transition from H to L
X = irrelevant
†Operation initiated by last ↓ transition continues.

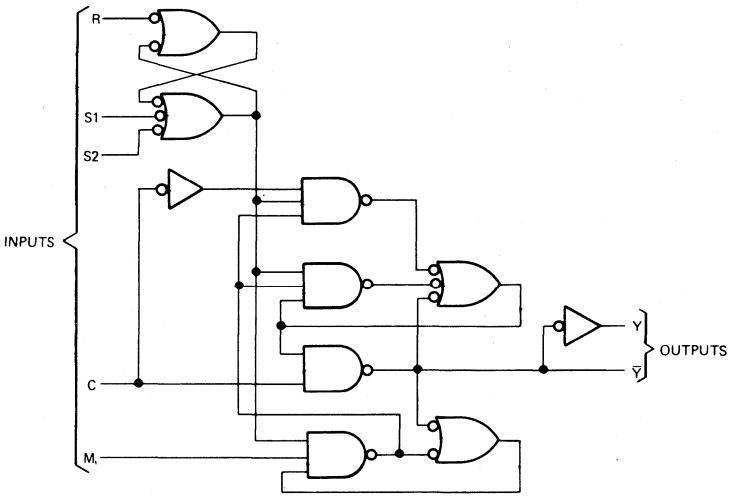
b. Low-to-high-level transitions at the mode control input should be avoided during the 20-nanosecond period immediately following the negative transition of the input clock pulse as transitions during this time period may or may not allow the next pulse to pass (see Figures 4 and 5). When pulses are terminated by the mode control input, a positive transition at the mode control input meeting the high-level setup time, t_{su} (H), (specified under recommended operating conditions) will pass that positive clock pulse then inhibit remaining clock pulses. The clock input (C) is latch-controlled ensuring that once initiated the output pulse will not be terminated until the full pulse has been passed.

description (continued)

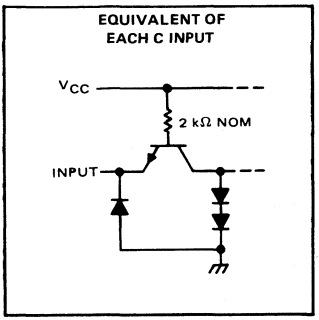
This clock driver circuit is entirely compatible for use with either digital logic circuits or mechanical switches for input controls since all inputs, except the clock, have internal pull-up resistors. This eliminates the requirement to supply an external resistor to prevent the input from floating when the control switch is open. The internal resistor also means that these inputs may be left disconnected if unused.

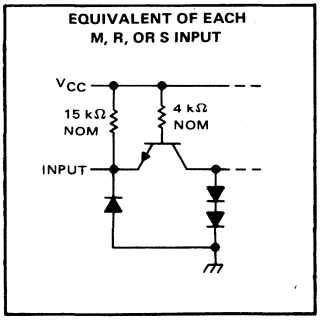
Typical propagation delay time is 9 nanoseconds to the $\overline{Y}$ output and 16 nanoseconds to the Y output from the clock input. The outputs will drive 60 Series 54/74 loads at a high logic level and 30 loads at a low logic level. Typical power dissipation is 127 milliwatts per driver. The SN54120 is characterized for operation from −55°C to 125°C; the SN74120 is characterized for operation from 0°C to 70°C.

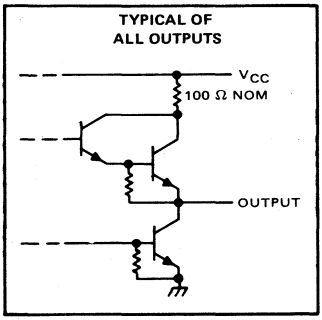
functional block diagram (each driver)



schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54120 Circuits . . . . . −55°C to 125°C
SN74120 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the S1 and S2 inputs.

recommended operating conditions

			SN54120			SN74120			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					−2.4			−2.4	mA
Low-level output current, I_{OL}					48			48	mA
Setup time (see Figures 2 thru 5)	Any input except mode control, t_{su}(H or L)		12			12			ns
	Mode control	t_{su}(H)	0			0			
		t_{su}(L)	12			12			
Hold time (see Figures 3 and 5)	Any input except mode control, t_h(H or L)		3			3			ns
	Mode control, t_h(H or L)		20			20			
Operating free-air temperature, T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 48 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Clock input	V_{CC} = MAX, V_I = 2.4 V			80	μA
		Other inputs		−0.12	−0.2	−0.36	mA
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX, V_I = 0.4 V			−3.2	mA
		Other inputs				−2.1	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−35		−90	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		51	90	mA

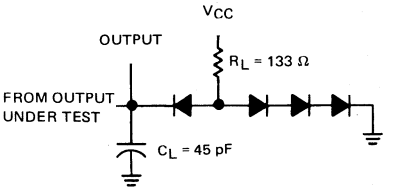
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with ground applied to all inputs except R which is at 4.5 V and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C	Y	C_L = 45 pF, R_L = 133 Ω, See Figure 1		14	22	ns
t_{PHL}					17	25	
t_{PLH}	C	∇			10	16	ns
t_{PHL}					8	13	

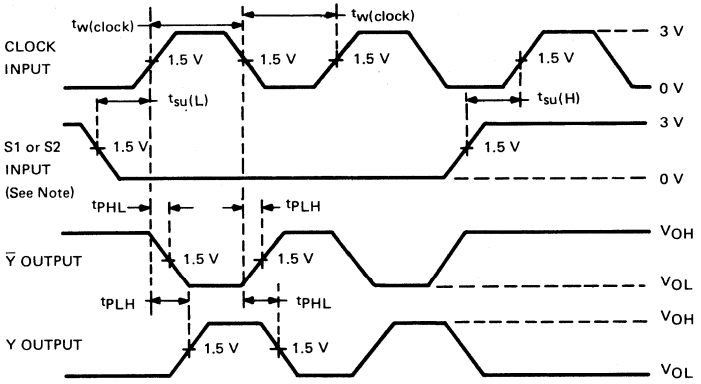
¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



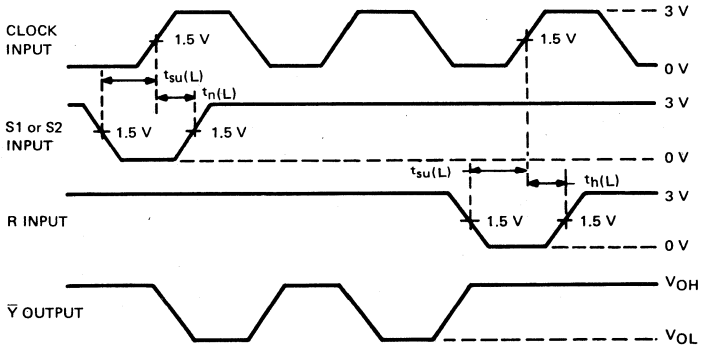
NOTES: A. The clock input pulse in figures 2 through 5 is supplied by a generator having the following characteristics: $t_{w(clock)} \geq 15$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–LOAD CIRCUIT FOR SWITCHING TESTS



NOTE: Mode control and R inputs are low unused S input is high.

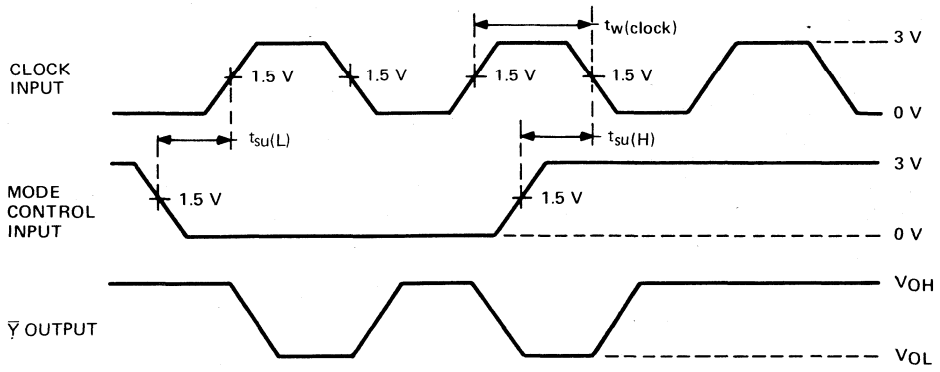
FIGURE 2–INITIATING AND TERMINATING PULSE TRAIN FROM S INPUTS



NOTE: Mode control input is low and unused S input is high.

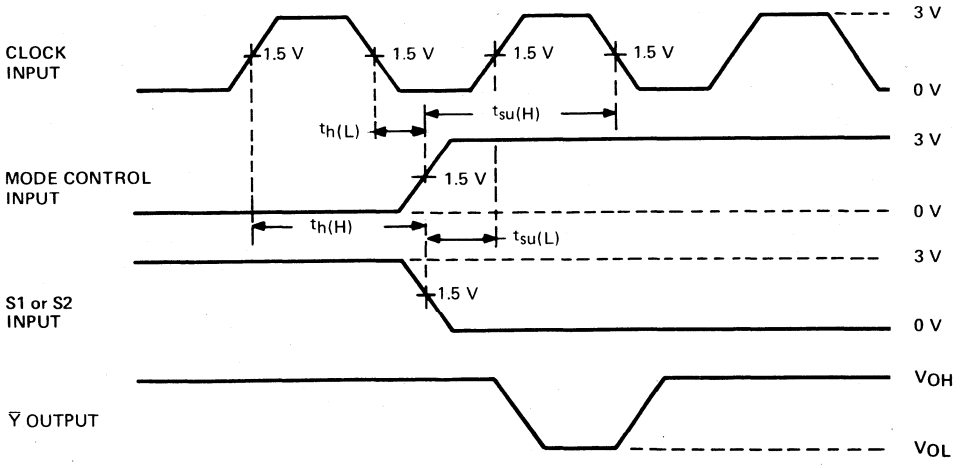
FIGURE 3–INITIATING PULSE TRAIN FROM S AND TERMINATING WITH R INPUTS

PARAMETER MEASUREMENT INFORMATION



NOTE: At least one of the S inputs is low.

FIGURE 4–INITIATING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT



NOTE: Input R is low and the unused S input is high.

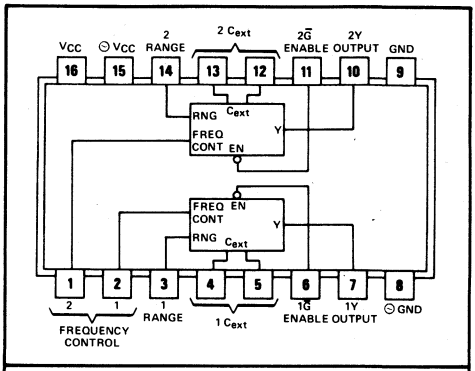
FIGURE 5–ENABLING SINGLE PULSE

TYPES SN54S124, SN74S124
DUAL VOLTAGE-CONTROLLED OSCILLATORS

BULLETIN NO. DL-S 12025, MARCH 1974—REVISED DECEMBER 1980

- Two Independent VCO's in a 16-Pin Package
- Output Frequency Set by Single External Component:
  - Crystal for High-Stability Fixed-Frequency Operation
  - Capacitor for Fixed- or Variable-Frequency Operation
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry
- Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges
- Typical f_{max} . . . . . 85 MHz
  Typical Power Dissipation . . . . . 525 mW
- Frequency Spectrum . . . 1 Hz to 60 MHz

SN54S124 . . . J OR W PACKAGE
SN74S124 . . . J OR N PACKAGE
(TOP VIEW)



logic: While the enable input is low, the output is enabled. While the enable input is high, the output is high.

description

The 'S124 features two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-sensitive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. Under the conditions used in Figure 3, the output frequency can be approximated as follows:

$$f_o = \frac{5 \times 10^{-4}}{C_{ext}}$$

where: f_o = output frequency in hertz

C_{ext} = external capacitance in farads.

These devices can operate from a single 5-volt supply. However, one set of supply-voltage and ground pins (V_{CC} and GND) is provided for the enable, synchronization-gating, and output sections, and a separate set (⊖V_{CC} and ⊖GND) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system.

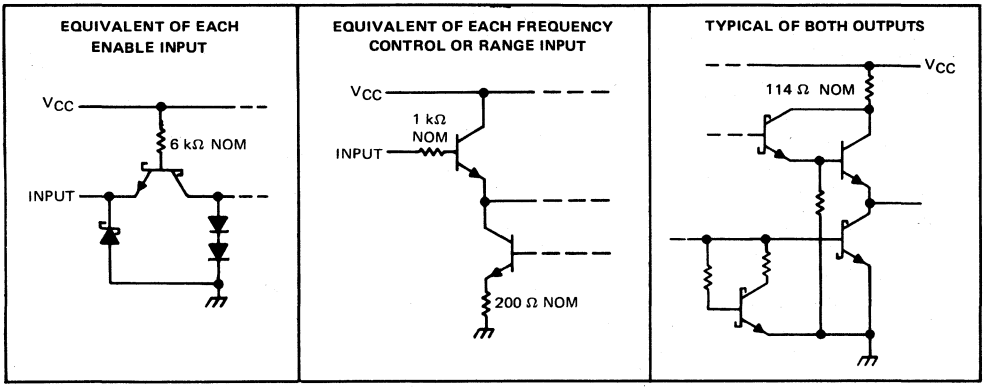
The enable input of these devices starts or stops the output pulses when it is low or high, respectively. The internal oscillator of the 'S124 is started and stopped by the enable input. The enable input is one standard load; it and the buffered output operate at standard Schottky-clamped TTL levels.

The pulse synchronization-gating section ensures that the first output pulse is neither clipped nor extended. Duty cycle of the square-wave output is fixed at approximately 50 percent.

The SN54S124 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S124 is characterized for operation from 0°C to 70°C.

2e 74LS629

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Notes 1 and 2)	7V
Input voltage	5.5 V
Operating free-air temperature range: SN54S124	−55°C to 125°C
SN74S124	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.
2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and $\ominus V_{CC}$ terminals, unless otherwise noted.

recommended operating conditions

	SN54S124			SN74S124			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$	1		5	1		5	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Output frequency (enabled), f_o	1			1			Hz
			60			60	MHz
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both pins 15 and 16.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage at enable				2			V
V_{IL}	Low-level input voltage at enable						0.8	V
V_{IK}	Input clamp voltage at enable		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
				SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current	Freq control or range	V_{CC} = MAX	V_I = 5 V		10	50	μA
				V_I = 1 V		1	15	
I_I	Input current at maximum input voltage	Enable	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Enable	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	Enable	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current, total into pins 15 and 16		V_{CC} = MAX, See Note 2			105	150	mA
			V_{CC} = MAX, T_A = 125°C, See Note 2	W package only			110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the outputs disabled and open.

switching characteristics, V_{CC} = 5 V, R_L = 280 Ω, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_o	Output frequency	C_{ext} = 2 pF	$V_{I(freq)}$ = 4 V, $V_{I(rng)}$ = 1 V	60	85		MHz
			$V_{I(freq)}$ = 1 V, $V_{I(rng)}$ = 5 V	25	40		
	Output duty cycle	C_{ext} = 8.3 pF to 500 μF			50%		
t_{PHL}	Propagation delay time, high-to-low-level output from enable	f_o = 1 Hz to 20 MHz			$\frac{1.4}{f_{o(Hz)}}$		s
		f_o > 20 MHz			70		ns

TYPICAL APPLICATION DATA

free-running oscillator

Free-running oscillators can be implemented for most systems by setting the output frequency of the VCO with either a capacitor or a crystal. If excitation is provided with a capacitor the frequency control and/or range inputs can be used to vary the output frequency.

When the 'S124 is excited with a crystal, low-frequency response ($\leqslant$ 1 MHz) can be improved if a relatively small capacitor (5 to 15 pF) is paralleled with the crystal. When operated at the fundamental frequency of a crystal, the frequency control input should be high ($\approx$ 5 V) and the range input should be low (grounded) for maximum stability over temperature and supply voltage variations.

phase-locked loops

A basic crystal-controlled phase-locked loop is illustrated in Figure 1. This application can be used for implementation of:

a. A highly stable fixed-frequency clock generator.
b. A highly stable fixed- or variable-frequency synthesizer.
c. A highly efficient "slave-clock" system for synchronizing off-card, remote, or data-interfacing clock systems

With fixed division rates for both M and N, the output frequency (f_o) will be stable at $f_o = \frac{N}{M} f_1$. Obviously, either M or N, or both, could be programmable counters in which case the output frequency (f_o) will be a variable frequency dependent on the instantaneous value of $\frac{N}{M} f_1$.

The crystal-controlled VCO can be operated up to 60 MHz with an accuracy that is dependent on the crystal. At the higher frequencies, response of the phase comparator can become a limiting factor and one of the following approaches may be necessary to extend the operating frequency range.

a. Frequencies $\frac{f_1}{M}$ and $\frac{f}{N}$ can be divided equally by the same constant (K) also shown in Figure 1. The constant can be any value greater than unity ($K > 1$), and should be selected to yield frequency ranges that can be handled adequately by the phase-comparator and filter. The output frequency (f_o) retains the same relationship as previously explained because now:

$$f_o = \frac{KN}{KM} f_1 = \frac{N}{M} f_1$$

b. In another method, the comparison of $\frac{f_1}{M}$ and $\frac{f}{N}$ can be performed with either an SN54LS85/SN74LS85 or SN54S85/SN74S85. The resultant $A > B$ and $A < B$ outputs from the 'LS85 or 'S85 permit the detector to be simplified to a charge-pump circuit. See Figure 2.

TYPICAL APPLICATION DATA

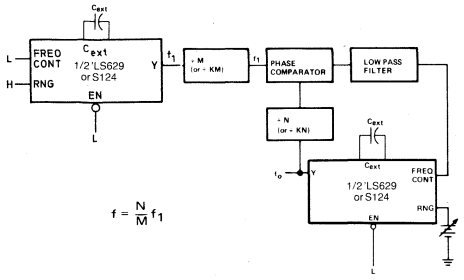


FIGURE 1–PHASE-LOCKED LOOP

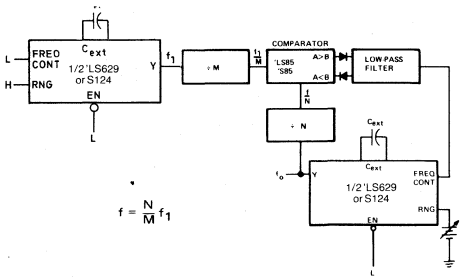


FIGURE 2–HIGH-FREQUENCY PHASE-LOCKED LOOP

TYPICAL CHARACTERISTICS ('S124 only)

BASE OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

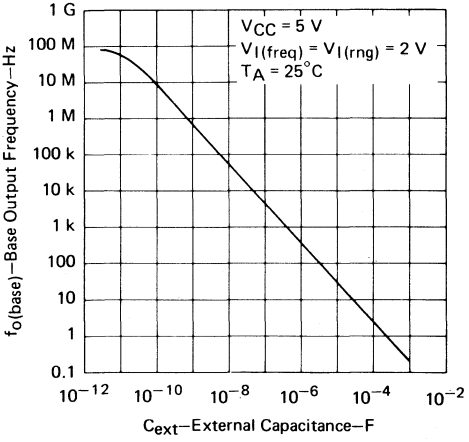


FIGURE 3

NORMALIZED OUTPUT FREQUENCY
vs
INPUT VOLTAGE

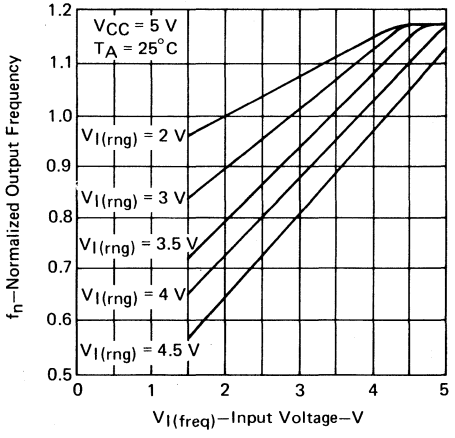


FIGURE 4

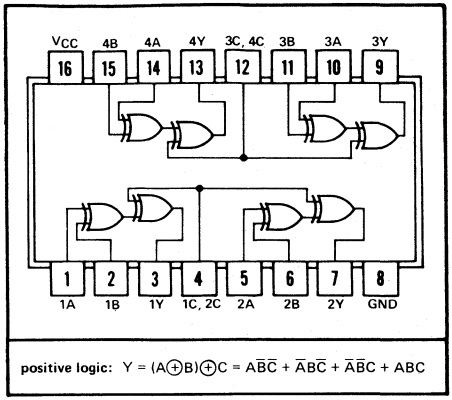
NOTE: $f_o = f_n \times f_{o(base)}$.

TYPES SN54S135, SN74S135
QUADRUPLE EXCLUSIVE-OR/NOR GATES

BULLETIN NO. DL-S 7211826, DECEMBER 1972

- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times . . . 8 ns Typical
- Can Operate as Exclusive-OR Gate (C Input Low) or as Exclusive-NOR Gate (C Input High)

SN54S135 . . . J OR W PACKAGE
SN74S135 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = (A \oplus B) \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

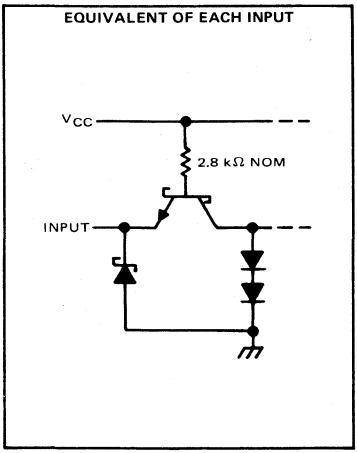
FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

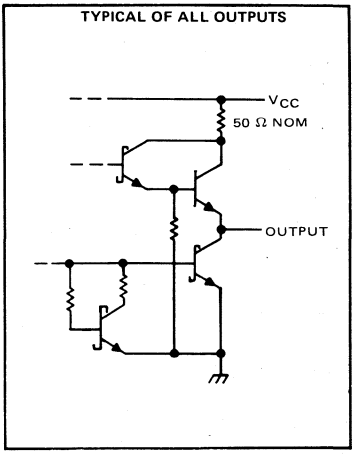
H = high level, L = low level

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S135 . . . . . −55°C to 125°C
SN74S135 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S135			SN74S135			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			65	99	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

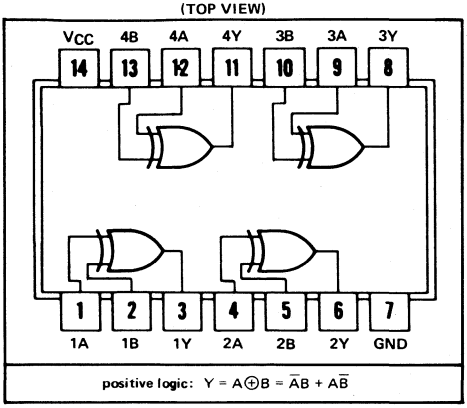
PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A = L, C = L	C_L = 15 pF, R_L = 280 Ω, See Note 3		8.5	13	ns
t_{PHL}					11	15	
t_{PLH}	A or B	B or A = H, C = L			8	12	ns
t_{PHL}					9	13.5	
t_{PLH}	A or B	B or A = L, C = H			10	15	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	B or A = H, C = H			8.5	12	ns
t_{PHL}					7	11	
t_{PLH}	C	A = B			8	12	ns
t_{PHL}					9.5	14.5	
t_{PLH}	C	A ≠ B			7.5	11.5	ns
t_{PHL}					8	12	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54136, SN54LS136, SN74136, SN74LS136
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES
WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7611827, DECEMBER 1972—REVISED OCTOBER 1976

SN54136, SN54LS136 . . . J OR W PACKAGE
SN74136, SN74LS136 . . . J OR N PACKAGE
(TOP VIEW)



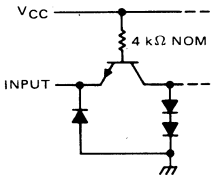
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

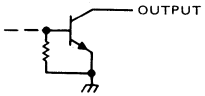
H = high level, L = low level

schematics of inputs and outputs

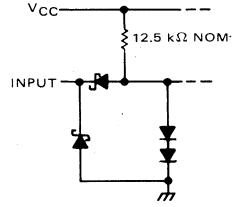
EQUIVALENT OF EACH INPUT
OF '136



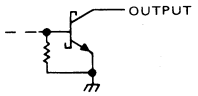
TYPICAL OF ALL OUTPUTS
OF '136



EQUIVALENT OF EACH INPUT
OF 'LS136



TYPICAL OF ALL OUTPUTS
OF 'LS136



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54136 . . . . . −55°C to 125°C
SN74136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54136			SN74136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −8 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current, high-level output	V_{CC} = MAX, See Note 2		SN54136		30	43	mA
				SN74136		30	50	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 400 Ω, See Note 3		12	18	ns
t_{PHL}					39	50	
t_{PLH}	A or B	Other input high			14	22	ns
t_{PHL}					42	55	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS136 . . . . . −55°C to 125°C
SN74LS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS136			SN74LS136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS136			SN74LS136			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 4		18	30	ns
t_{PHL}					18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

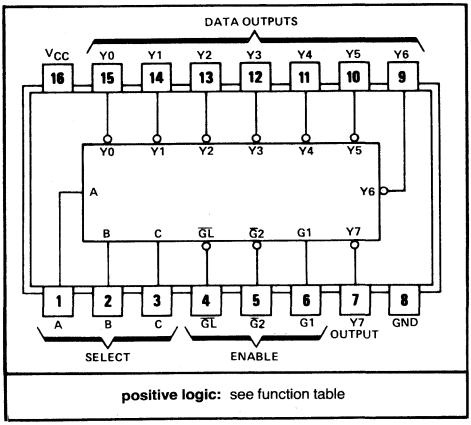
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS137, SN74LS137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2416, JUNE 1978

- Combines Decoder and 3-Bit Address Latch
- Incorporates 3 Enable Inputs to Simplify Cascading
- Low Power Dissipation . . . 65 mW Typ

SN54LS137 . . . J OR W PACKAGE
SN74LS137 . . . J OR N PACKAGE
(TOP VIEW)

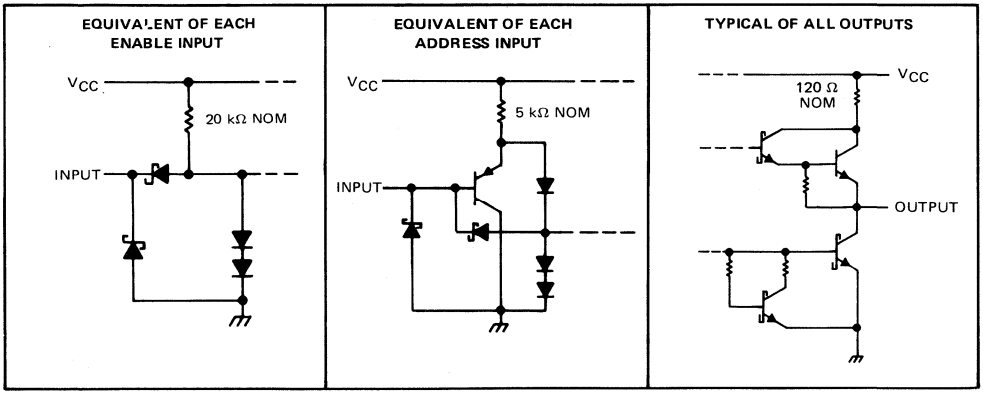


positive logic: see function table

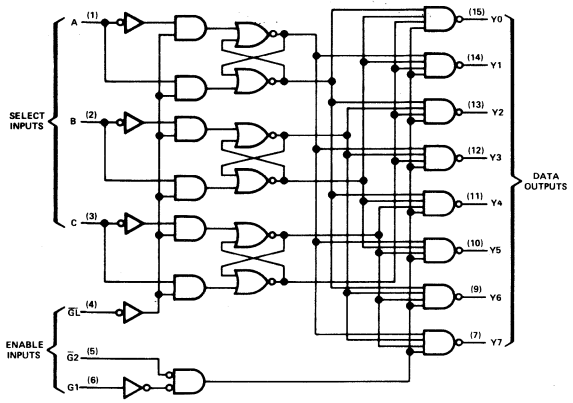
description

The 'LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'LS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The 'LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

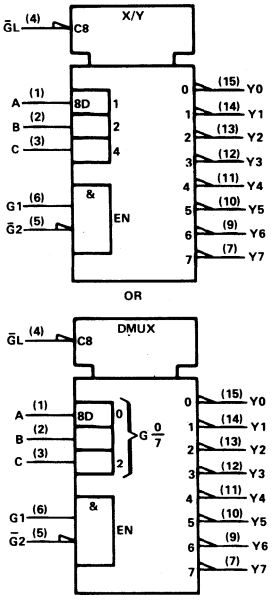
schematics of inputs and outputs



functional block diagram (positive logic)



logic symbol



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS137 . . . . . −55°C to 125°C
SN74LS137 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS137			SN74LS137			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse at $\overline{G1}$, t_w	15			15			ns
Setup time at A, B, and C inputs, t_{su}	10			10			ns
Hold time at A, B, and C inputs, t_h	10			10			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS137			SN74LS137			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Enable			−0.4			−0.4	mA
			A, B, C			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			11	18		11	18	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, C	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 3		11	17	ns
t_{PHL}			4			25	38	
t_{PLH}	A, B, C	Y	3			16	24	ns
t_{PHL}			3			19	29	
t_{PLH}	Enable $\overline{G2}$	Y	2			13	21	ns
t_{PHL}			2			16	27	
t_{PLH}	Enable G1	Y	3			14	21	ns
t_{PHL}			3			18	27	
t_{PLH}	Enable $\overline{G1}$	Y	3			18	27	ns
t_{PHL}			4			25	38	

◇t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 3: For load circuit and voltage waveforms, see page 3-11

TYPICAL APPLICATION DATA

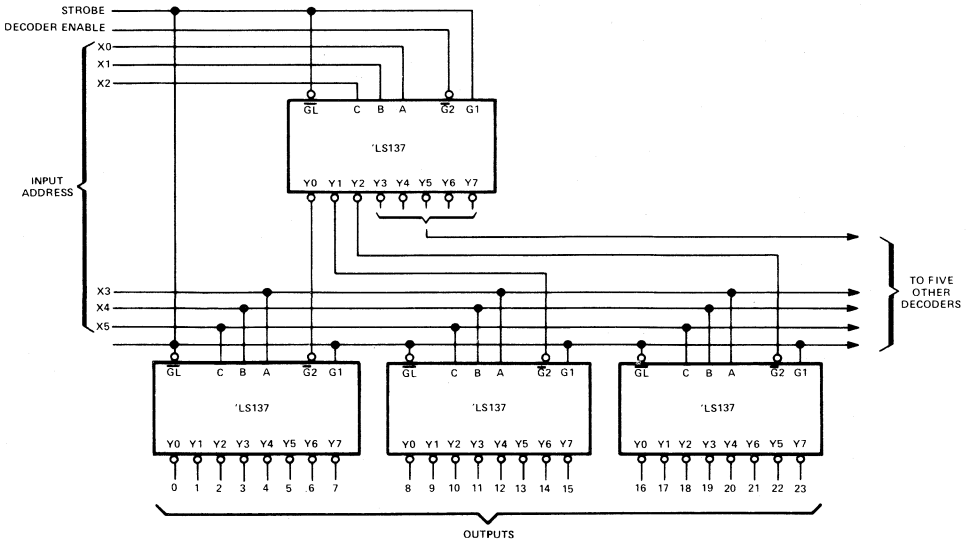


FIGURE 1–6-LINE TO 64-LINE DECODER WITH INPUT ADDRESS STORAGE

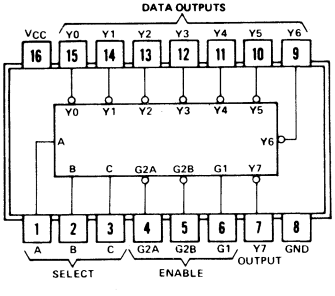
7

TYPES SN54LS138, SN54LS139A, SN54S138, SN54S139, SN74LS138, SN74LS139A, SN74S138, SN74S139 DECODERS /MULTIPLEXERS

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139A Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Clamped for High Performance

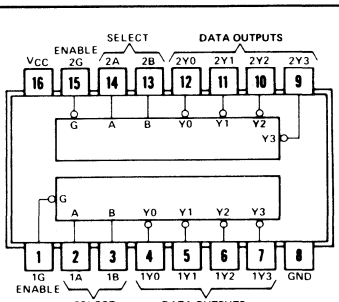
TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139A	22 ns	34 mW
'S139	7.5 ns	300 mW

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS139A, SN54S139 . . . J OR W PACKAGE
SN74LS139A, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

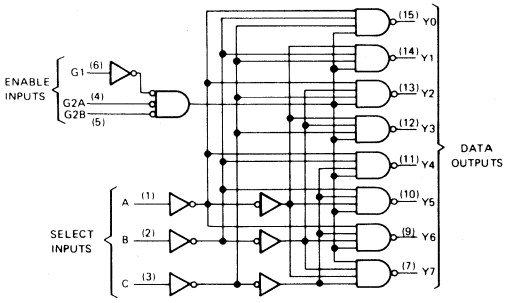
The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139A and 'S139 comprise two individual two-line-to-four-line-decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74SL load ('LS138, 'LS139A) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operatio over the full military temperature range of −55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.

functional block diagrams and logic

'LS138, 'S138



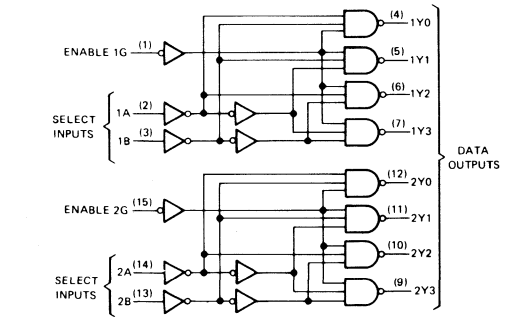
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139A, 'S139



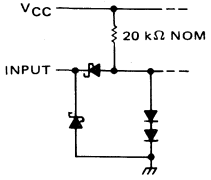
'LS139A, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

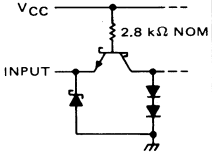
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

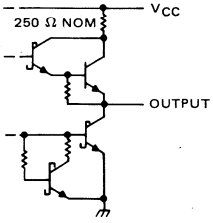
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139A



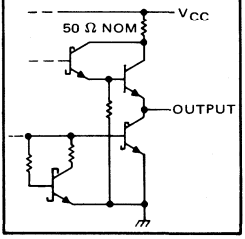
EQUIVALENT OF EACH INPUT OF 'S138, 'S139



TYPICAL OF OUTPUTS OF 'LS138, 'LS139A



TYPICAL OF OUTPUTS OF 'S138, 'S139



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS138, SN54LS139A Circuits . . . . . −55°C to 125°C
SN74LS138, SN74LS139A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS138 SN54LS139A			SN74LS138 SN74LS139A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS138 SN54LS139A			SN74LS138 SN74LS139A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS} Short circuit output current §	V_{CC} = MAX	'LS138	−20		−100	−20		−100	mA
		'LS139A	−20		−100	−20		−100	
I_{OS} Supply current	V_{CC} = MAX, Outputs enabled and open	'LS138		6.3	10		6.3	10	mA
		'LS139A		6.8	11		6.8	11	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS138 SN74LS138			SN54LS139A SN74LS139A			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	C_L = 15 pF, R_L = 2 kΩ, See Note 2		13	20		13	20	ns
t_{PHL}						27	41		22	33	ns
t_{PLH}			3			18	27		18	29	ns
t_{PHL}						26	39		25	38	ns
t_{PLH}	Enable	Any	2			12	18		16	24	ns
t_{PHL}						21	32		21	32	ns
t_{PLH}			3			17	26				ns
t_{PHL}						25	38				ns

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuits and waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S138, SN54S139 Circuits . . . . . −55°C to 125°C
SN74S138, SN74S139 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S138 SN54S139			SN74S138 SN74S139			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S138 SN54S138			SN54S139 SN74S139			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		2.5	3.4		V
			SN74S'	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs enabled and open			49	74		60	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S138, SN74S138			SN54S139 SN74S139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary select	Any	2	C_L = 15 pF, R_L = 280 Ω, See Note 3		4.5	7		5	7.5	ns
t_{PHL}						7	10.5		6.5	10	
t_{PLH}			3			7.5	12		7	12	ns
t_{PHL}						8	12		8	12	
t_{PLH}	Enable	Any	2			5	8		5	8	ns
t_{PHL}						7	11		6.5	10	
t_{PLH}			3			7	11				ns
t_{PHL}						7	11				

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 3: Load circuits and waveforms are shown on page 3-10.

TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

BULLETIN NO. DL-S 7211801, DECEMBER 1972

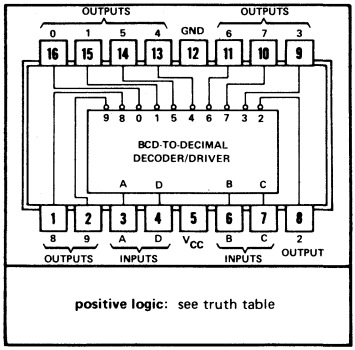
- Drives gas-filled cold-cathode indicator tubes directly
- Fully decoded inputs ensure all outputs are off for invalid codes
- Input clamping diodes minimize transmission-line effects

FUNCTION TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

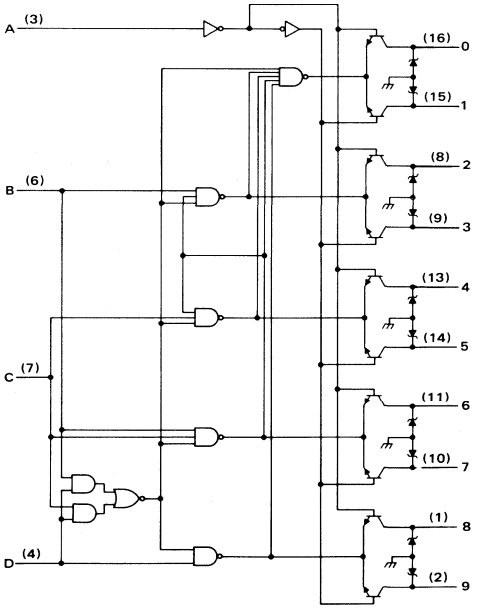
H = high level, L = low level
†All other outputs are off

J OR N PACKAGE
(TOP VIEW)



positive logic: see truth table

functional block diagram



description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 80 milliwatts. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current into any output (off-state) . . . . . 2 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage			60	V
Operating free-air temperature, T_A	0		70	°C

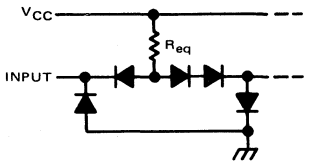
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −5 mA				−1.5	V
$V_{O(on)}$	On-state output voltage		V_{CC} = MIN, I_O = 7 mA				2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9		V_{CC} = MAX, I_O = 0.5 mA		60			V
$I_{O(off)}$	Off-state reverse current		V_{CC} = MAX, V_O = 55 V				50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15		V_{CC} = MAX, V_O = 30 V	T_A = 55°C			5	μA
				T_A = 70°C			15	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A input	V_{CC} = MAX, V_I = 2.4 V				40	μA
		B, C, or D input					80	
I_{IL}	Low-level input current	A input	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		B, C, or D input					−3.2	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			16	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

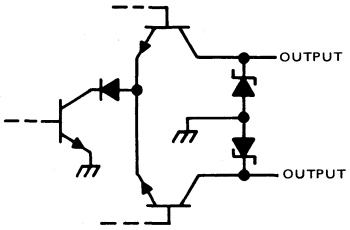
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Input A: R_{eq} = 6 kΩ NOM
Inputs B, C, D: R_{eq} = 2 kΩ NOM

TYPICAL OF ALL OUTPUTS



TYPE SN74142
BCD COUNTER/4-BIT LATCH/BCD DECODER/DRIVER

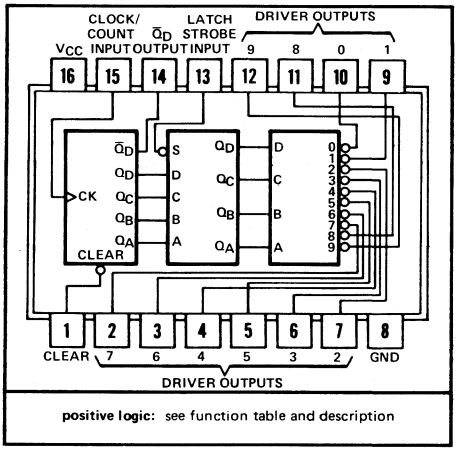
BULLETIN NO. DL-S 7211719, MAY 1972—REVISED DECEMBER 1972

FUNCTION TABLE

INPUTS			OUTPUTS	
COUNT PULSE (CLOCK)	CLEAR	LATCH STROBE	ON†	$\overline{Q}_D$
X	L	L	0	H
1	H	L	1	H
2	H	L	2	H
3	H	L	3	H
4	H	L	4	H
5	H	L	5	H
6	H	L	6	H
7	H	L	7	H
8	H	L	8	L
9	H	L	9	L
10	H	L	0	H
11	H	H	0	H

†All other outputs are off.
H = high level, L = low level, X = irrelevant

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table and description

description

The SN74142 contains a divide-by-ten (BCD) counter, a four-bit latch, and a decoder/*Nixie*‡ tube driver on a monolithic chip and is packaged in popular 16-pin packages. This single MSI function can replace the equivalent of three separately packaged MSI circuits to reduce printed-circuit board area and the number of system interconnections, resulting in reduced costs and improved reliability.

Four master-slave flip-flops are fully decoded to provide a divide-by-ten counter. A direct clear input will, when taken low, reset and hold the counter at zero (all Q outputs low, $\overline{Q}_D$ output high). While the clear input is inactive (high), each positive-going transition of the clock will increment the counter. The $\overline{Q}_D$ output is made available externally for cascading to n-bit counters.

The Q outputs of the counter are routed to the data inputs of the four-bit latch. While the latch strobe input is low, the internal latch outputs will follow the respective Q outputs of the counter. When the latch strobe input is taken high, the latch stores the data which has been setup by the counter outputs prior to the low-to-high level transition of the latch strobe input. The $\overline{Q}_D$ output from the counter is not stored by the latch since it is intended for clocking the next counter stage. This means that the system counter can continuously acquire new data. Since all outputs of the latch and Q outputs of the counter drive low-capacitance on-chip loads, the circuitry is considerably simplified with respect to the number of components required. This results in a highly efficient function which typically reduces power requirements 15% when compared to systems using the three separate packages.

The SN74142 counter/latch/driver features fully buffered inputs to reduce drive requirements to one normalized Series 74 load per input, and diode-clamping of all inputs to minimize transmission line effects. The counter will accept input clock frequencies up to 20 MHz and is entirely compatible for use with all popular TTL and DTL logic circuits. The high-performance n-p-n driver outputs are identical to the SN74141 and have a maximum off-state reverse current of 50 microamperes at 55 volts.

‡*Nixie* is a registered trademark of the Burroughs Corporation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state current into outputs 0 thru 9 . . . . . 1 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current from $\overline{Q}_D$, I_{OH}				−400	μA
Low-level output current from $\overline{Q}_D$, I_{OL}				8	mA
Input clock frequency, f_{clock}		0		20	MHz
Clock pulse width, $t_{w(clock)}$ (see Figure 1)	High logic level	15			ns
	Low logic level	35			
Clear pulse width, $t_{w(clear)}$ (see Figure 1)		25			ns
Strobe pulse width, $t_{w(strobe)}$ (see Figure 1)		20			ns
Clear inactive-state setup time, t_{su} (see Figure 1)		25			ns
Strobe time, t_{strobe} (see Figure 1)		45		$t_{w(clock)}$ +10	ns
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

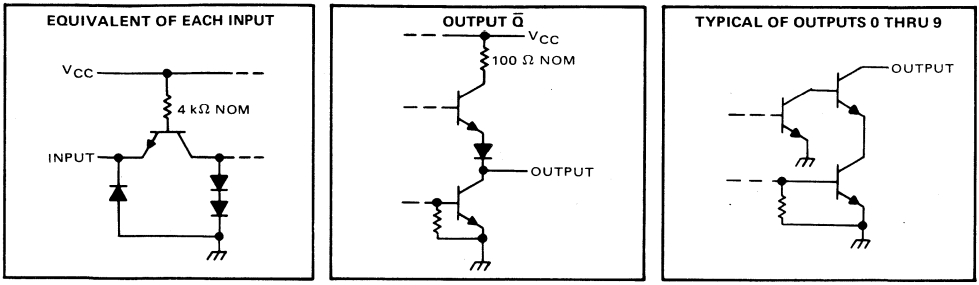
PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OL} = 8 mA		0.2	0.4	V
$V_{O(on)}$	On-state voltage, outputs 0 thru 9	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state voltage, outputs 0 thru 9	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state current, outputs 0 thru 9	V_{CC} = MAX, V_O = 55 V			50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit $\overline{Q}_D$ output current	V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open		68	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

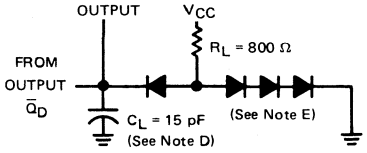
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clock	C_L = 15 pF, R_L = 800 Ω, See Figure 1		35	55	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}_D$ output from clock			30	45	
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clear			30	45	ns

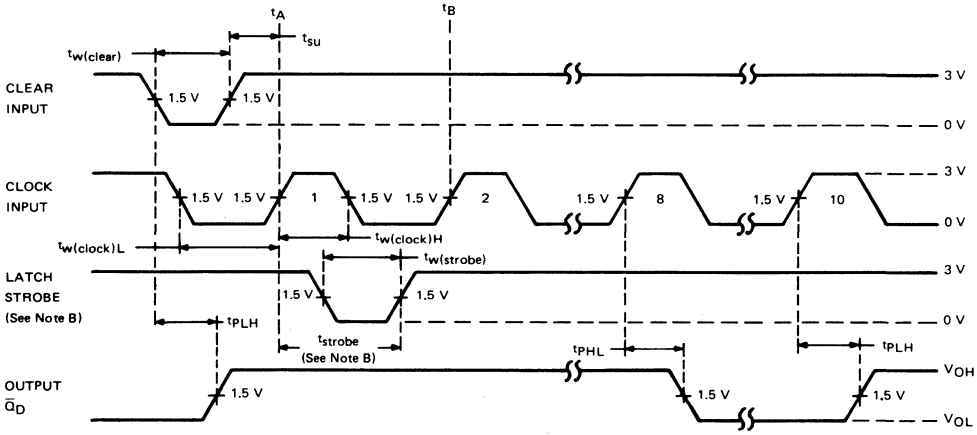
schematics of inputs and outputs



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. This typical abbreviated sequence illustrates clearing from count 8 or 9 and counting through ten clock pulses. Clock pulses 3 through 7 and 9 are omitted for brevity.

B. Strobe input can go low at any time; however, the positive transition to store data from any given clock transition (t_A) must occur a minimum of 45 ns after t_A and prior to 10 ns after the next positive-going clock transition (t_B + 10 ns).

C. Input pulses are supplied by generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.

D. C_L includes probe and jig capacitance.

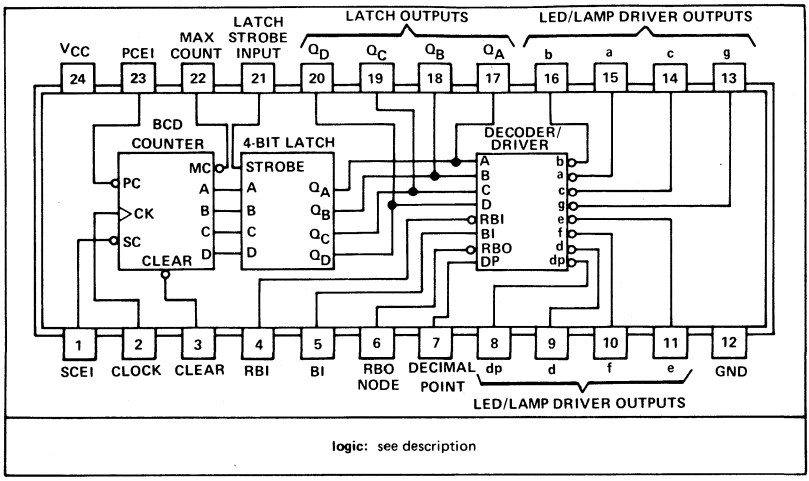
E. All diodes are 1N3064.

FIGURE 1

TYPES SN54143, SN54144, SN74143, SN74144
4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

BULLETIN NO. DL-S 7211538, NOVEMBER 1971—REVISED DECEMBER 1972

SN54143, SN54144 . . . J OR W PACKAGE
SN74143, SN74144 . . . J, N OR NT PACKAGE
(TOP VIEW)



logic: see description

- **Choice of Driver Outputs:**

  SN54143 and SN74143 have 15-mA Constant-Current Outputs for Driving Common-Anode LED's such as TIL302 or TIL303 without Series Resistors

  SN54144 and SN74144 Drive High-Current Lamps, Numitrons†, or LED's from Saturated Open-Collector Outputs

- **Universal Logic Capabilities**

  Ripple Blanking of Extraneous Zeros
  Latch Outputs Can Drive Logic Processors Simultaneously
  Decimal Point Driver Is Included

- **Synchronous BCD Counter Capability Includes:**

  Cascadable to N-Bits
  Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display
  Direct Clear Input

description

These TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard series 54/74 load. The logic outputs, except RBO, have active pull-ups.

The SN54143 and SN74143 driver outputs are designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from outputs "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

†Trademark of RCA

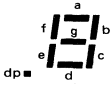
description (continued)

The SN54144 and SN74144 drivers have high-sink-current saturated outputs for driving indicators having voltage ratings up to 15 volts or requiring up to 25 milliamperes drive. The SN54144 sinks 20 milliamperes and the SN74144 sinks 25 milliamperes at an on-level voltage of 0.6 volts across their respective operating temperature ranges.

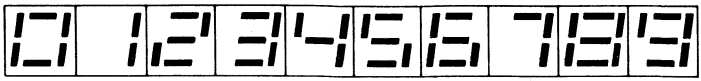
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN54143 and SN54144 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74143 and SN74144 are characterized for operation from 0°C to 70°C.

Functions of the inputs and outputs of these devices are as follows:

FUNCTION	PIN NO.	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	5	When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches in BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.



SEGMENT IDENTIFICATION

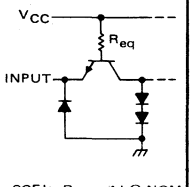


NUMERICAL DESIGNATIONS–RESULTANT DISPLAYS

schematics of inputs and outputs

'143, '144

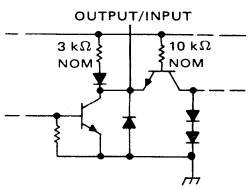
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



SCEI: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 8 kΩ NOM

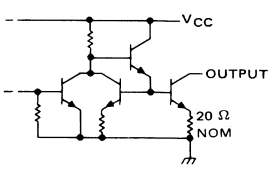
'143, '144

EQUIVALENT OF BI/RBO



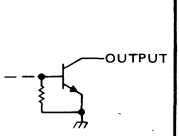
'143

TYPICAL OF ALL OUTPUTS EXCEPT BI/RBO



'144

TYPICAL OF ALL OUTPUTS EXCEPT BI/RBO



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state voltage at outputs "a" thru "g" and "dp", '144 . . . . . 15 V
Off-state current at outputs "a" thru "g" and "dp", '143 . . . . . 250 μA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 2) . . . . . 1.4 W
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the SN54143 and SN54144 in the N and W packages, this rating applies at (or below) 80°C free-air temperature. For operation above this temperature, derate linearly at the rate of 11.7 mW/°C for the W package and 14.7 mW/°C for the N package. No derating is required for these devices in the J package.

recommended operating conditions

		SN54143, SN54144			SN74143, SN74144			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
On-state voltage at outputs a thru g and dp ('143 only)		1		5	1		5	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			−240			−240	μA
	Maximum count			−560			−560	
	RBO			−120			−120	
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D, RBO			4.8			4.8	mA
	Maximum count			11.2			11.2	
Clock pulse width, $t_{w(clock)}$	High logic level	25			25			ns
	Low logic level	55			55			
Clear pulse width, $t_{w(clear)}$		25			25			ns
Setup time, t_{su}	Serial and parallel carry	30↑			30↑			ns
	Clear inactive state	60↑			60↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54143, SN74143			SN54144, SN74144			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4			2.4			V
		Q_A, Q_B, Q_C, Q_D								
		Maximum count								
V_{OL}	Low-level output voltage	Q_A, Q_B, Q_C, Q_D, RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.4			0.4	V
		Maximum count								
$V_{O(off)}$	Off-state output voltage	Outputs a thru g, dp	V_{CC} = MAX, I_{OH} = 250 μA	7			15			V
$V_{O(on)}$	On-State output voltage	Outputs a thru g, dp	V_{CC} = MIN, See Note 3						0.6	V
$I_{O(on)}$	On-state output current	Outputs a thru g	V_{CC} = MIN, V_O = 1 V	9	15					mA
			V_{CC} = 5 V, V_O = 2 V		15					
			V_{CC} = MAX, V_O = 5 V		15	22				
		Output dp	V_{CC} = MIN, V_O = 1 V	4.5	7					
			V_{CC} = 5 V, V_O = 2 V		7					
			V_{CC} = MAX, V_O = 5 V		7	12				
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Serial carry	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		RBO node		−0.12	−0.5		−0.12	−0.5		mA
		Other inputs				20			20	μA
I_{IL}	Low-level input current	Serial carry	V_{CC} = MAX, V_I = 0.4 V, See Note 4			−1.6			−1.6	mA
		RBO node			−1.5	−2.4		−1.5	−2.4	
		Other inputs				−0.8			−0.8	
I_{OS}	Short-circuit output current	Q_A, Q_B, Q_C, Q_D	V_{CC} = MAX	−9		−27.5	−9		−27.5	mA
		Maximum count		−15		−55	−15		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		56	93		56	93	mA

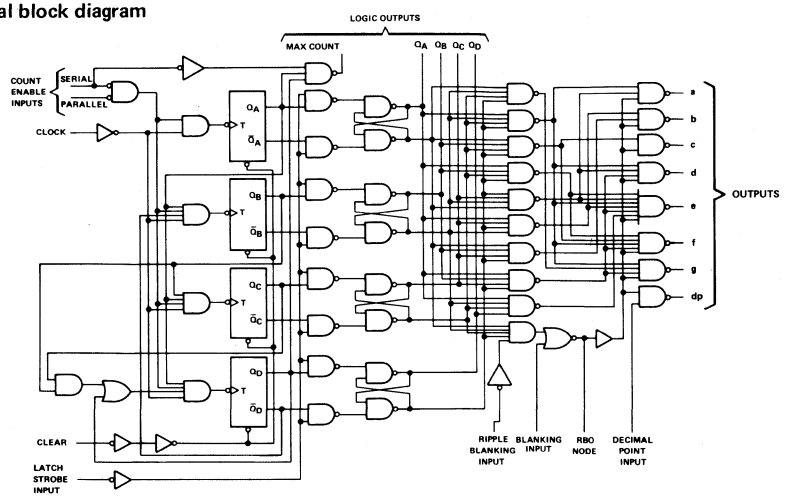
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 3. For SN54144, I_{OL} = 20 mA; for SN74144, I_{OL} = 25 mA.
4. I_{IL} at RBO node is tested with BI grounded and RBI at 4.5 V.
5. I_{CC} is measured after the following conditions are established:
a) Strobe = RBI = DP = 4.5 V
b) Parallel count enable = serial count enable = BI = GND
c) Clear (⊓) then clock until all outputs are on (⊔)
d) For '143, outputs "a" through "g" and "dp" = 2.5 V, all other outputs open. For '144, all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				12	18		MHz
t_{PLH}	Serial look-ahead	Maximum count	C_L = 15 pF, R_L = 560 Ω, See Note 6		12	20	ns
t_{PHL}					23	35	
t_{PLH}	Clock	Maximum count			26	40	ns
t_{PHL}					29	45	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D	C_L = 15 pF, R_L = 1.2 kΩ, See Note 6		28	45	ns
t_{PHL}					38	60	
t_{PHL}	Clear	Q_A, Q_B, Q_C, Q_D			57	90	ns

§f_{max} ≡ Maximum clock frequency, t_{PLH} ≡ Propagation delay time, low-to-high-level output, t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 6: Load circuit and voltage waveforms are shown on page 3-10.

functional block diagram

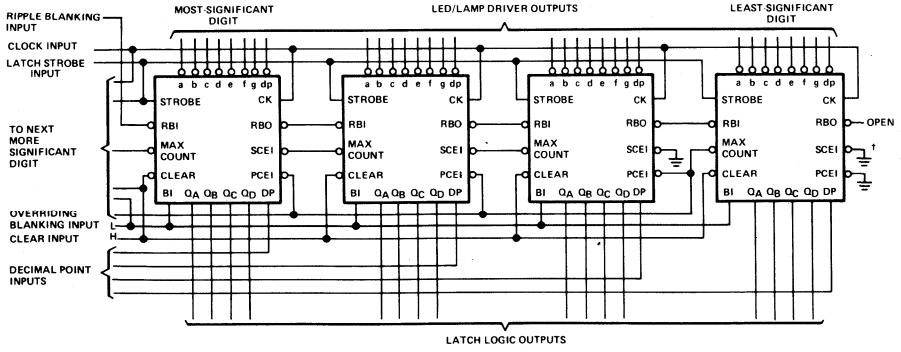


... Dynamic input activated by a transition from a high level to a low level.

TYPICAL APPLICATION DATA

This application demonstrates how the drivers may be cascaded for N-bit display applications. It features:

- Synchronous, look-ahead counting
- Ripple blanking of leading zeros; blanking of trailing zeros (not illustrated) can also be implemented
- Overriding blanking for total suppression or intensity modulation of display
- Direct parallel clear
- Latch strobe permits counter to acquire next display while viewing current display



†The serial count-enable input of the least-significant digit is normally grounded; however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

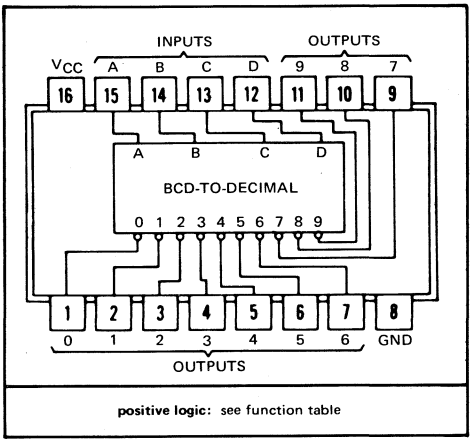
TYPES SN54145, SN54LS145, SN74145, SN74LS145
BCD-TO-DECIMAL DECODERS/DRIVERS

BULLETIN NO. DL-S 7611815, MARCH 1974—REVISED OCTOBER 1976

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145 . . . 35 mW Typical

SN54145, SN54LS145 . . . J OR W PACKAGE
SN74145, SN74LS145 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

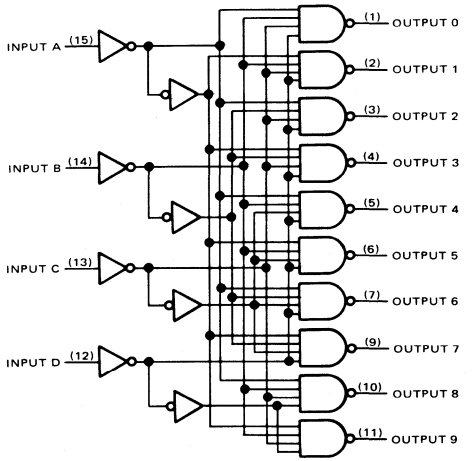
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monilithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN54145 . . . . . −55°C to 125°C
SN74145 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54145			SN74145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = 15 V				250	μA
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54145		43	62	mA
			SN74145		43	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

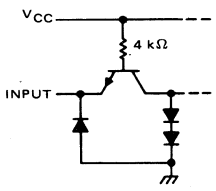
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			50	ns

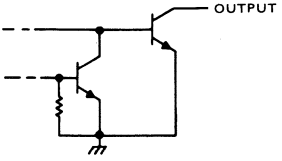
NOTE 3: Load circuit and waveforms are shown on page 3-10.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS145 . . . . . −55°C to 125°C
SN74LS145 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS145			SN74LS145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS145			SN74LS145			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 15 V			250			250	μA
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		V_{IL} = V_{IL} max	I_{OL} = 80 mA					2.3	3	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

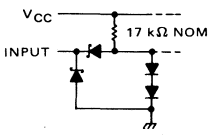
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF,	R_L = 665 Ω, See Note 4		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

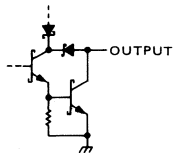
NOTE 4: Load circuit and waveforms are shown on page 3-11.

schematic of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



TYPES SN54147, SN54148, SN54LS147, SN54LS148, SN74147, SN74148 (TIM9907), SN74LS147, SN74LS148
10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

BULLETIN NO. DL-S 7611727, OCTOBER 1976

'147, 'LS147

- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:

  Keyboard Encoding
  Range Selection

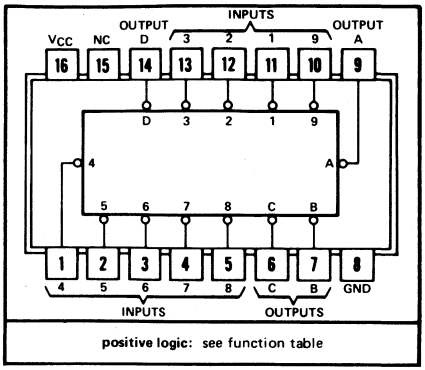
'148, 'LS148

- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:

  N-Bit Encoding
  Code Converters and Generators

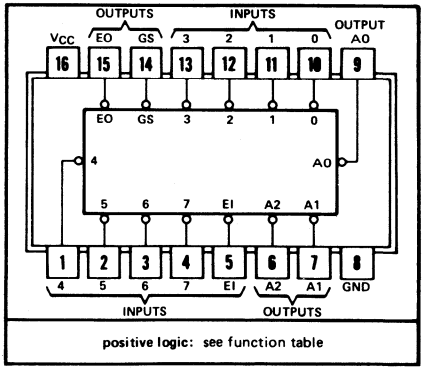
TYPE	TYPICAL DATA DELAY	TYPICAL POWER DISSIPATION
'147	10 ns	225 mW
'148	10 ns	190 mW
'LS147	15 ns	60 mW
'LS148	15 ns	60 mW

SN54147, SN54LS147 . . . J OR W PACKAGE
SN74147, SN74LS147 . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

SN54148, SN54LS148 . . . J OR W PACKAGE
SN74148, SN74LS148 . . . J OR N PACKAGE
(TOP VIEW)



description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The '147 and 'LS147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. The '148 and 'LS148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 54/74 or 54LS/74LS load, respectively.

'147, 'LS147
FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

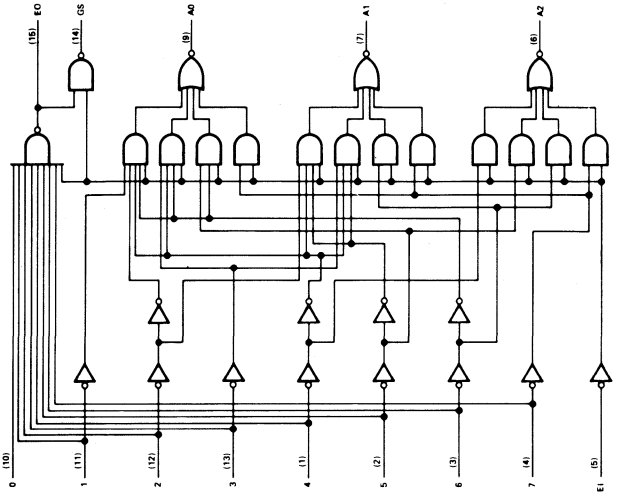
H = high logic level, L = low logic level, X = irrelevant

'148, 'LS148
FUNCTION TABLE

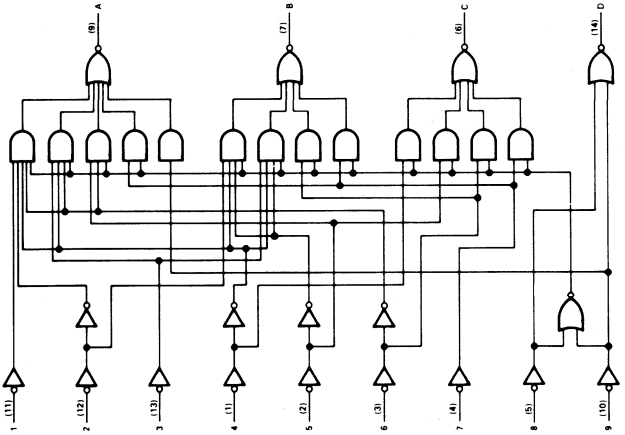
INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

functional block diagrams

'148, 'LS148

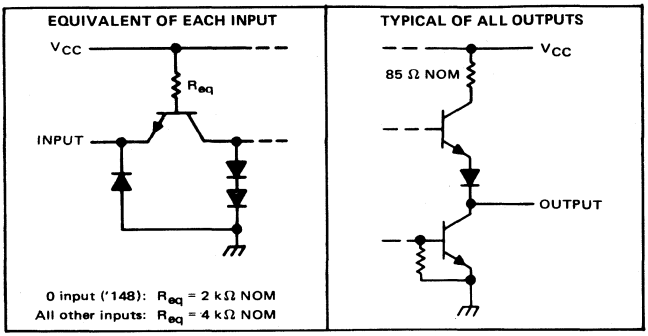


'147, 'LS147

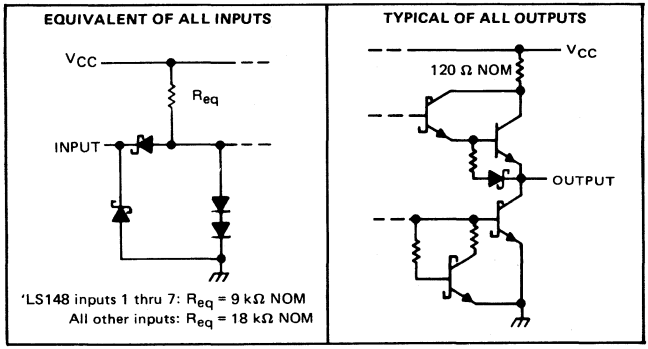


schematics of inputs and outputs

'147, '148



'LS147, 'LS148



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '147, '148 . . . . . 5.5 V
'LS147, 'LS148 . . . . . 7 V
Interemitter voltage: '148 only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54LS Circuits . . . . . −55°C to 125°C
SN74', SN74LS Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For '148 circuits, this rating applies between any two of the eight data lines, 0 through 7.

recommended operating conditions

	SN54'			SN74'			SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800			−400			−400	μA
Low-level output current, I_{OL}			16			16			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'147 MIN	'147 TYP‡	'147 MAX	'148 MIN	'148 TYP‡	'148 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	0 input	V_{CC} = MAX, V_I = 2.4 V							40	μA
		Any input except 0					40			80	
I_{IL}	Low-level input current	0 input	V_{CC} = MAX, V_I = 0.4 V							−1.6	mA
		Any input except 0					−1.6			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−35		−85	−35		−85	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition 1		50	70		40	60	mA
				Condition 2		42	62		35	55	mA

NOTE 3: For '147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For '148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		9	14	ns
t_{PHL}						7	11	
t_{PLH}	Any	Any	Out-of-phase output			13	19	ns
t_{PHL}						12	19	

SN54148, SN74148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		10	15	ns
t_{PHL}						9	14	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			13	19	ns
t_{PHL}						12	19	
t_{PLH}	0 thru 7	EO	Out-of-phase output			6	10	ns
t_{PHL}						14	25	
t_{PLH}	0 thru 7	GS	In-phase output			18	30	ns
t_{PHL}						14	25	
t_{PLH}	EI	A0, A1, or A2	In-phase output			10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	In-phase output			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	In-phase output			10	15	ns
t_{PHL}						17	30	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuits and waveforms are shown on page 3-10.

REVISED DECEMBER 1980

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	'LS148 inputs 1 thru 7	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		All other inputs					0.1			0.1	
I_{IH}	High-level input current	'LS148 inputs 1 thru 7	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		All other inputs					20			20	
I_{IL}	Low-level input current	'LS148 inputs 1 thru 7	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		All other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 5	Condition 1		12	20		12	20	mA
				Condition 2		10	17		10	17	mA

NOTE 5: For 'LS147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For 'LS148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open, I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

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SN54LS147, SN74LS147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	C_L = 15 pF, R_L = 2 kΩ, See Note 4		12	18	ns
t_{PHL}						12	18	
t_{PLH}	Any	Any	Out-of-phase output			21	33	ns
t_{PHL}						15	23	

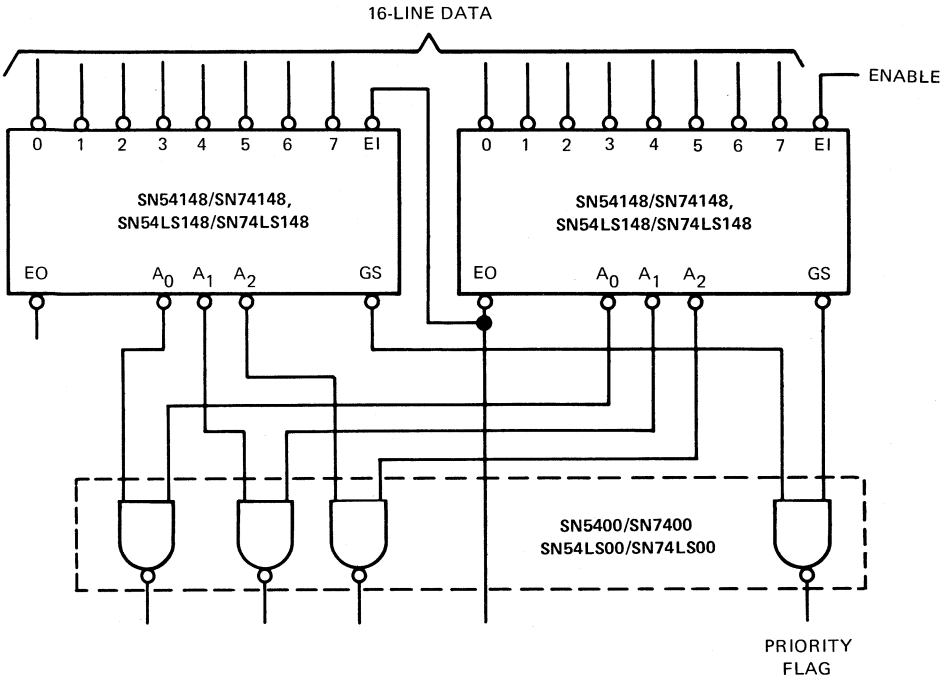
SN54LS148, SN74LS148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 2 kΩ, See Note 6		14	18	ns
t_{PHL}						15	25	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			20	36	ns
t_{PHL}						16	29	
t_{PLH}	0 thru 7	EO	Out-of-phase output			7	18	ns
t_{PHL}						25	40	
t_{PLH}	0 thru 7	GS	In-phase output			35	55	ns
t_{PHL}						9	21	
t_{PLH}	EI	A0, A1, or A2	In-phase output			16	25	ns
t_{PHL}						12	25	
t_{PLH}	EI	GS	In-phase output			12	17	ns
t_{PHL}						14	36	
t_{PLH}	EI	EO	In-phase output			12	21	ns
t_{PHL}						23	35	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low level output

NOTE 6: Load circuits and waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA



Full 4-bit binary 16-line-to-4-line encoding can be implemented as shown above. The enable input must be low to enable the function. Decoding with 2-input NAND gates produces true (active-high) data for the 4-line binary outputs. If active-low data is required, the SN5408/SN7408 or SN54LS08/SN74LS08 AND gate may be used, respectively.

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611819, DECEMBER 1972—REVISED OCTOBER 1976

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	11 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	11 ns†	30 mW
'LS152	11 ns†	28 mW
'S151	4.5 ns	225 mW

†Tentative data

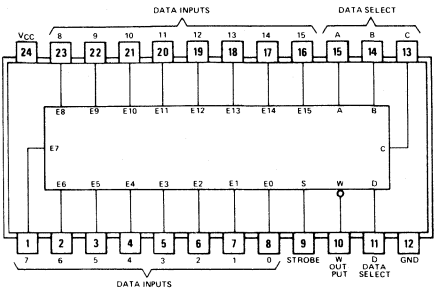
description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

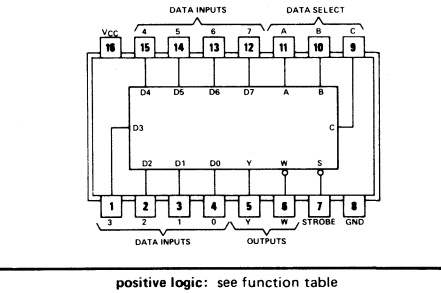
The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

SN54150 . . . J OR W PACKAGE
SN74150 . . . J, N OR NT PACKAGE
(TOP VIEW)



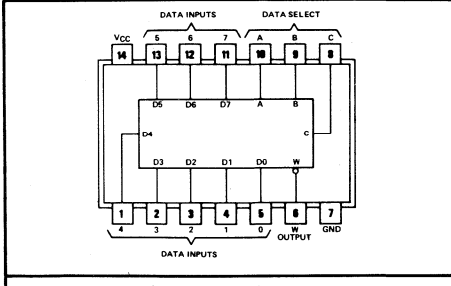
positive logic: see function table

SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A, SN74LS151, SN74S151 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54152A, SN54LS152 . . . W PACKAGE
(TOP VIEW)



positive logic: see function table

logic

'150

FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

'151A, 'LS151, 'S151

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

'152A, 'LS152

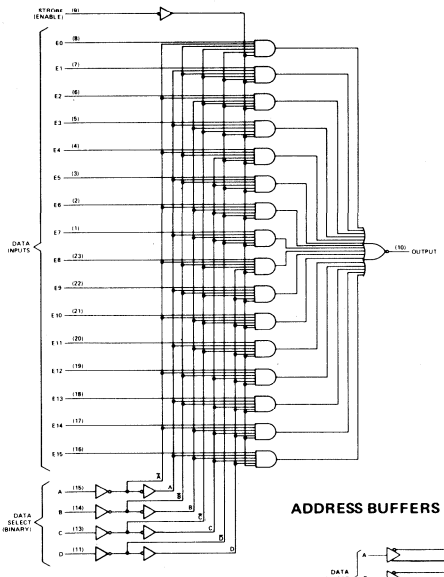
FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

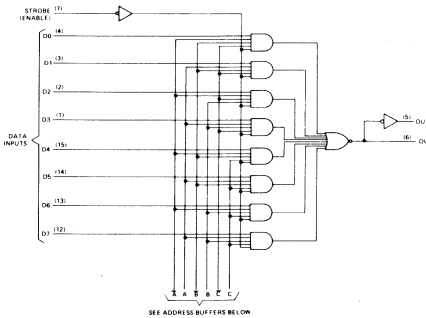
H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

functional block diagrams

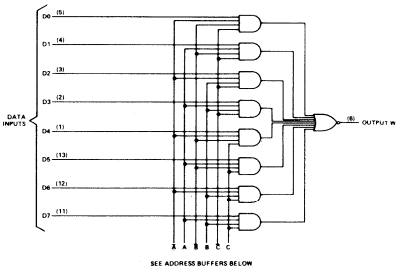
'150



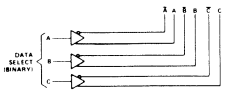
'151A, 'LS151, 'S151



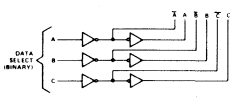
'152A, 'LS152



ADDRESS BUFFERS FOR '151A, '152A



ADDRESS BUFFERS FOR 'LS151, 'S151, 'LS152



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range: . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the '150, input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'150			'151A, '152A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA							−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−55	−20		−55	mA
			SN74'	−18		−55	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	'150		40	68				mA
			'151A					29	48	
			'152A					26	43	

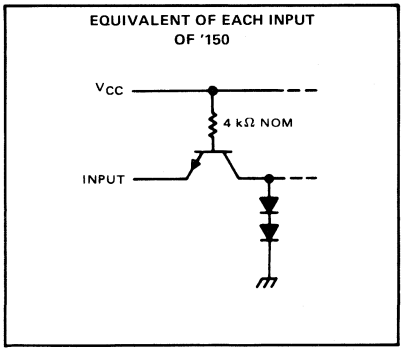
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output of the '151A should be shorted at a time.
NOTE 3: I_{CC} is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

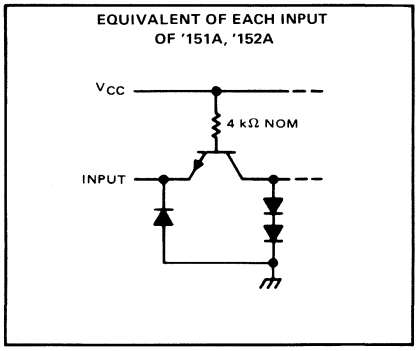
switching characteristics, V_{CC} = 5 V, T_A = 25°C

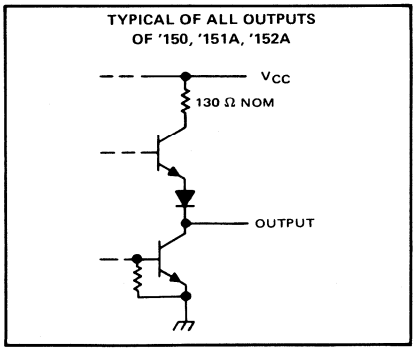
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'150			'151A, '152A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 400 Ω, See Note 4					25	38	ns
t_{PHL}								25	38	
t_{PLH}	A, B, C, or D (3 levels)	W			23	35		17	26	ns
t_{PHL}					22	33		19	30	
t_{PLH}	Strobe	Y						21	33	ns
t_{PHL}								22	33	
t_{PLH}	Strobe	W			15.5	24		14	21	ns
t_{PHL}					21	30		15	23	
t_{PLH}	D0 thru D7	Y						13	20	ns
t_{PHL}								18	27	
t_{PLH}	E0 thru E15, or D0 thru D7	W			8.5	14		8	14	ns
t_{PHL}					13	20		8	14	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open, All inputs at 4.5 V	'LS151		6.0	10		6.0	10	mA
			'LS152		5.6	9				

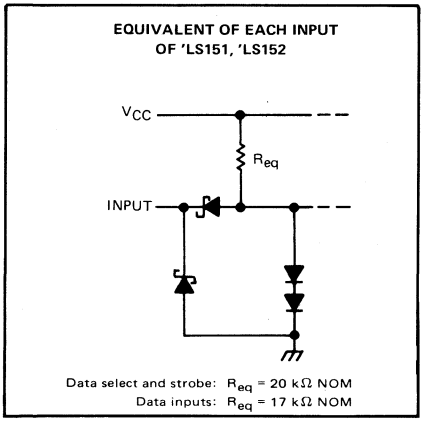
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

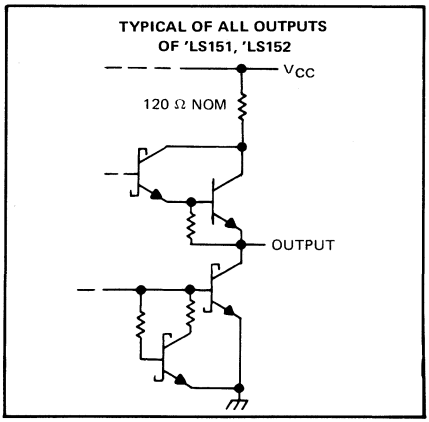
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS', SN74LS' MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 5		27	43	ns
t_{PHL}					18	30	
t_{PLH}	A, B, or C (3 levels)	W			14	23	ns
t_{PHL}					20	32	
t_{PLH}	Strobe	Y			26	42	ns
t_{PHL}					20	32	
t_{PLH}	Strobe	W			15	24	ns
t_{PHL}					18	30	
t_{PLH}	Any D	Y			20	32	ns
t_{PHL}					16	26	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					12	20	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 5: See load circuits and waveforms on page 3-11.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S151 Circuits . . . . . −55°C to 125°C
SN74S151 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S151			SN74S151			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs at 4.5 V, All outputs open			45	70	mA

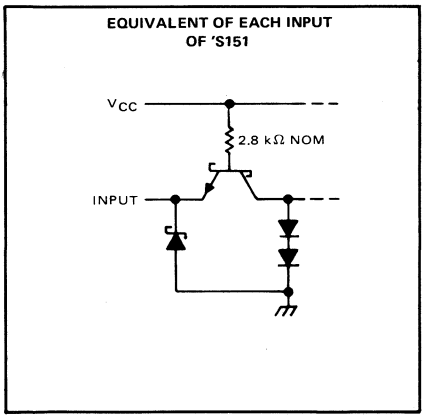
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

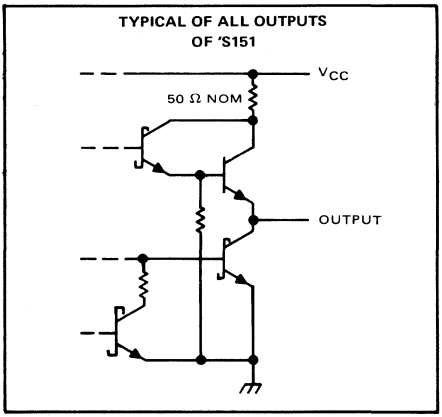
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S151, SN74S151			UNIT
				MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 4		12	18	ns
t_{PHL}					12	18	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	Strobe	Y			11	16.5	ns
t_{PHL}					12	18	
t_{PLH}	Strobe	W			9	13	ns
t_{PHL}					8.5	12	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 4: See load circuits and waveforms on page 3-10.

schematics of inputs and outputs





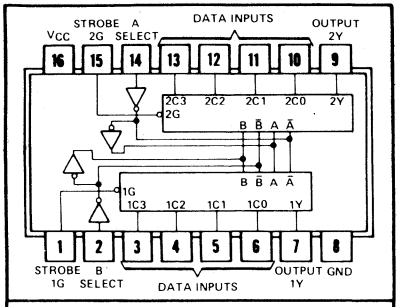
TYPES SN54153, SN54LS153, SN54S153, SN74153, SN74LS153, SN74S153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611852, DECEMBER 1972 – REVISED OCTOBER 1976

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES FROM DATA	FROM STROBE	FROM SELECT	TYPICAL POWER DISSIPATION
'153	14 ns	17 ns	22 ns	180 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

SN54153, SN54LS153, SN54S153 . . . J OR W PACKAGE
SN74153, SN74LS153, SN74S153 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

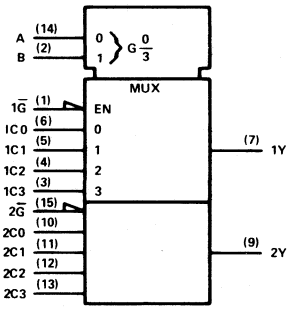
Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

logic symbol



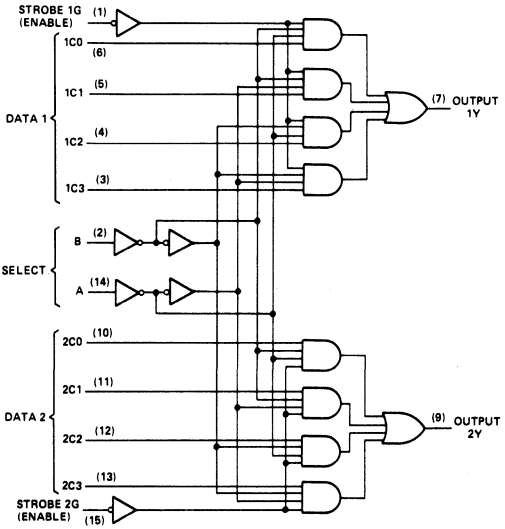
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '153, 'S153 . . . . . 5.5 V
'LS153 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

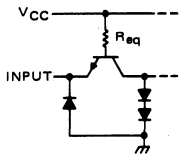
REVISED DECEMBER 1980

functional block diagram



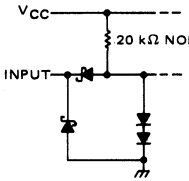
schematics of inputs and outputs

EQUIVALENT OF INPUTS OF '153

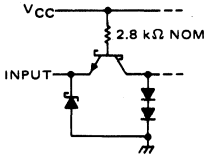


'153: R_{eq} = 4 kΩ NOM

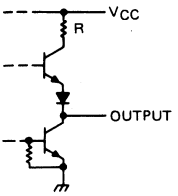
EQUIVALENT OF INPUTS OF 'LS153 EXCEPT 1G AND 2G INPUTS



EQUIVALENT OF INPUTS OF 'S153

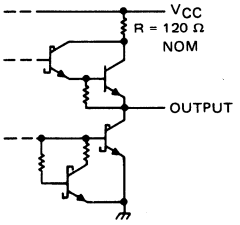


TYPICAL OF OUTPUTS OF '153

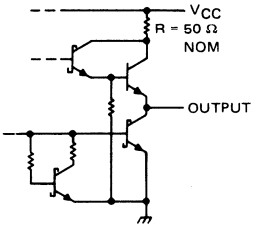


'153: R = 130 Ω NOM

TYPICAL OF OUTPUTS OF 'LS153



TYPICAL OF OUTPUTS OF 'S153



recommended operating conditions

	SN54153			SN74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54153			SN74153			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2		36	52		36	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 30 pF, R_L = 400 Ω, See Note 3		12	18	ns
t_{PHL}	Data	Y			15	23	ns
t_{PLH}	Select	Y			22	34	ns
t_{PHL}	Select	Y			22	34	ns
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}	Strobe	Y			15	23	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS153			SN74LS153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS153			SN74LS153			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V				0.4			0.4	mA
		1$\overline{G}$ and 2$\overline{G}$ inputs			−0.2			−0.2	
I_{OS} Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCL} Supply current, output low	V_{CC} = MAX, See Note 2			6.2	10		6.2	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 4		10	15	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54S153			SN74S153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2			45	70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 280 Ω, See Note 3		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe	Y			10	15	ns
t_{PHL}	Strobe	Y			9	13.5	ns

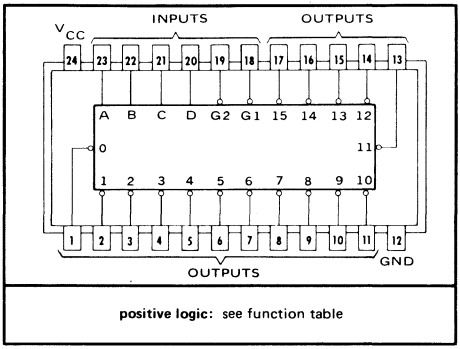
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54154, SN74154, 4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7211805, DECEMBER 1972

- '154 is Ideal for High-Performance Memory Decoding
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits

SN54154 . . . J OR W PACKAGE
SN74154 . . . J, N OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

TYPE	TYPICAL AVERAGE PROPAGATION DELAY 3 LEVELS OF LOGIC	STROBE	TYPICAL POWER DISSIPATION
'154	23 ns	19 ns	170 mW

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high-speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL and DTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C;
Series 74 devices are characterized for operation from 0°C to 70°C.

logic

FUNCTION TABLE

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
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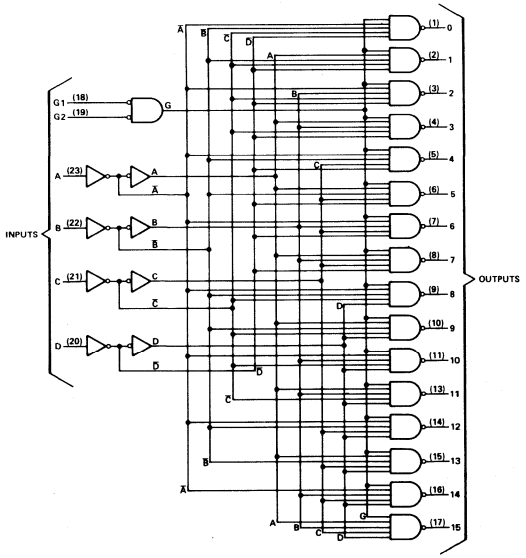
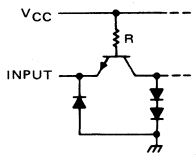
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

functional block diagram and schematics of inputs and outputs

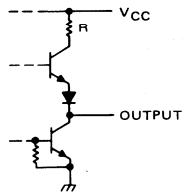


EQUIVALENT OF EACH INPUT



'154: R = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



'154: R = 130 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54154			SN74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54154			SN74154			UNIT
			MIN	TYP	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		34	49		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

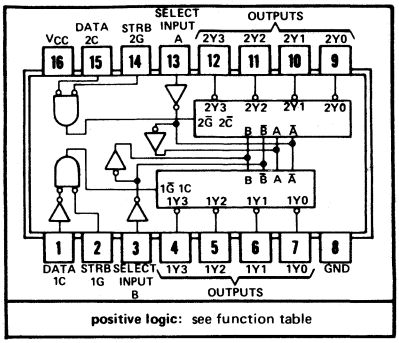
TYPES SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7611850, MARCH 1974—REVISED OCTOBER 1976

- **Applications:**
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
  - Totem Pole ('155, 'LS155A)
  - Open-Collector ('156, 'LS156)

TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155A	18 ns	31 mW
'LS156	32 ns	31 mW

SN54155, SN54156, SN54LS155A, SN54LS156 . . . J OR W PACKAGE
SN74155, SN74156, SN74LS155A, SN74LS156 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

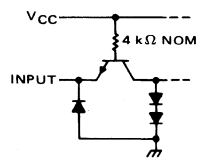
These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

Series 54 and 54LS are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

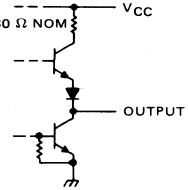
'155, '156

EQUIVALENT OF EACH INPUT



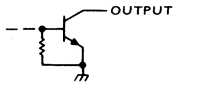
'155

TYPICAL OF ALL OUTPUTS



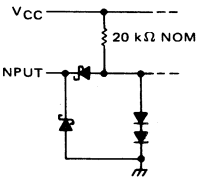
'156

TYPICAL OF ALL OUTPUTS



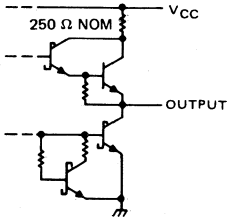
'LS155A 'LS156

EQUIVALENT OF EACH INPUT



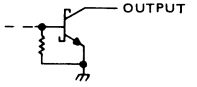
'LS155A

TYPICAL OF ALL OUTPUTS

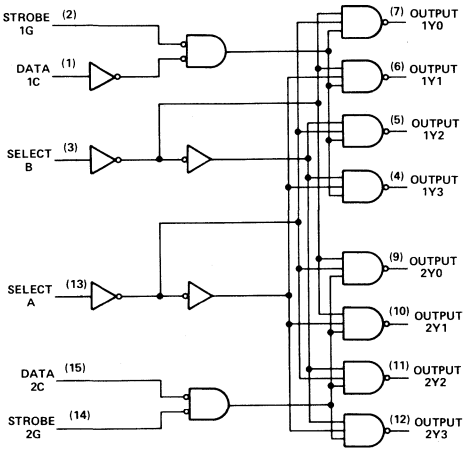


'LS156

TYPICAL OF ALL OUTPUTS



functional block diagram and logic



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155A, 'LS156 . . . . . 7 V
Off-state output voltage: '156 . . . . . 5.5 V
'LS156 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54155 SN74155			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54155	−20		−55	mA
			SN74155	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54155		25	35	mA
			SN74155		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS155A			SN74LS155A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS155A			SN74LS155A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155A SN74LS155A			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 4		10	15	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			19	30	ns
t_{PLH}	A or B	Y	3			17	26	ns
t_{PHL}	A or B	Y	3			19	30	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			18	27	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54156 SN74156			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54156		25	35	mA
			SN74156		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			20	30	ns
t_{PLH}	A or B	Y	3			23	34	ns
t_{PHL}	A or B	Y	3			23	34	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			22	33	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS156			SN74LS156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS156			SN74LS156			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C 1G, or 2G	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 4		25	40	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			34	51	ns
t_{PLH}	A or B	Y	3			31	46	ns
t_{PHL}	A or B	Y	3			34	51	ns
t_{PLH}	1C	Y	3			32	48	ns
t_{PHL}	1C	Y	3			32	48	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54157, SN54LS157, SN54LS158, SN54S157, SN54S158, SN74157, SN74LS157, SN74LS158, SN74S157, SN74S158 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611847, MARCH 1974—REVISED OCTOBER 1976

features

- **Buffered Inputs and Outputs**
- **Three Speed/Power Ranges Available**

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'LS157	9 ns	49 mW
'S157	5 ns	250 mW
'LS158	7 ns	24 mW
'S158	4 ns	195 mW

applications

- **Expand Any Data Input Point**
- **Multiplex Dual Data Buses**
- **Generate Four Functions of Two Variables (One Variable Is Common)**
- **Source Programmable Counters**

description

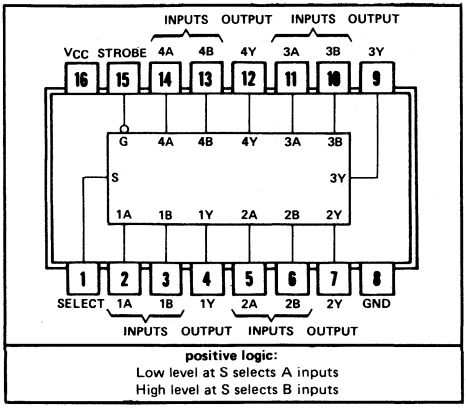
These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'LS157, and 'S157 present true data whereas the 'LS158 and 'S158 present inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157 'LS157,'S157	'LS158 'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

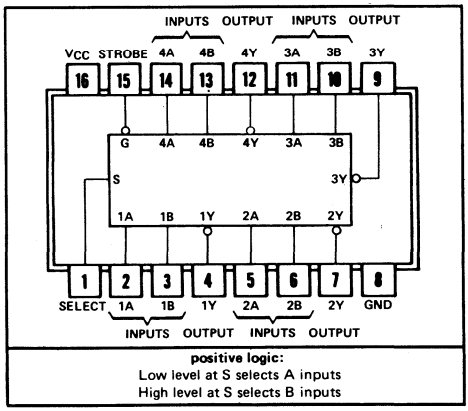
H = high level, L = low level, X = irrelevant

SN54157, SN54LS157, SN54S157 . . . J OR W PACKAGE
SN74157, SN74LS157, SN74S157 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

SN54LS158, SN54S158 . . . J OR W PACKAGE
SN74LS158, SN74S158 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low level at S selects A inputs
High level at S selects B inputs

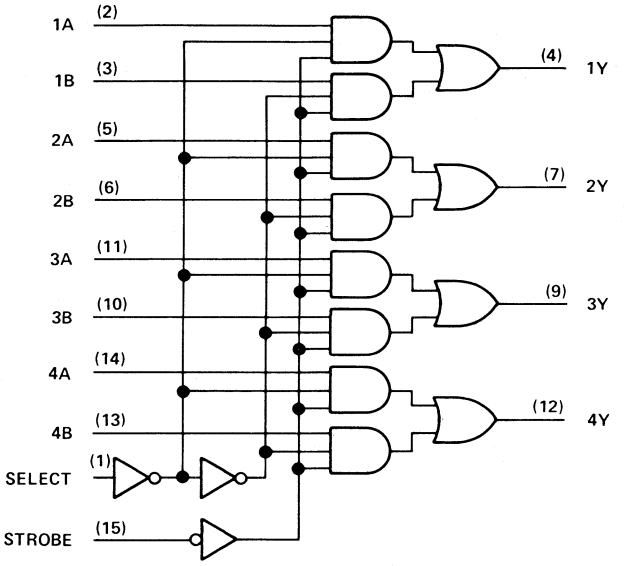
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '157, 'S158 . . . . . 5.5 V
'LS157, 'LS158 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74LS', SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

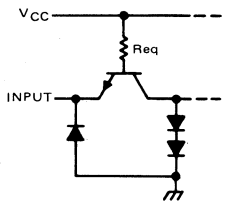
functional block diagram

'157



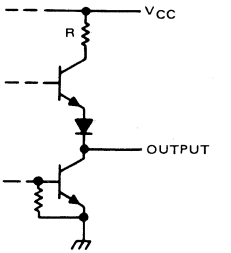
schematics of inputs and outputs

'157
EQUIVALENT OF EACH INPUT



'157: Req = 4 kΩ NOM

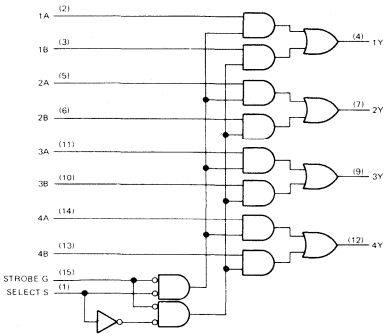
'157
TYPICAL OF ALL OUTPUTS



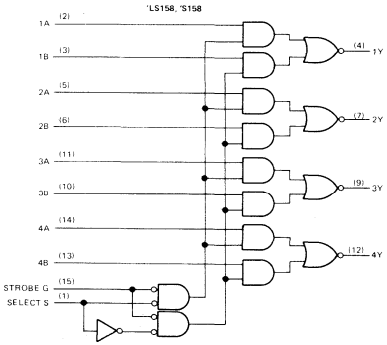
'157: R = 100 Ω NOM

functional block diagrams

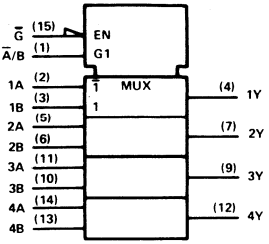
'LS157, 'S157



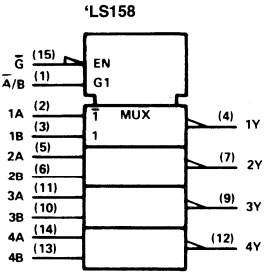
'LS158, 'S158



'LS157



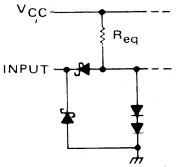
'LS158



schematics of inputs and outputs

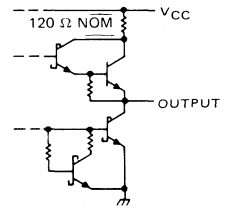
'LS157, 'LS158

EQUIVALENT OF EACH INPUT



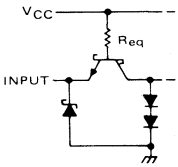
S or G inputs: R_{eq} = 8.5 kΩ NOM
A or B inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF ALL OUTPUTS



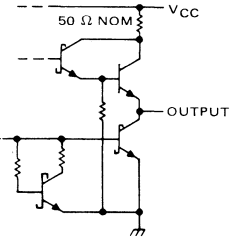
'S157, 'S158

EQUIVALENT OF EACH INPUT



S or G inputs: R_{eq} = 1.4 kΩ NOM
A or B inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS



7

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54157			SN74157			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		30	48		30	48	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω, See Note 3		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	S or G input	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
		A or B input					0.1			0.1	
I_{IH}	High-level input current	S or G input	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		A or B input					20			20	
I_{IL}	Low-level input current	S or G input	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		A or B input					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	'LS157		9.7	16		9.7	16	mA
				'LS158		4.8	8		4.8	8	
			V_{CC} = MAX, All A inputs at 4.5 V, All other inputs at 0 V	'LS158		6.5	11		6.5	11	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	'LS157 MIN	'LS157 TYP	'LS157 MAX	'LS158 MIN	'LS158 TYP	'LS158 MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 2 kΩ, See Note 4		9	14		7	12	ns
t_{PHL}				9	14		10	15	
t_{PLH}	Strobe			13	20		11	17	ns
t_{PHL}				14	21		18	24	
t_{PLH}	Select			15	23		13	20	ns
t_{PHL}				18	27		16	24	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S157 SN74S157			SN54S158 SN74S158			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
				Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	S or G input	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
		A or B input					50			50	
I_{IL}	Low-level input current	S or G input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
		A or B input					−2			−2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 4.5 V, See Note 2			50	78		39	61	mA
			V_{CC} = MAX, A inputs at 4.5 V, B,G,S inputs at 0 V, see Note 2							81	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 280 Ω, See Note 3		5	7.5		4	6	ns
t_{PHL}				4.5	6.5		4	6	
t_{PLH}	Strobe			8.5	12.5		6.5	11.5	ns
t_{PHL}				7.5	12		7	12	
t_{PLH}	Select			9.5	15		8	12	ns
t_{PHL}				9.5	15		8	12	

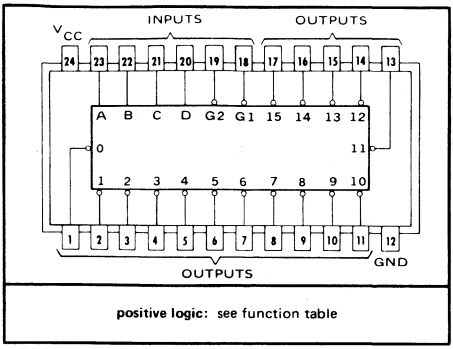
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54159, SN74159
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS
WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7211800, DECEMBER 1972

- Open-Collector Outputs for Interfacing with MOS or Memory Decoders/Drivers
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Typical Average Propagation Delay Times:
  24 ns through 3 Levels of Logic
  19 ns from Strobe Input
- Output Off-State Current is Less Than 50 μA
- Fully Compatible with Most TTL, DTL, and MSI Circuits

SN54159 . . . J OR W PACKAGE
SN74159 . . . J, N, OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing MOS memory decoding or for interfacing with discrete memory address drivers. For ultra-high-speed applications, the SN54S138/SN74S138 or SN54S139/SN74S139 is recommended.

These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54159 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74159 is characterized for operation from 0°C to 70°C.

function table

Same as SN54154, SN74154. See page 7-161.

functional block diagram

Same as SN54154, SN74154. See page 7-161.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54159 Circuits	−55°C to 125°C
SN74159 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54159			SN74159			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded		34	56	mA

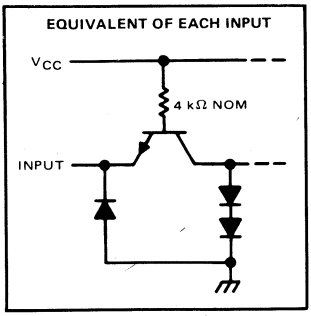
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

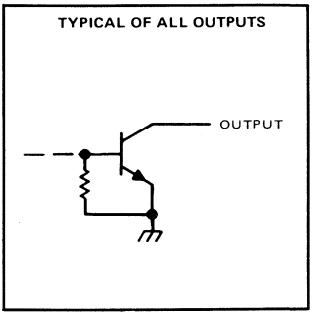
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 2		23	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			22	36	ns

NOTE 2: See load circuit and waveforms shown on page 3-10.

schematics of inputs and outputs





TYPES SN54160 THRU SN54163, SN54LS160A THRU SN54LS163A, SN54S162, SN54S163, SN74160 THRU SN74163, SN74LS160A THRU SN74LS163A, SN74S162, SN74S163 SYNCHRONOUS 4-BIT COUNTERS

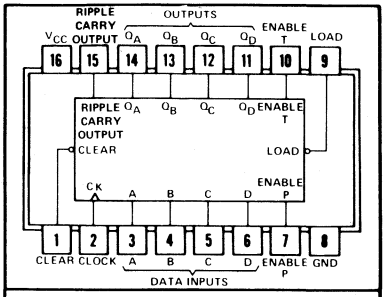
BULLETIN NO. DL-S 7611385, OCTOBER 1976

'160, '161, 'LS160A, 'LS161A . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
'162, '163, 'LS162A, 'LS163A, 'S162, 'S163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs

TYPE	TYPICAL PROPAGATION TIME, CLOCK TO Q OUTPUT	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'160 thru '163	14 ns	32 MHz	305 mW
'LS160A thru 'LS163A	14 ns	32 MHz	93 mW
'S162 and 'S163	9 ns	70 MHz	475 mW

SERIES 54', 54LS', 54S' . . . J OR W PACKAGE
SERIES 74', 74LS', 74S' . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The '160, '162, 'LS160A, 'LS162A, and 'S162 are decade counters and the '161, '163, 'LS161A, 'LS163A, and 'S163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of the '160 thru '163 should be avoided when the clock is low if the enable inputs are high at or before the transition. This restriction is not applicable to the 'LS 160A thru 'LS163A or 'S162 or 'S163. The clear function of the '160, '161, 'LS160A, and 'LS161A is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The clear function for the '162, '163, 'LS162A, 'LS163A, 'S162, and 'S163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count lengths to be modified as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL). Low-to-high transitions at the clear input of the '162 and '163 should be avoided when the clock is low if the enable and load inputs are high at or before the transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the '160 thru '163 should occur only when the clock input is high. Transitions at the enable P or T inputs of the 'LS160A thru 'LS163A or 'S162 and 'S163 are allowed regardless of the level of the clock input. The use of the ripple carry output as an edge trigger pulse is not recommended.

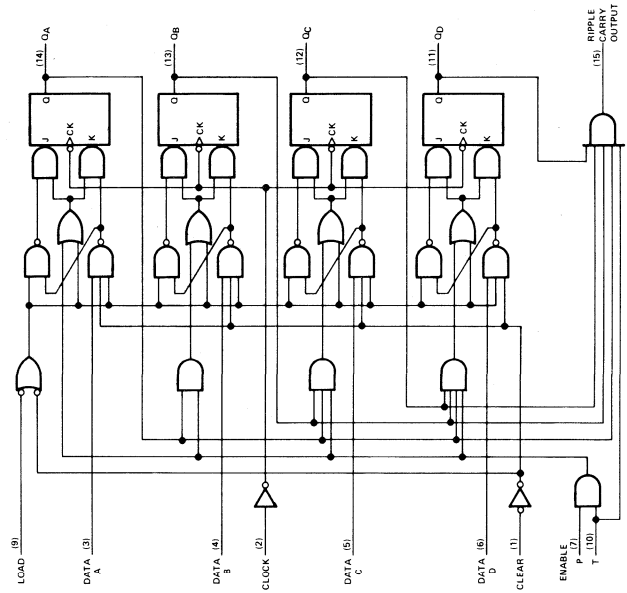
'LS160A thru 'LS163A, 'S162 and 'S163 feature a fully independent clock circuit. Changes at control inputs (enable P or T, or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS160A thru 'LS163A are completely new designs. Compared to the original 'LS160 thru 'LS163, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

functional block diagrams

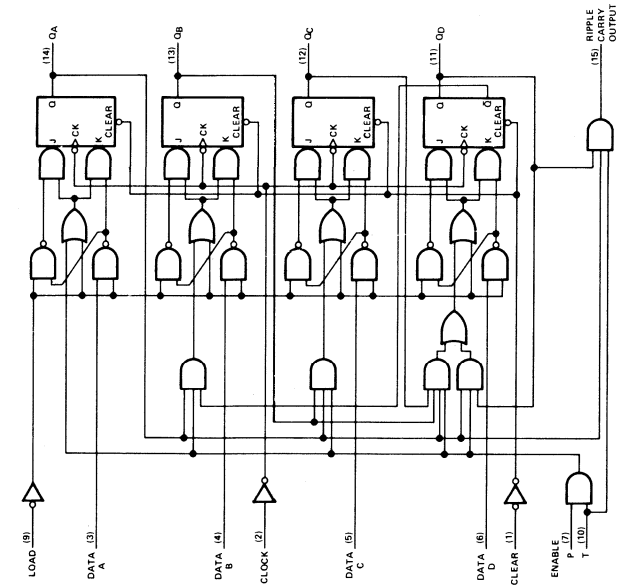
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

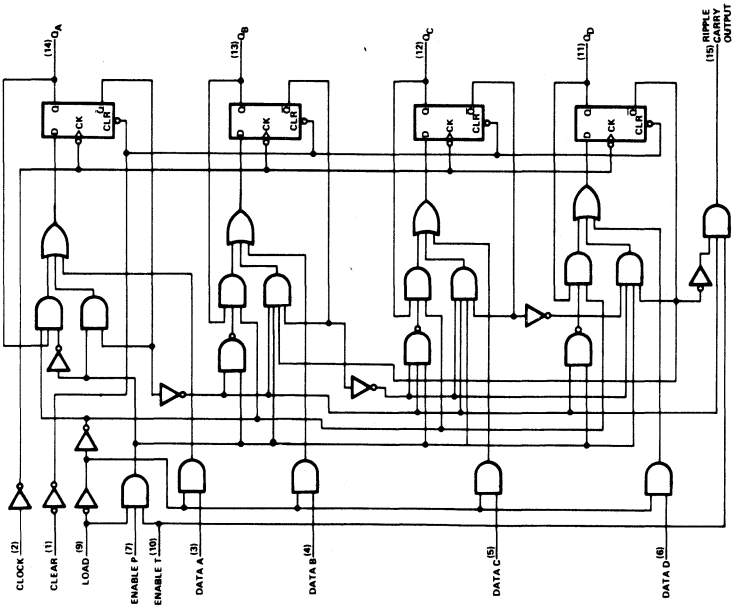
SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.



functional block diagram

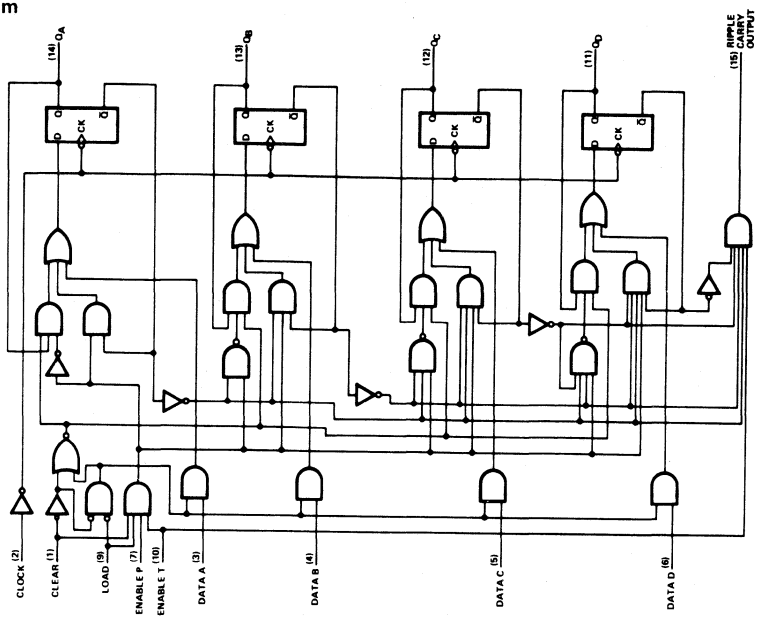
SN54LS160A, SN74LS160A SYNCHRONOUS DECADE COUNTERS

SN54LS162A, SN74LS162A synchronous decade counters are similar; however the clear is synchronous as shown for the SN54LS163A, SN74LS163A binary counters at right.



SN54LS163A, SN74LS163A SYNCHRONOUS BINARY COUNTERS

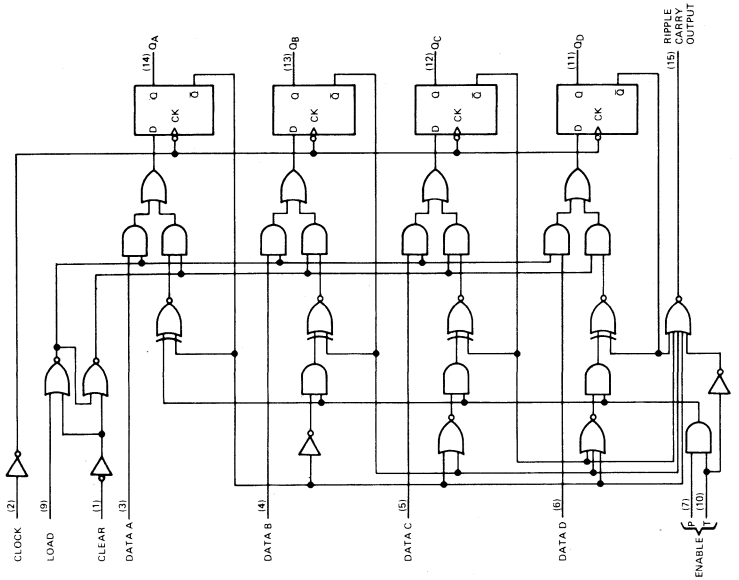
SN54LS161A, SN74LS161A synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54LS160A, SN74LS160A decade counters at left.



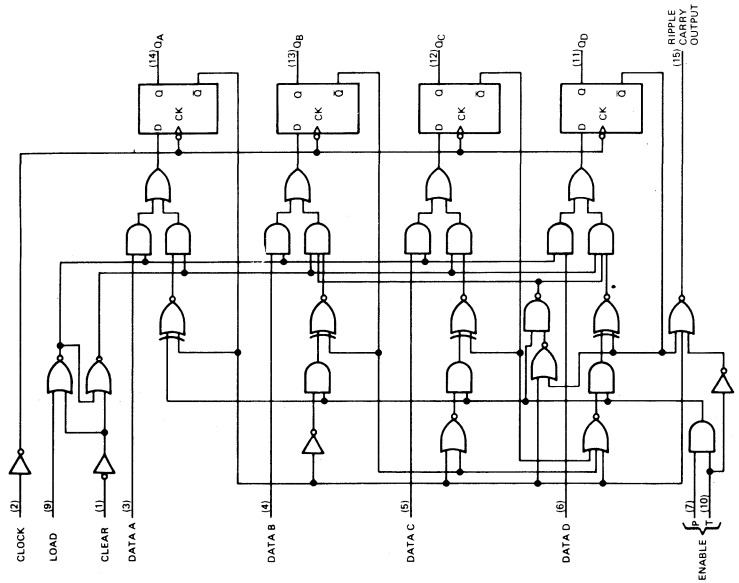
REVISED OCTOBER 1976

functional block diagrams

SN54S163, SN74S163 SYNCHRONOUS BINARY COUNTERS



SN54S162, SN74S162 SYNCHRONOUS DECADE COUNTERS

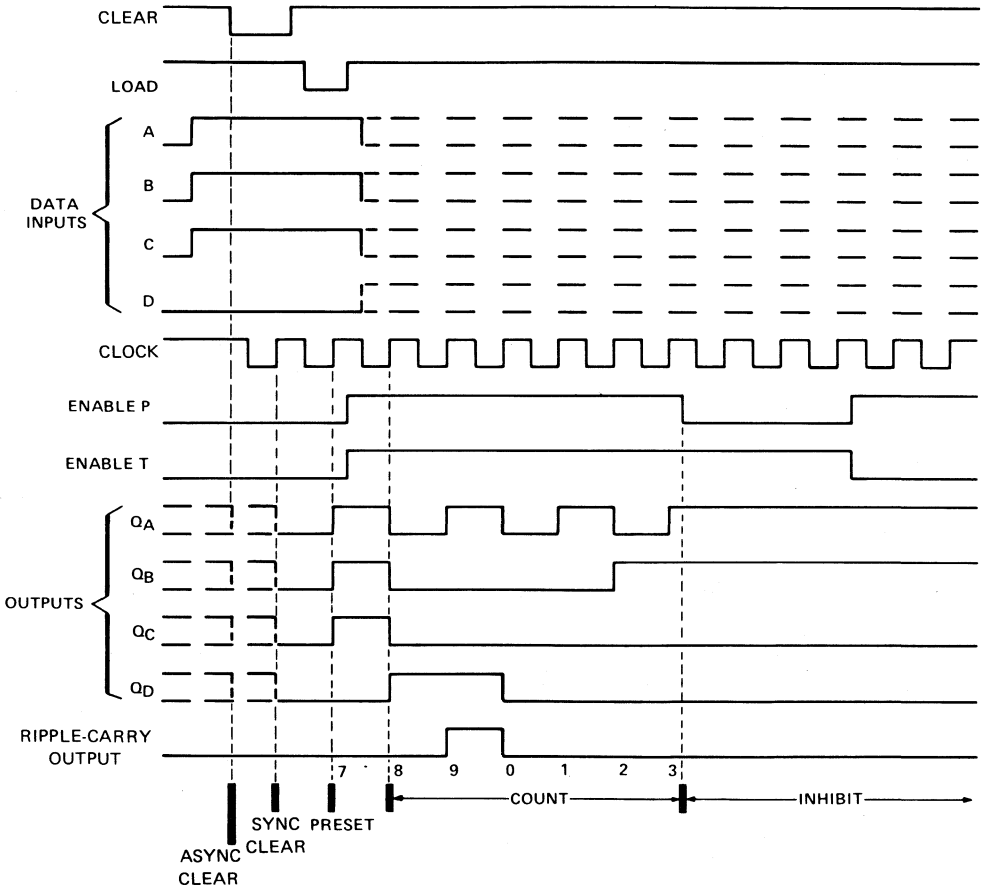


'160, '162, 'LS160A, 'LS162A, 'S162 DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('160 and 'LS160A are asynchronous; '162, 'LS162A,and 'S162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

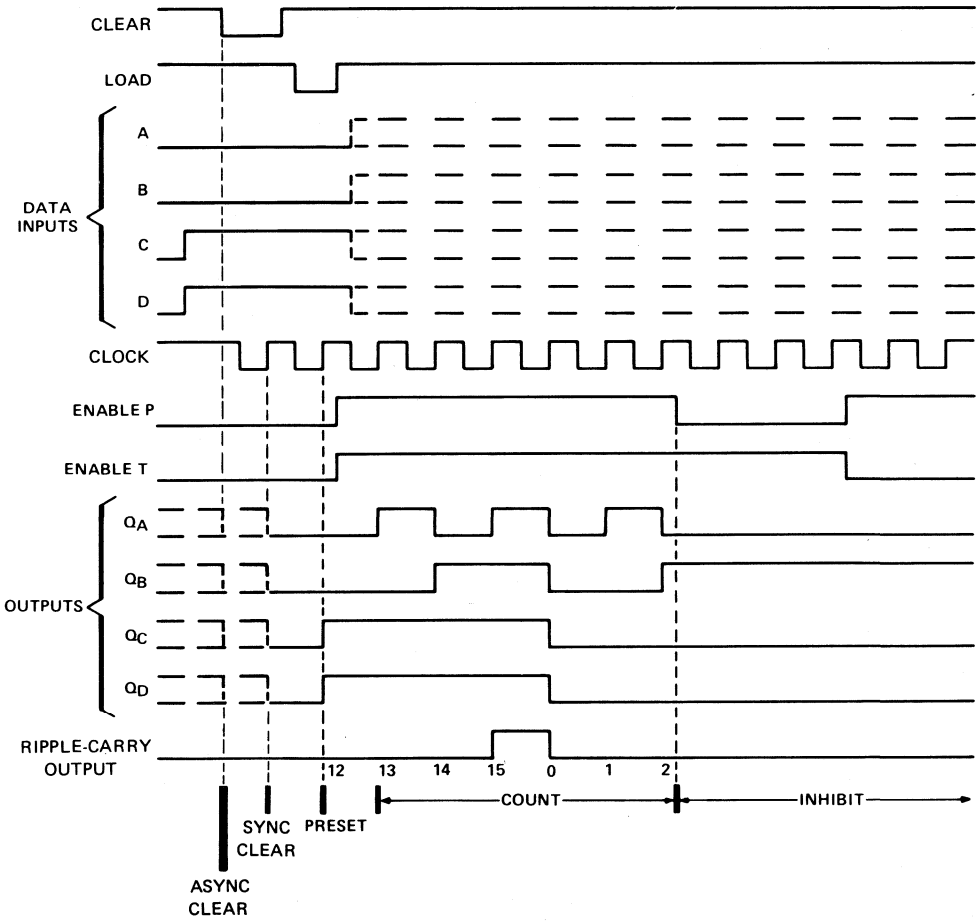


'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

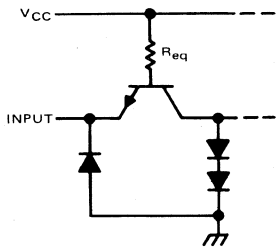
Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit



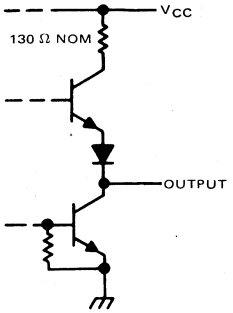
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Clock: R_{eq} = 2.8 kΩ NOM
Enable T: R_{eq} = 2 kΩ NOM
Clear, Enable P: R_{eq} = 4 kΩ NOM
A, B, C, D: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	Enable P	20			20			
	Load	25			25			
	Clear◇	20			20			
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

◇This applies only for '162 and '163, which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161 SN54162, SN54163			SN74160, SN74161 SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

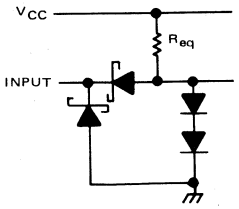
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2 and Notes 5 and 6	25	32		ns
t_{PLH}	Clock	Ripple carry			23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock (load input high)	Any Q			13	20	ns
t_{PHL}					15	23	
t_{PLH}	Clock (load input low)	Any Q			17	25	ns
t_{PHL}					19	29	
t_{PLH}	Enable T	Ripple carry			11	16	ns
t_{PHL}					11	16	
t_{PHL}	Clear	Any Q			26	38	ns

¶f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTES: 5. Load circuit is shown on page 3-10.
6. Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.

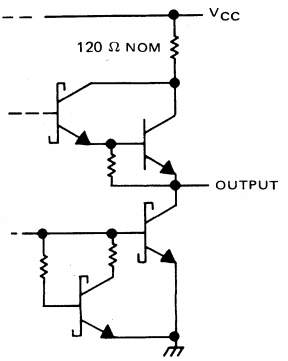
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data: R_{eq} = 2.5 kΩ NOM
Enable T, Load: R_{eq} = 10 kΩ NOM
Clock, Enable P: R_{eq} = 20 kΩ NOM
Clear ('LS160A, 'LS161A): R_{eq} = 20 kΩ NOM
Clear ('LS162A, 'LS163A): R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 7: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su} (see Figures 1 and 2)	Data inputs A, B, C, D	20			20			ns
	Enable P or T	20			20			
	Load	20			20			
	Clear◇	20			20			
Hold time at any input, t_h		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

◇ This applies only for 'LS162 and 'LS163, which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Data or enable P	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Load, clock, or enable T					0.2			0.2	
		Clear ('LS160A, 'LS161A)					0.1			0.1	
		Clear ('LS162A, 'LS163A)					0.2			0.2	
I_{IH}	High-level input current	Data or enable P	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Load, clock, or enable T					40			40	
		Clear ('LS160A, 'LS161A)					20			20	
		Clear ('LS162A, 'LS163A)					40			40	
I_{IL}	Low-level input current	Data or enable P	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Load, clock, or enable T					−0.8			−0.8	
		Clear ('LS160A, 'LS161A)					−0.4			−0.4	
		Clear ('LS162A, 'LS163A)					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX,	See Note 3		18	31		18	31	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX,	See Note 4		19	32		19	32	mA

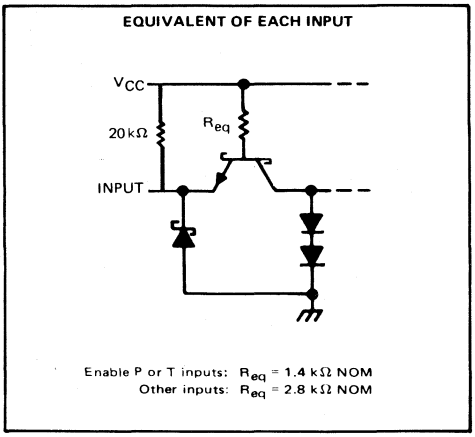
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

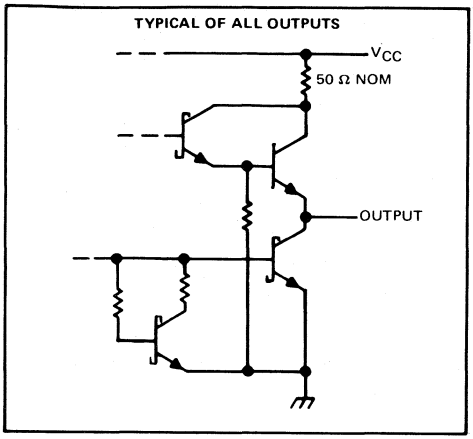
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2 and Notes 8 and 9	25	32		MHz
t_{PLH}	Clock	Ripple carry			20	35	ns
t_{PHL}					18	35	
t_{PLH}	Clock (load input high)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Clock (load input low)	Any Q			13	24	ns
t_{PHL}					18	27	
t_{PLH}	Enable T	Ripple carry			9	14	ns
t_{PHL}					9	14	
t_{PHL}	Clear	Any Q			20	28	ns

¶f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTES: 8. Load circuit is shown on page 3-11.
9. Propagation delay for clearing is measured from the clear input for the 'LS160A and 'LS161A or from the clock transition for the 'LS162A and 'LS163A.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54S162, SN54S163 (see Note 10) . . . . . −55°C to 125°C
SN74S162, SN74S163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S162, SN54S163			SN74S162, SN74S163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low)		10			10			ns
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su} (see Figure 4)	Data inputs, A, B, C, D	4			4			ns
	Enable P or T	12			12			
	Load	14			14			
	Clear	14			14			
	Load inactive-state	12			12			
	Clear inactive-state	12			12			
Release time, $t_{release}$ (see Figure 4)	Enable P or T			4			4	ns
Hold time, t_h (see Figure 4)	Data inputs A, B, C, D	3			3			ns
	Load	0			0			
	Clear	0			0			
Operating free-air temperature, T_A (see Note 10)		−55		125	0		70	°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.
10. An SN54S162 or SN54S163 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S162 SN54S163			SN74S162 SN74S163			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, Clock and data	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
	High-level input current, Other inputs		−10		−200	−10		−200	
I_{IL}	Low-level input current, Enable T	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
	Low-level input current, Other inputs				−2			−2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX		95	160		95	160	mA

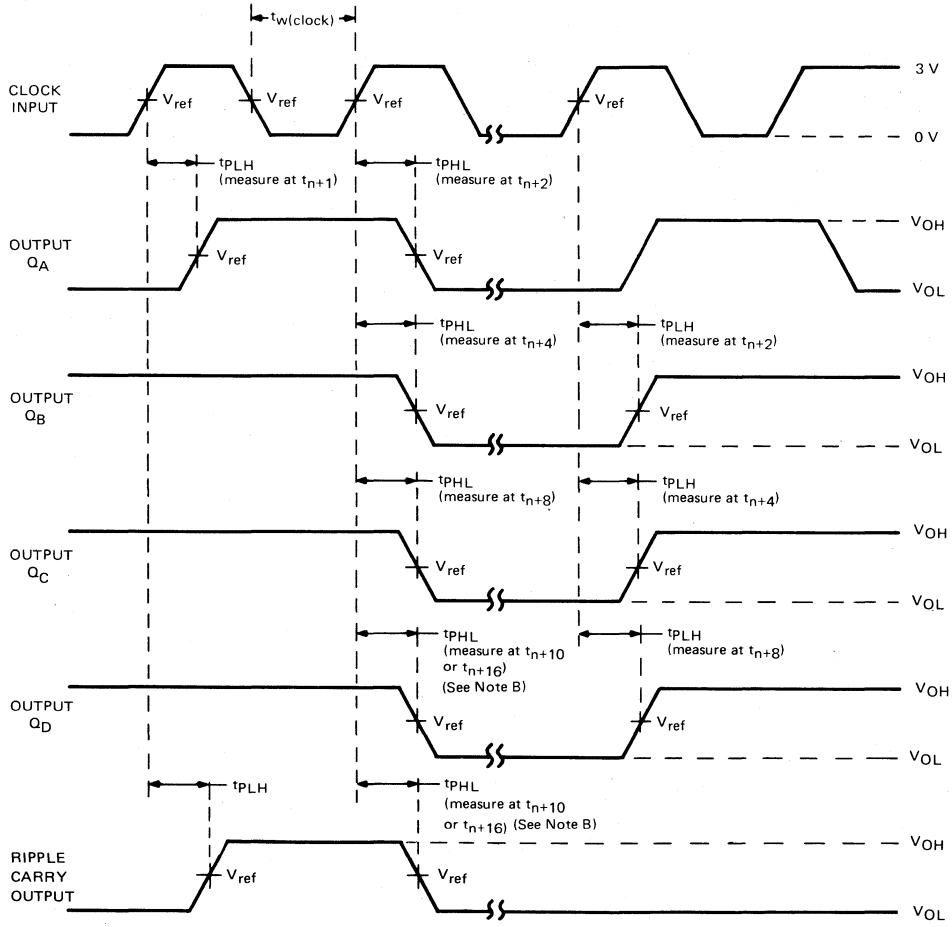
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Figures 1, 3, and 4 and Note 5	40	70		MHz
t_{PLH}	Clock	Ripple carry			14	25	ns
t_{PHL}					17	25	
t_{PLH}	Clock	Any Q			8	15	ns
t_{PHL}					10	15	
t_{PLH}	Enable T	Ripple carry			10	15	ns
t_{PHL}					10	15	

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 5: Load circuit is shown on page 3-10.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

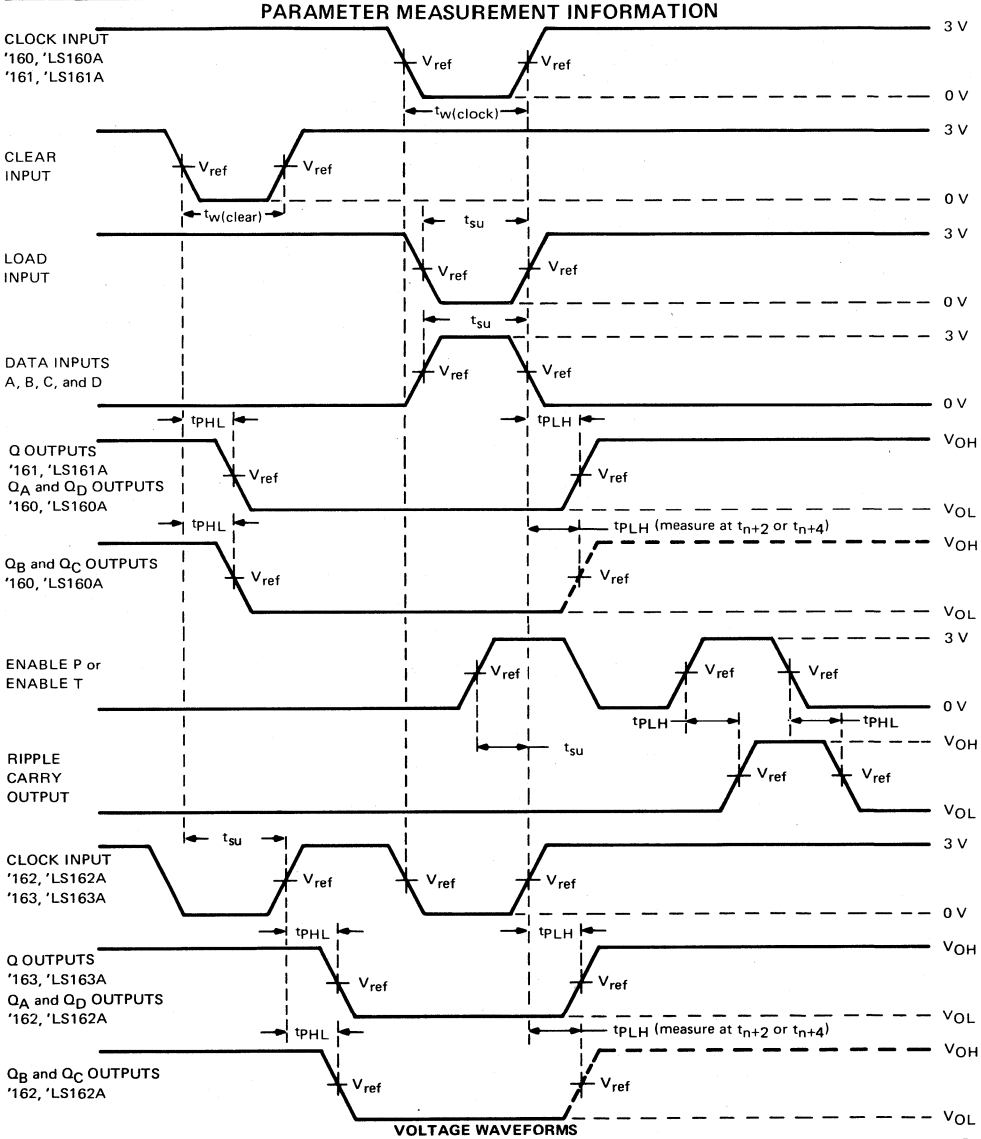
NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S162, 'S163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for '160, '162, 'LS160A, 'LS162A, and 'S162, and at t_{n+16} for '161, '163, 'LS161A, 'LS163A, and 'S163, where t_n is the bit time when all outputs are low.

C. For '160 thru '163, 'S162, and 'S163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 1–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

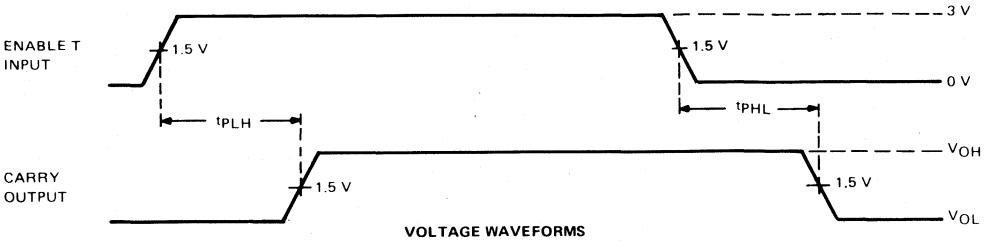
NOTES: A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '160 thru '163, $t_r \leq 10$ ns, $t_f \leq 10$ ns; and for 'LS160A thru 'LS163A, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. For '160 thru '163, $V_{ref} = 1.5$ V; for 'LS160A thru 'LS163A, $V_{ref} = 1.3$ V.

FIGURE 2–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

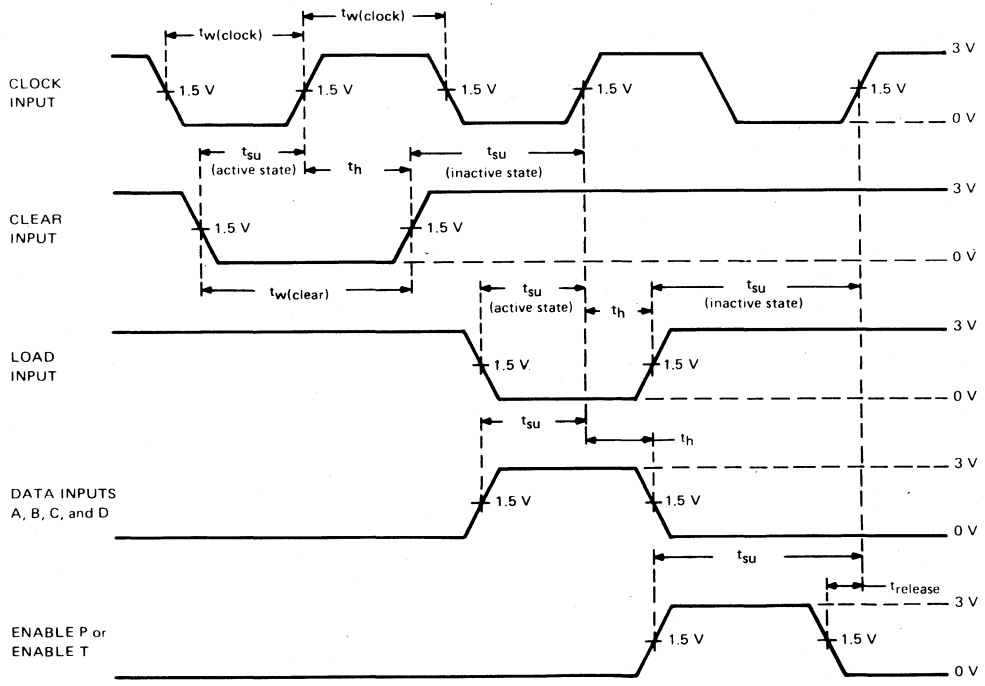


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\ \Omega$.

B. t_{PLH} and t_{PHL} from enable T input to carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S162, all Q outputs high for 'S163).

FIGURE 3–PROPAGATION DELAY TIMES FROM ENABLE T INPUT TO CARRY OUTPUT



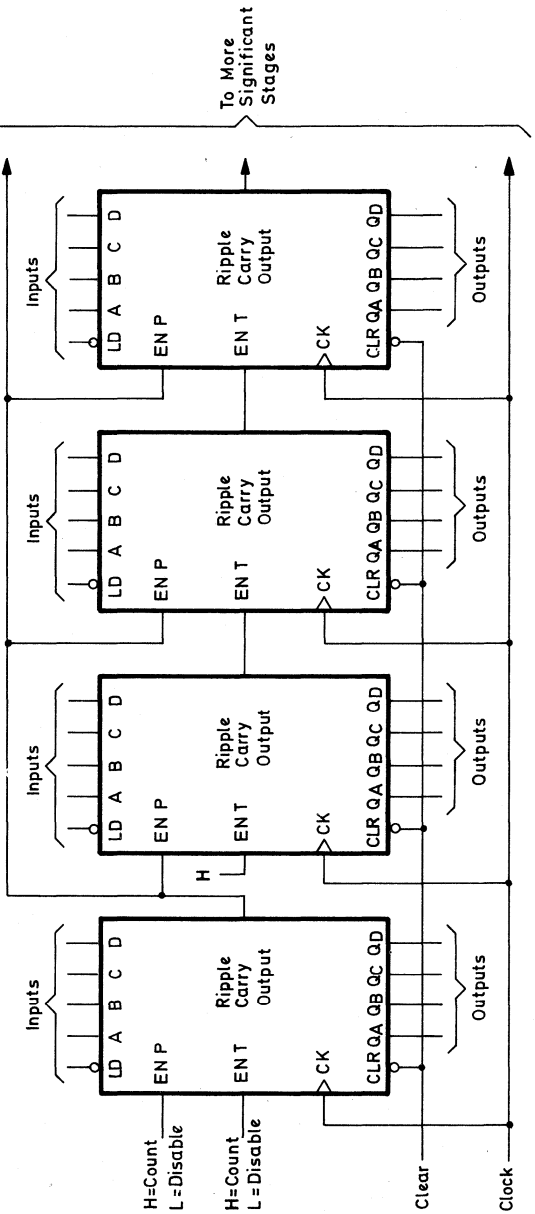
VOLTAGE WAVEFORMS

NOTE A: The input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\ \Omega$.

FIGURE 4–PULSE WIDTHS, SETUP TIMES, HOLD TIMES, AND RELEASE TIME

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160, '162, 'LS160A, 'LS162A, or 'S162 will count in BCD and the '161, '163, 'LS161A, 'LS163A or 'S163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



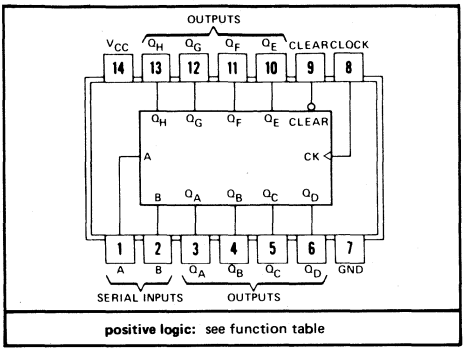
TYPES SN54164, SN54LS164, SN74164, SN74LS164
8-BIT PARALLEL-OUT SERIAL REGISTERS

BULLETIN NO. DL-S 7611835, MARCH 1974—REVISED OCTOBER 1976

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'LS164	36 MHz	10 mW per bit

SN54164, SN54LS164 . . . J OR W PACKAGE
SN74164, SN74LS164 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Series 54 and 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS devices are characterized for operation from 0°C to 70°C.

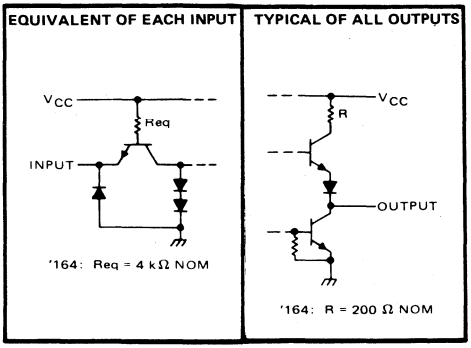
FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

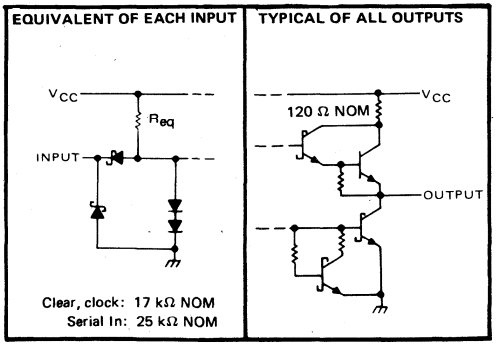
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

schematics of inputs and outputs

'164

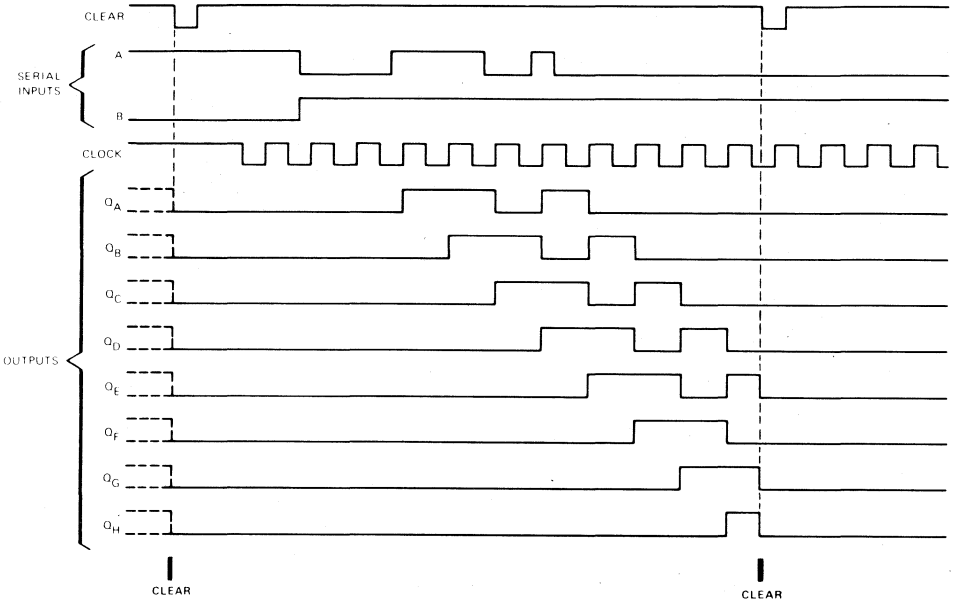


'LS164

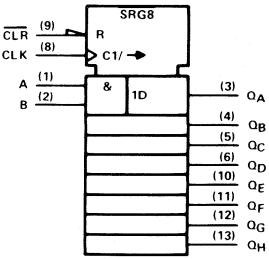


REVISED OCTOBER 1976

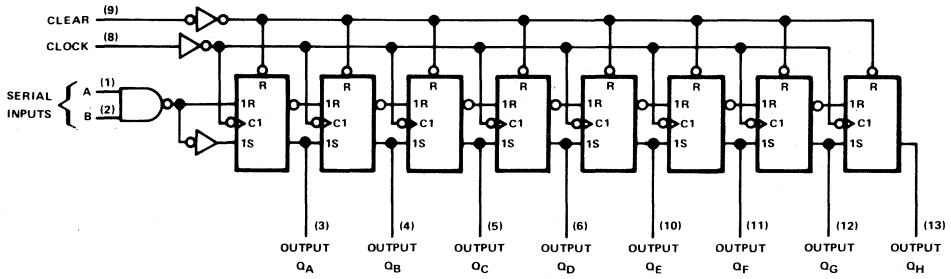
typical clear, shift, and clear sequences



logic symbol



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54164 . . . . . −55°C to 125°C
SN74164 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{su} (see Figure 1)	15			15			ns
Data hold time, t_h (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C
Clear inactive setup time, Min = 20 ns.	20			20			ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54164			SN74164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.2		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V,				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−10		−27.5	−9		−27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4 V		30			30		mA
			$V_{I(clock)}$ = 2.4 V		37	54		37	54	

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than two outputs should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		24	36	ns
			C_L = 50 pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	17	27	ns
			C_L = 50 pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from the clock input		C_L = 15 pF	10	21	32	ns
			C_L = 50 pF	10	25	37	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS164 . . . . . −55°C to 125°C
SN74LS164 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS164			SN74LS164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{su} (see Figure 1)	15			15			ns
Data hold time, t_h (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

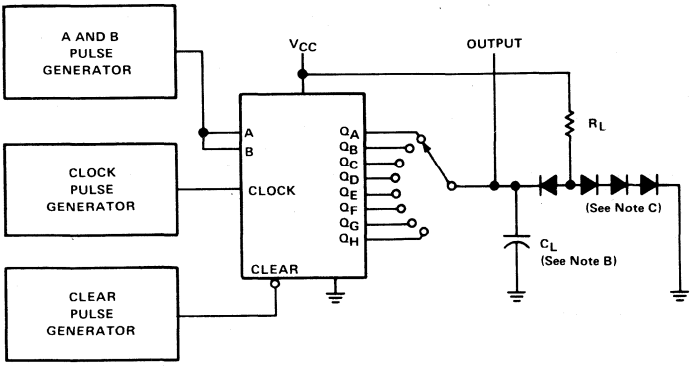
PARAMETER		TEST CONDITIONS†		SN54LS164			SN74LS164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			16	27		16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V applied to clear.

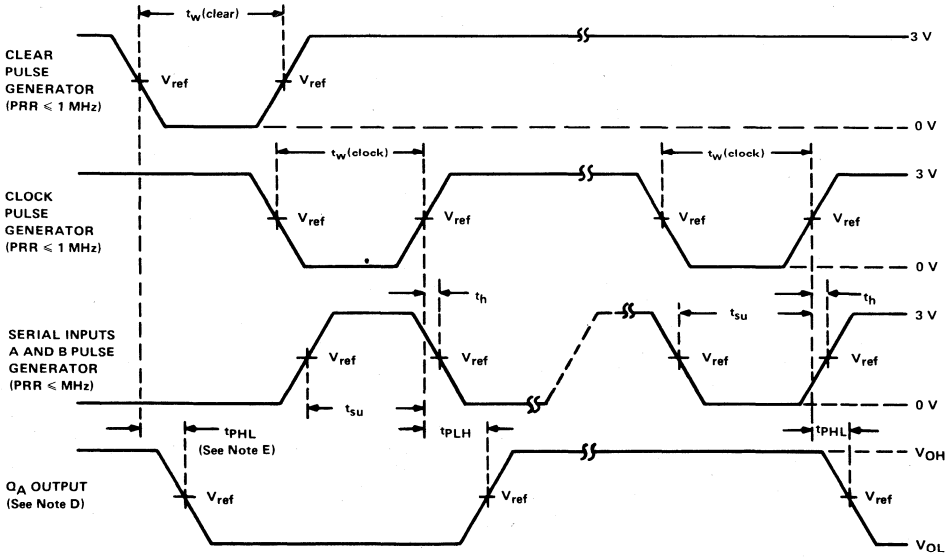
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input			24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input			21	32	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: duty cycle ≤ 50 %, $Z_{out} \approx 50\ \Omega$; for '164, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS164, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and jig capacitance.
C All diodes are 1N3064 or 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
F. For '164 V_{ref} = 1.5 V; for 'LS164, V_{ref} = 1.3 V.

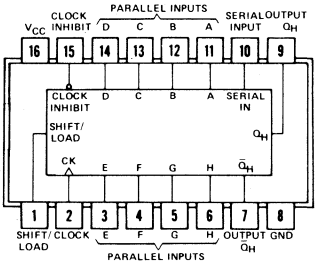
FIGURE 1–SWITCHING TIMES

TYPES SN54165, SN54LS165A, SN74165, SN74LS165A
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165A	35 MHz	105 mW

SN54165, SN54LS165A . . . J OR W PACKAGE
SN74165, SN74LS165A . . . J OR N PACKAGE
(TOP VIEW)



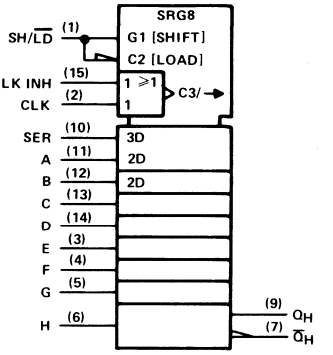
positive logic: see description

description

The '165 and 'LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

logic symbol



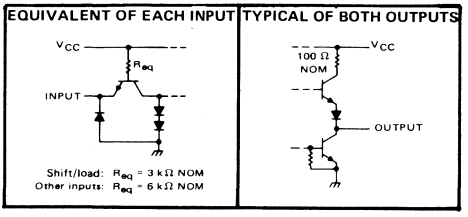
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

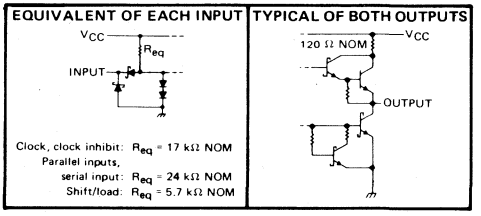
See explanation of function tables on page 3-8.

schematic of inputs and output

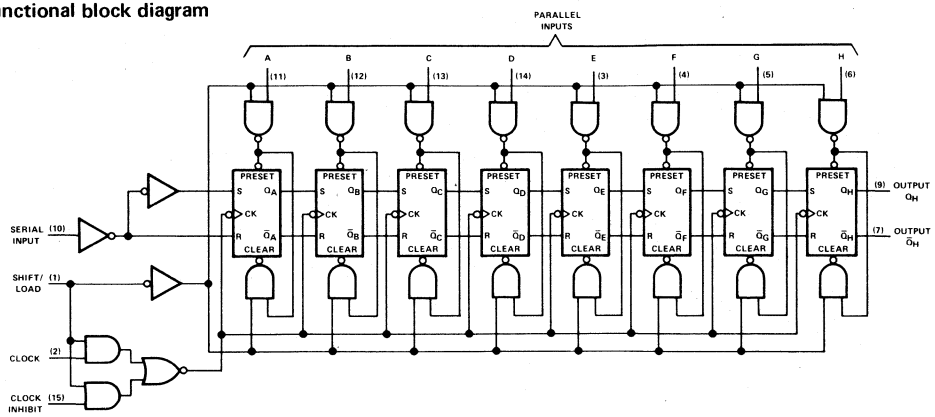
'165



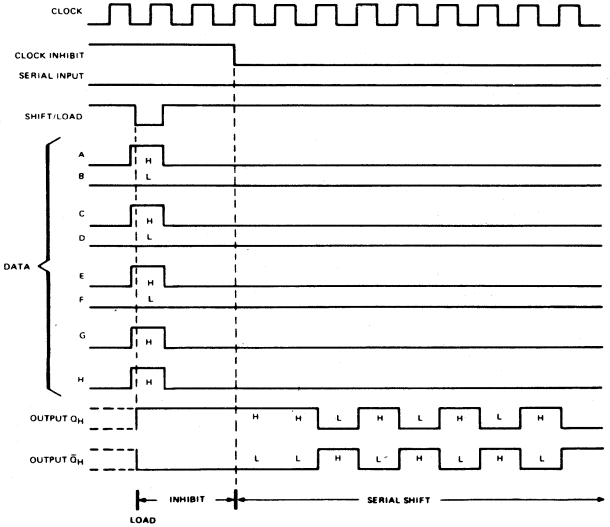
'LS165A



functional block diagram



typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: SN54165, SN74165	5.5 V
SN54LS165A, SN74LS165A	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54165, SN54LS165A	−55°C to 125°C
SN74165, SN74LS165A	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the shift/load input in conjunction with the clock-inhibit inputs.

recommended operating conditions

	SN54165			SN74165			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$ (clock high)	25			15			ns
Clock-enable setup time, t_{su} (see Figure 1)	30			30			ns
Parallel input setup time, t_{su} (see Figure 1)	10			10			ns
Serial input setup time, t_{su} (see Figure 2)	20			20			ns
Shift setup time, t_{su} (see Figure 2)	45			45			ns
Hold time at any input, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54165			SN74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Shift/load	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Shift/load	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift/load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

	SN54LS165A			SN74LS165A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	17			17			ns
Clock-enable setup time, t_{su} (see Figure 1)	30			30			ns
Parallel input setup time, t_{su} (see Figure 1)	10			10			ns
Serial input setup time, t_{su} (see Figure 2)	20			20			ns
Shift setup time, t_{su} (see Figure 2)	45			45			ns
Hold time at any input, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS165A			SN74LS165A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Shift/load	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Other inputs					0.1			0.1	
I_{IH}	High-level input current	Shift/load	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Other inputs					20			20	
I_{IL}	Low-level input current	Shift/load	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3		21	36		18	30	mA

NOTE 3: With the outputs open, clock inhibit and clock at 4.5 V, and a clock pulse applied to the shift/load input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

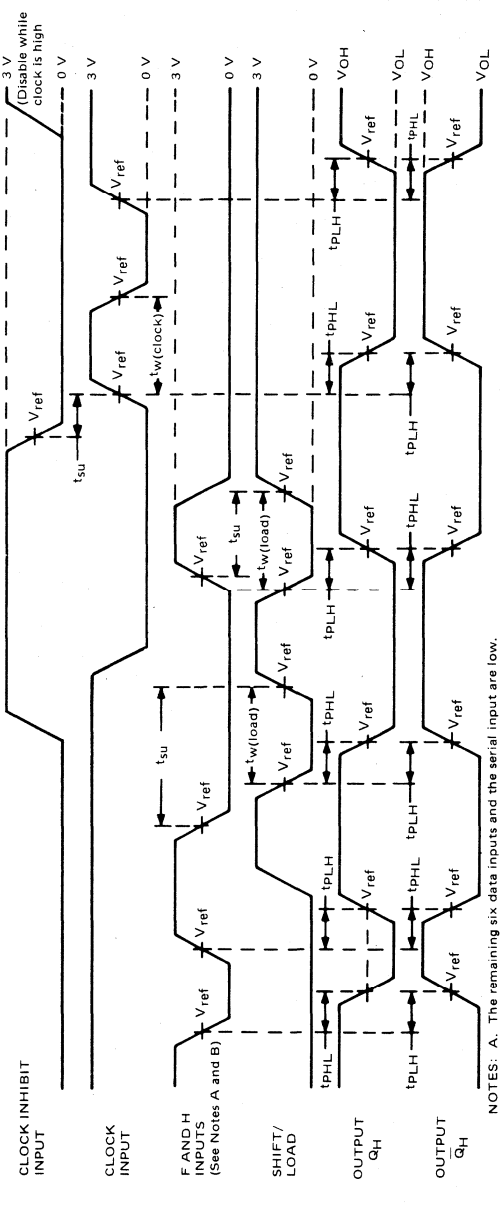
§Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See figures 1 thru 3	25	35		MHz
t_{PLH}	Load	Any			21	35	ns
t_{PHL}					26	35	
t_{PLH}	Clock	Any			14	25	ns
t_{PHL}					16	25	
t_{PLH}	H	Q_H			13	25	ns
t_{PHL}					24	30	
t_{PLH}	H	$\overline{Q}_H$			19	30	ns
t_{PHL}					17	25	

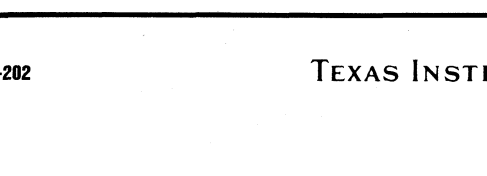
¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



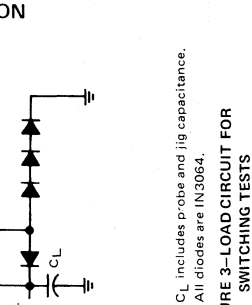
NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: PRR ⩽ 1 MHz, duty cycle ⩽ 50% $Z_{out} \approx 50\ \Omega$; for '165, $t_r \leqslant 10$ ns, $t_f \leqslant 10$ ns; for 'LS165A, $t_r \leqslant 15$ ns, $t_f \leqslant 6$ ns.
D. For '165, $V_{ref} = 1.5$ V; for 'LS165A $V_{ref} = 1.3$ V.

FIGURE 1–VOLTAGE WAVEFORMS



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: PRR ⩽ 1 MHz, duty cycle ⩽ 50%, $Z_{out} \approx 50\ \Omega$; for '165, $t_r \leqslant 10$ ns; $t_f \leqslant 10$ ns; for 'LS165A, $t_r \leqslant 15$ ns, $t_f \leqslant 6$ ns.
C. For '165, $V_{ref} = 1.5$ V; for 'LS165A, $V_{ref} = 1.3$ V.

FIGURE 2–VOLTAGE WAVEFORMS



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are IN3064.

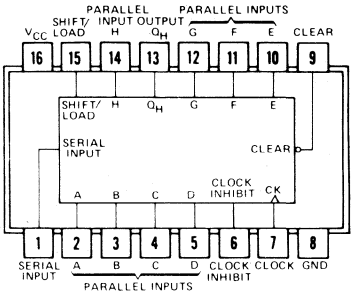
FIGURE 3–LOAD CIRCUIT FOR SWITCHING TESTS

TYPES SN54166, SN54LS166A, SN74166, SN74LS166A
8-BIT SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel to Serial Conversion

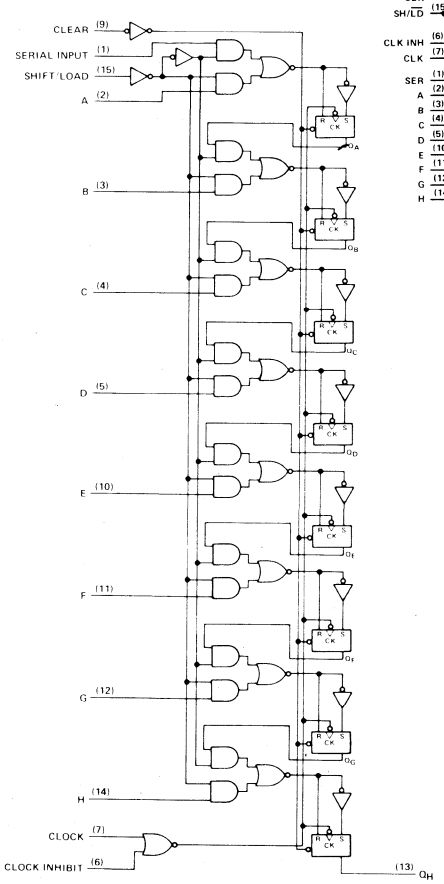
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'166	35 MHz	360 mW
'LS166A	35 MHz	110 mW

SN54166, SN54LS166A. J OR W PACKAGE
SN74166, SN74LS166A. J OR N PACKAGE
(TOP VIEW)

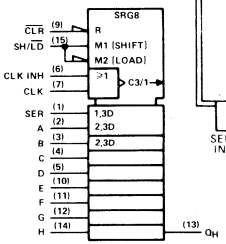


positive logic: see description

functional block diagram



logic symbol



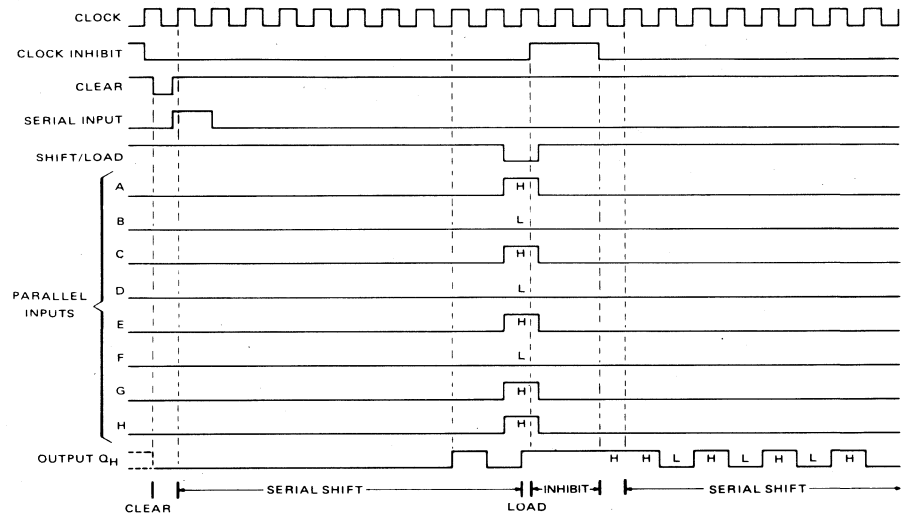
description

The '166 and 'LS166A 8-bit shift registers are compatible with most other TTL and DTL logic families. All '166 and 'LS166A inputs are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input clamping diodes minimize switching transients and simplify system design.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

. . . dynamic input activated by transition from a high level to a low level.

typical clear, shift, load, inhibit, and shift sequences



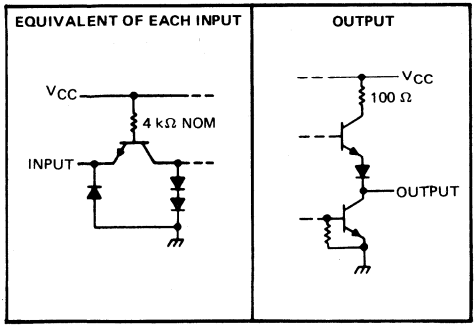
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

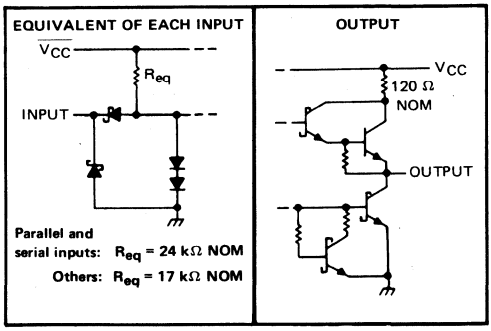
See explanation of function tables on page 3-8.

schematics of inputs and outputs

'166



'LS166 A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54166 (see Note 2) . . . . . −55°C to 125°C
SN74166 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A (See Note 2)	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54166			SN74166			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		90	127		90	127	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: An SN54166 in the W package operating at free-air temperature above 113°C requires a heat sink that provides a thermal resistance from case to free air $R_{\theta CA}$ of not more than 48°C/W.
NOTE 3: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS166A . . . . . −55°C to 125°C
SN74LS166A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS166A			SN74LS166A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

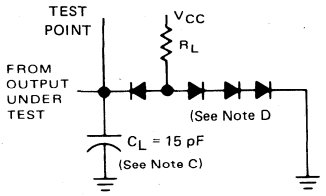
PARAMETER		TEST CONDITIONS†		SN54LS166A			SN74LS166A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			20	32		20	32	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 3: With all outputs open, 4.5 V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	14	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		5	11	20	ns

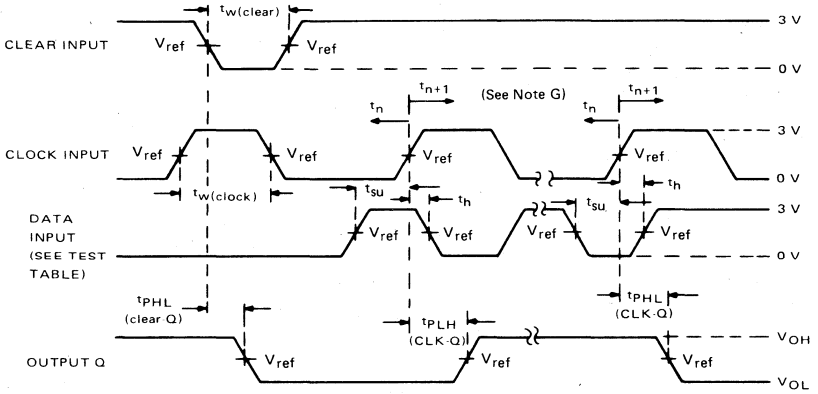
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE F)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTE: A. All pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for '166, $t_r \leq 7$ ns and $t_f \leq 7$ ns, for 'LS166A, $t_r \leq 15$ ns and $t_f \leq 6$ ns. $t_f \leq 6$ ns.

B. The clock pulse has the following characteristics: $t_{w(clock)} \leq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N3064 or 1N916.

E. A clear pulse is applied prior to each test.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

G. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

H. For '166 $V_{ref} = 1.5$ V; for 'LS166A $V_{ref} = 1.3$ V.

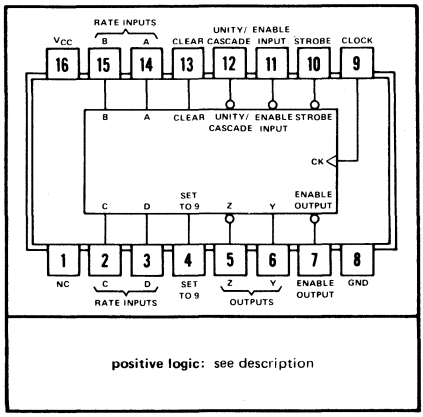
FIGURE 1

TYPES SN54167, SN74167
SYNCHRONOUS DECADE RATE MULTIPLIERS

BULLETIN NO DL-S 7211813, DECEMBER 1972

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN54167 . . . J OR W PACKAGE
SN74167 . . . J OR N PACKAGE
(TOP VIEW)



NC—No internal connection

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These decade counters feature buffered clock, clear, enable and set-to-nine inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe set-to-nine, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 10, ie.:

$$f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform two-decade rate multiplication (0-99), the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output. For longer words, see typical application data, Figure 1.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the output. These devices are completely compatible with most TTL and DTL families. Typical dissipation is 270 milliwatts. The SN54167 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74167 is characterized for operation from 0°C to 70°C.

STATE AND/OR RATE FUNCTION TABLE (See Note A)

INPUTS									OUTPUTS			
			BCD RATE						LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	H	L	L	L	10	H	8	8	1	C
L	L	L	H	L	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
D. These input conditions exceed the range of the decimal rate inputs.
E. Unity/cascade can be used to inhibit output Y.

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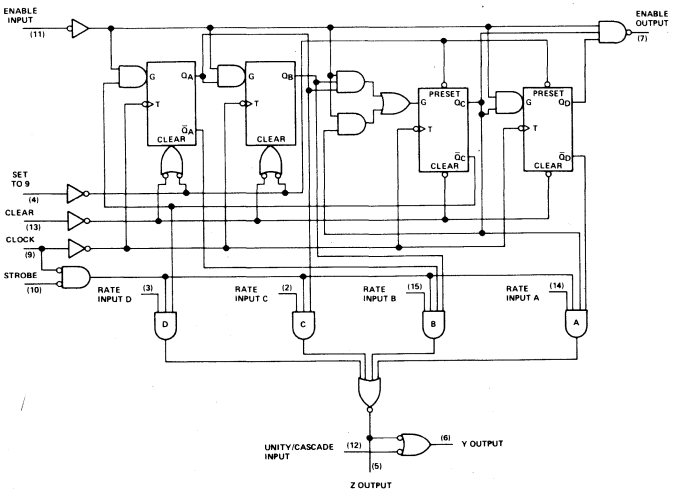
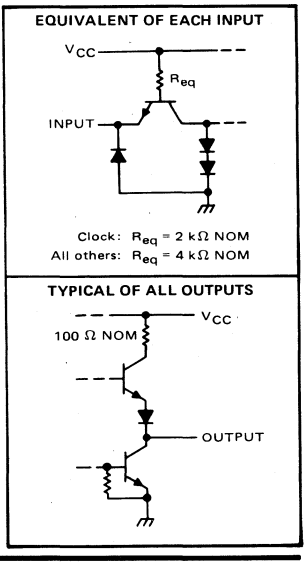
functional block diagram and schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54167 . . . . . −55°C to 125°C
SN74167 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54167			SN74167			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Width of set-to-nine pulse $t_{w(set\text{-}to\text{-}9)}$	15			15			ns
Enable setup time, t_{su}: (See Note 2)							
From positive-going transition of clock pulse	25			25			ns
From negative-going transition of previous clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
Enable hold time, t_h: (See Note 2)							
From positive-going transition of clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
From negative-going transition of previous clock pulse	20		$t_{cp}-10$	20		$t_{cp}-10$	ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 2: $t_{w(clock)}$ is the interval in which the clock is high. t_{cp} is the total clock cycle starting with a negative transition. See Figure 1 on SN5497, SN7497 data sheet.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock inputs	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, output high		V_{CC} = MAX,	See Note 3		43		mA
I_{CCL}	Supply current, output low		V_{CC} = MAX,	See Note 4		65	99	mA

NOTES: 3. I_{CCH} is measured with outputs open and all inputs low.
4. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETERS¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 5	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	$\overline{Y}$			24	36	ns
t_{PHL}		$\overline{Z}$			15	23	
t_{PHL}	Set-to-9	Enable			18	27	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶f_{max} is maximum clock frequency.
t_{PLH} is propagation delay time, low-to-high-level output.
t_{PHL} is propagation delay time, high-to-low-level output.
NOTE 5: Load circuit, voltage waveforms, and input conditions for measuring switching characteristics are the same as those for the SN5497 and SN7497.

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TYPICAL APPLICATION DATA

This application demonstrates how the decimal-rate multipliers may be cascaded for longer words. Three decades are illustrated (0.999 to 999) although longer words can be implemented by using the pattern shown. The output is decoded either from output Y with a NOR gate or from output Z with a NAND gate. Either method of decoding produces the complement of the output used.

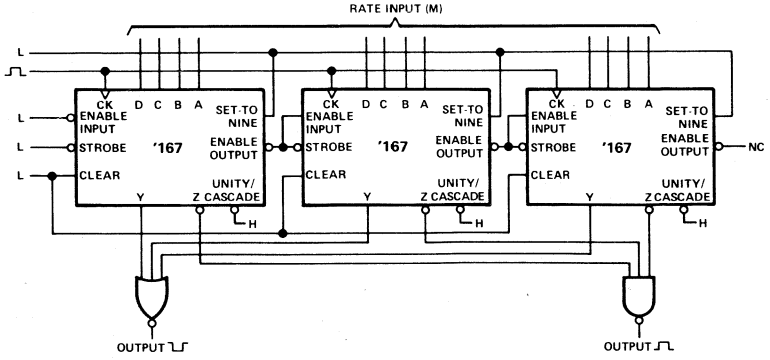


FIGURE 1

TYPES SN54LS169B, SN54S168, SN54S169
SN74LS169B, SN74S168, SN74S169
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

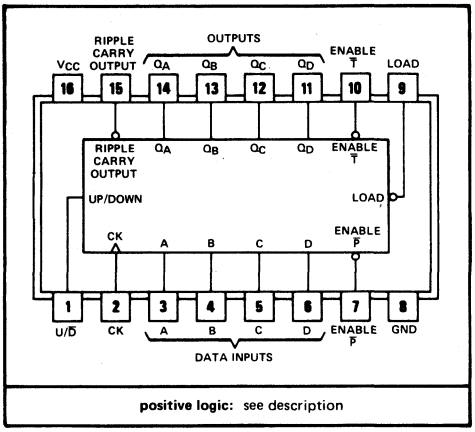
'S168 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS169B, 'S169 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS169B	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

SERIES SN54LS', SN54S' . . . J OR W PACKAGE
SERIES SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

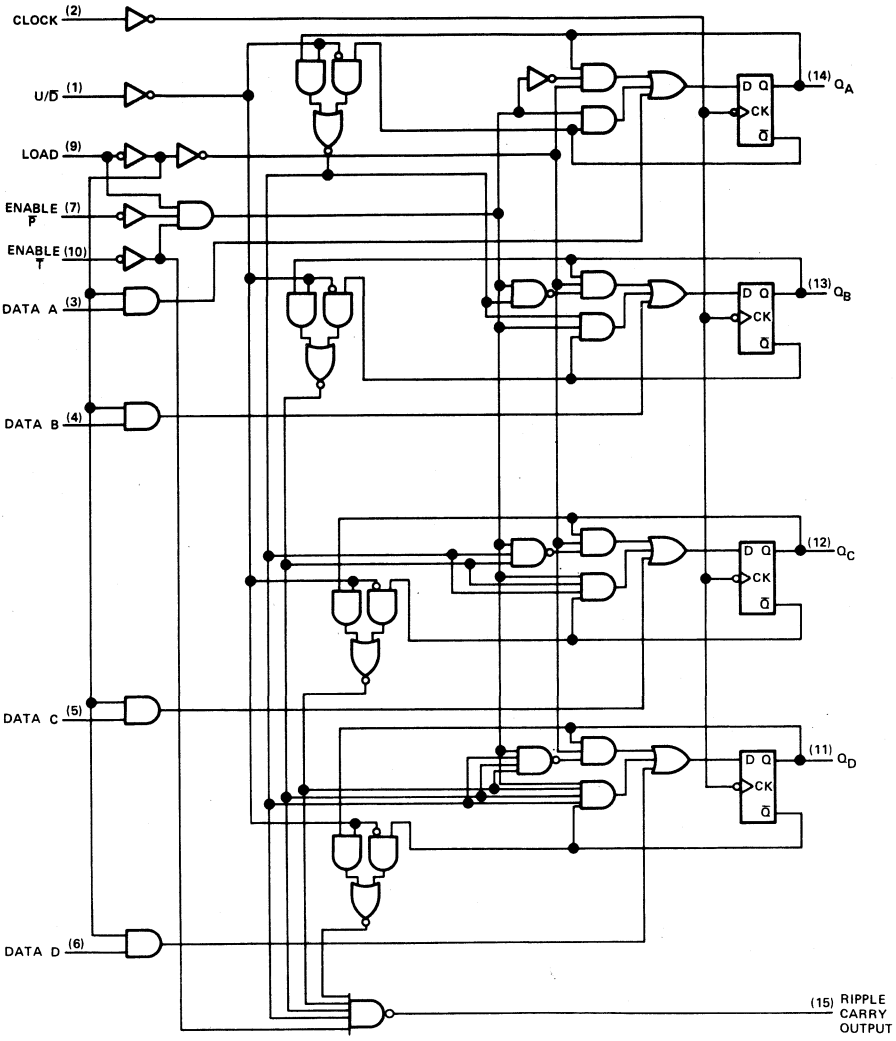
These synchronous presettable counters feature an internal carry look ahead for cascading in high-speed counting applications. The 'S168 is a decade counter and the 'LS169B and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

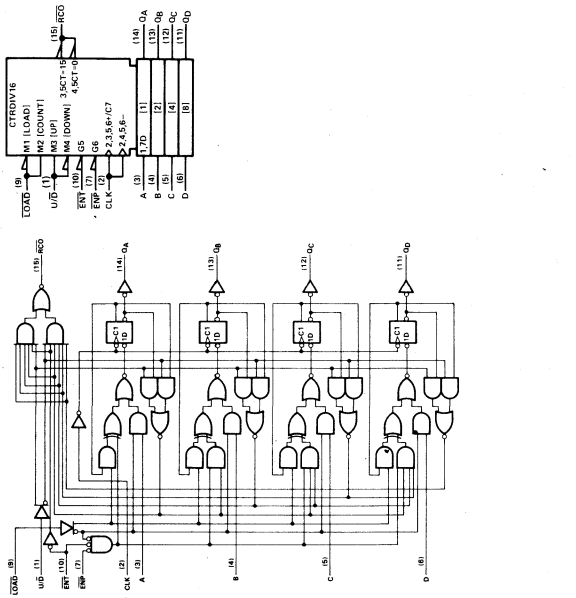
These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

functional block diagrams

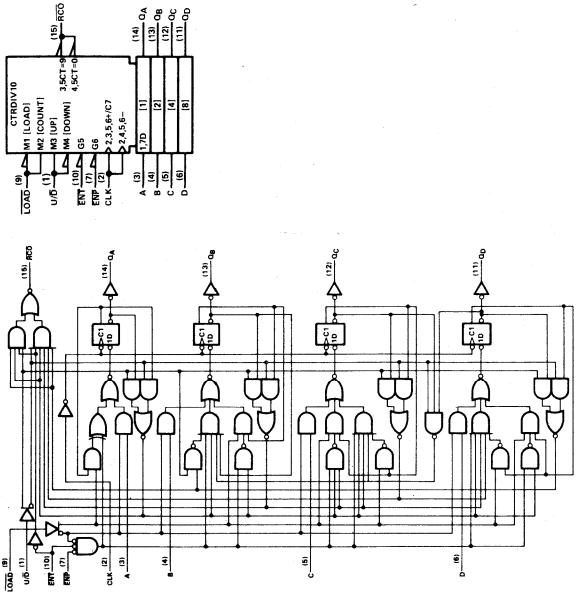


functional block diagrams

SN54S169, SN74S169 BINARY COUNTERS



SN54S168, SN74S168 DECADE COUNTERS

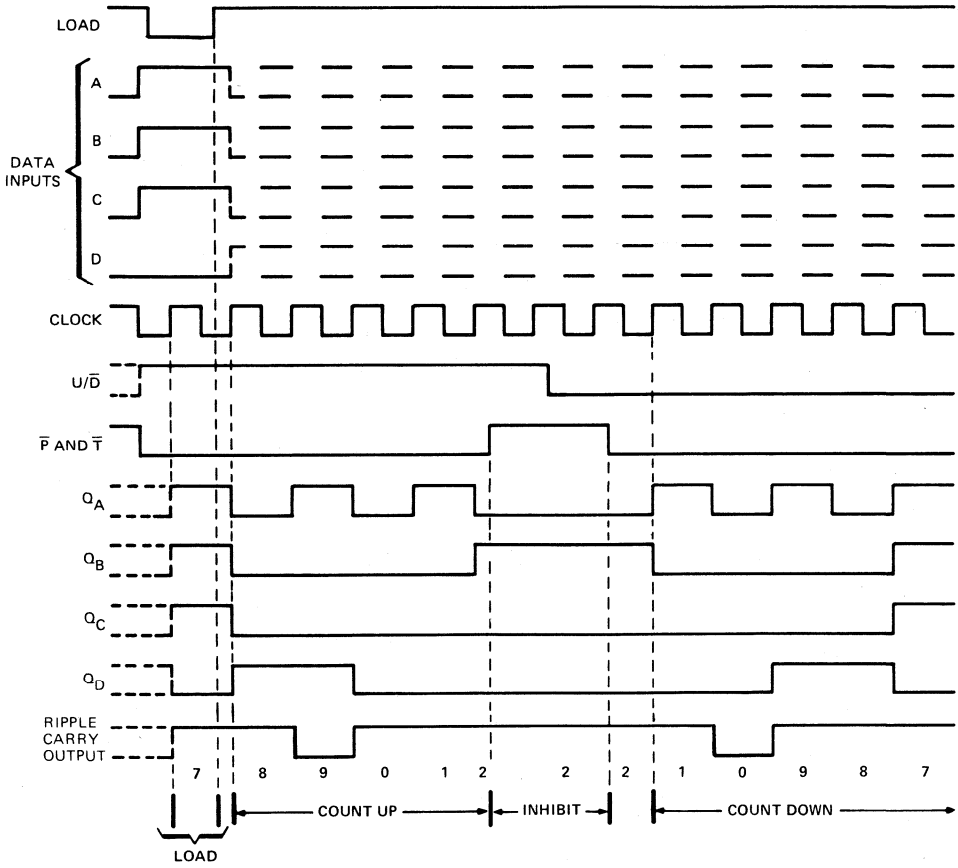


'S168 DECADE COUNTER

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven

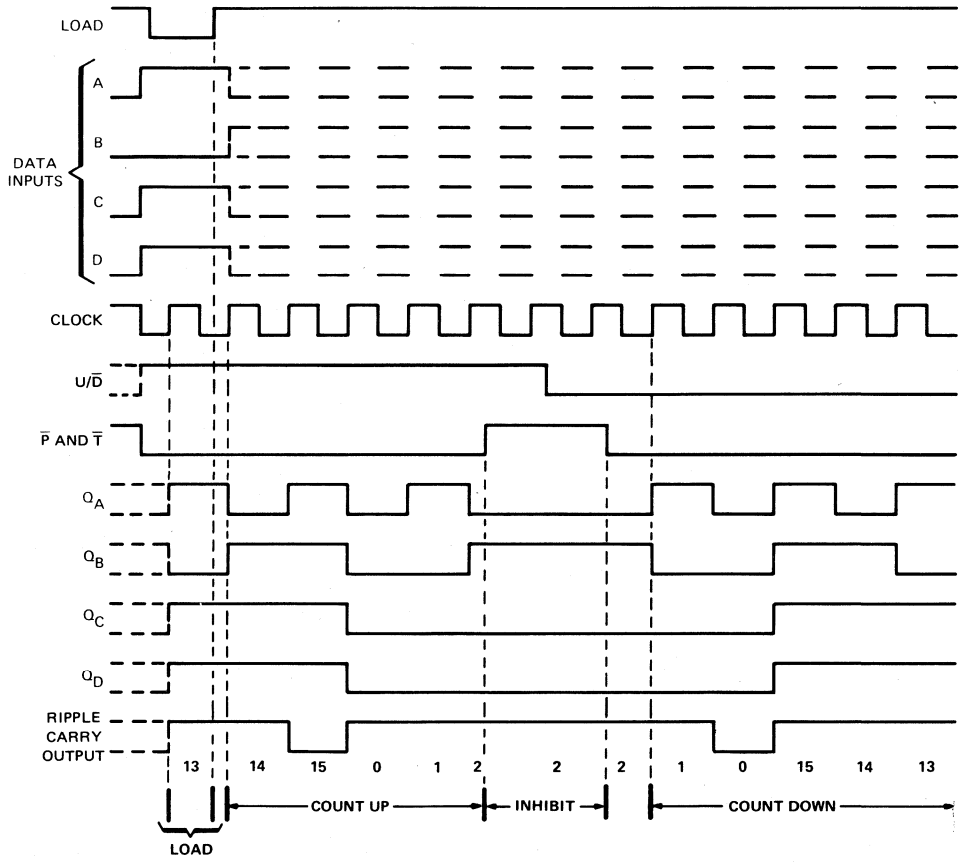


'LS169B, 'S169 BINARY COUNTERS

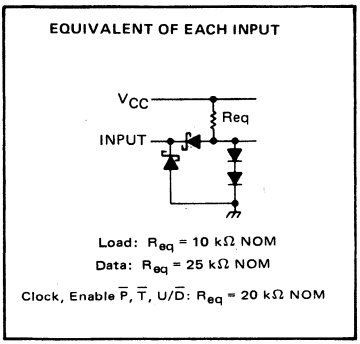
typical load, count, and inhibit sequences

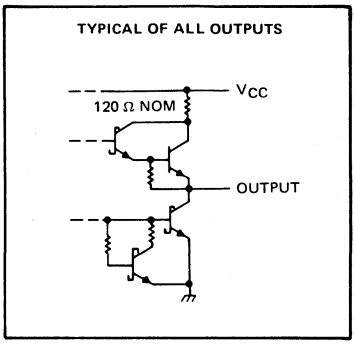
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS169B . . . . . −55°C to 125°C
SN74LS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS169B			SN74LS169B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	RCO			−400			−400	μA
	Any Q			−1.2			−1.2	mA
Low-level output current, I_{OL}	RCO			8			8	mA
	Any Q			24			24	
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low (see Figure 1)		25			25			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	30			30			ns
	Enable P̄ or T̄	30			30			
	Load	35			35			
	Up/Down	35			35			
Hold time at any input with respect to clock, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS169B			SN74LS169B			UNIT
				MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH} High-level output voltage	Ripple Carry	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		2.7	3.4		V
	Any Q	V_{IL} = V_{IL} max,	I_{OH} = −400 μA				2.4	3.2		
V_{OL} Low-level output voltage	Ripple Carry	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
V_{OL} Low-level output voltage	Any Q	V_{CC} = MIN V_{IH} = 2 V V_{IL} = V_{IL} MAX	I_{OL} = 12 mA					0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	V
I_I Input current at maximum input voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
	Clock, $\overline{T}$					0.1			0.1	
	Load					0.2			0.2	
I_{IH} High-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
	Clock, $\overline{T}$					20			20	
	Load					40			40	
I_{IL} Low-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	Clock, $\overline{T}$					−0.2			−0.2	
	Load					−0.2			−0.2	
I_{OS} Short circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX,	See Note 2		28	45		28	45	mA

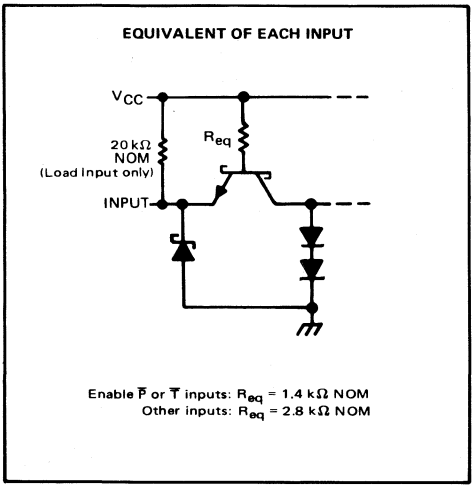
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

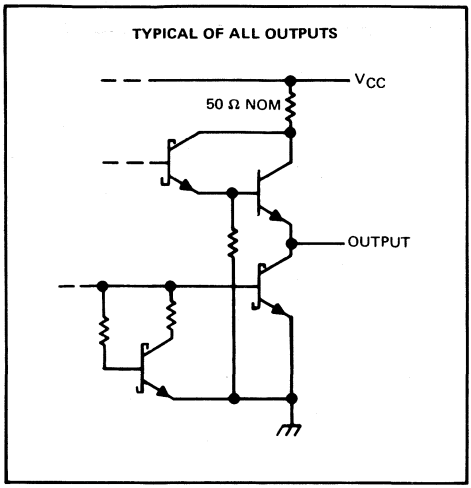
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 2 and 3 and Note 3	20	35		MHz
t_{PLH}	Clock	Ripple carry			26	40	ns
t_{PHL}					17	25	
t_{PLH}	Clock	Any Q			16	25	ns
t_{PHL}					17	25	
t_{PLH}	Enable $\overline{T}$	Ripple carry			15	25	ns
t_{PHL}					11	20	
t_{PLH}◇	Up/Down	Ripple carry			23	35	ns
t_{PHL}◇					15	25	

¶ f_{max} ≡ Maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.
NOTE 3: Load circuit is shown on page 3-11.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54S168, SN54S169 (see Note 6) . . . . . −55°C to 125°C
SN74S168, SN74S169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S168 SN54S169			SN74S168 SN74S169			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		40	0		40	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		10			10			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	4			4			ns
	Enable P̄ or T̄	14			14			
	Load	6			6			
	Up/Down	20			20			
Hold time at any input with respect to clock, t_h (see Figure 1)		1			1			ns
Operating free-air temperature, T_A (see Note 6)		−55		125	0		70	°C

NOTES: 4. Voltage values, except interemitter voltage, are with respect to network ground terminal.
5. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P̄ and T̄.
6. An SN54S168 or SN54S169 in the W package operating at free-air temperatures above 91°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 26°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S168 SN54S169			SN74S168 SN74S169			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Load input	V_{CC} = MAX, V_I = 2.7 V	−10		−200	−10		−200	μA
		Other inputs				50			50	
I_{IL}	Low-level input current	Enable $\overline{T}$	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
		Other inputs				−2			−2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply cureent		V_{CC} = MAX, See Note 2		100	160		100	160	mA
I_{IH}	High-level input current	Load	V_{CC} = MAX, V_I = 2.7 V	−10		−200	−10		−200	μA
		Enable $\overline{T}$				100			100	
		Other inputs				50			50	

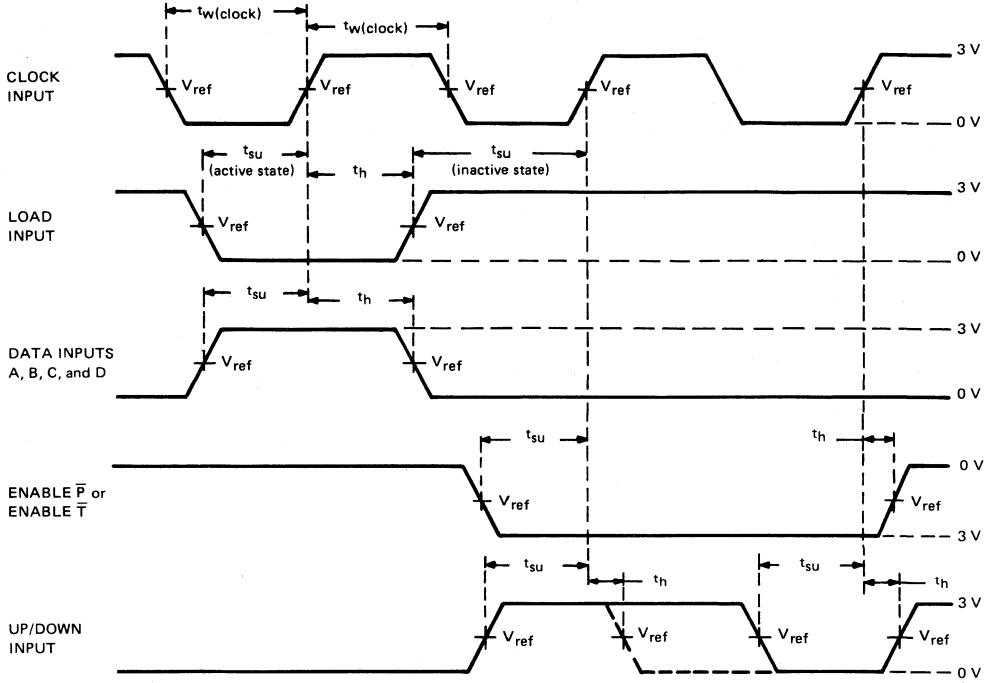
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	UP/DOWN = HIGH			UP/DOWN = LOW			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Figures 2 and 3 and Note 7	40	70		40	55		MHz
t_{PLH}	Clock	Ripple carry			14	21		14	21	ns
t_{PHL}					20	28		20	28	
t_{PLH}	Clock	Any Q			8	15		8	15	ns
t_{PHL}					11	15		11	15	
t_{PLH}	Enable $\overline{T}$	Ripple carry			7.5	11		6	12	ns
t_{PHL}					15	22		15	25	
t_{PLH}◇	Up/Down	Ripple carry			9	15		8	15	ns
t_{PHL}◇					10	15		16	22	

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
◇Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'S169), the ripple carry output will be out of phase.
NOTE 7: Load circuit is shown on page 3-10.

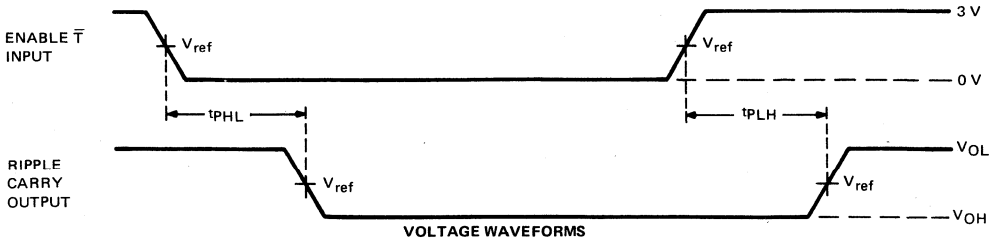
PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns, and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES

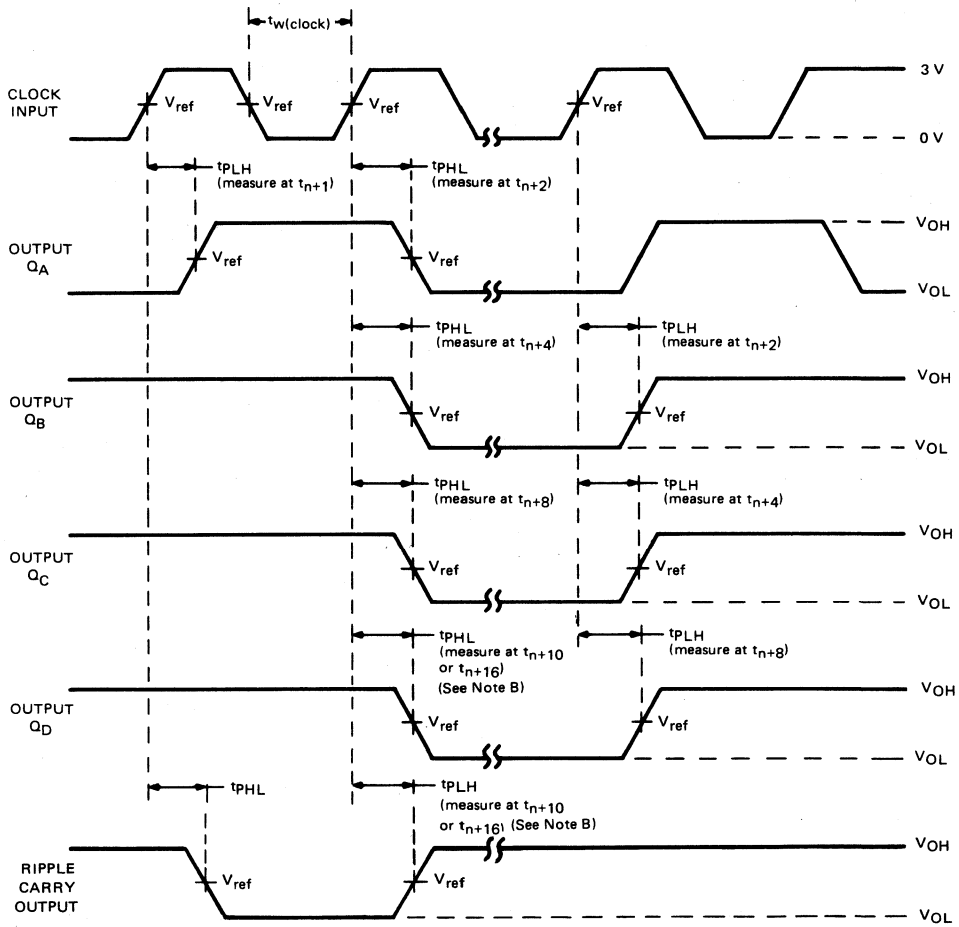


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
B. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'S168, all Q outputs high for 'LS169B and 'S169).
C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.
D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'S168 or 15 for 'LS169B and 'S169), the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for 'LS169B, $t_r \leq 15$ ns, $t_f \leq 6$ ns; and for 'S168 and 'S169, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the 'S168 and at t_{n+16} for the 'LS169B and 'S169, where t_n is the bit-time when all outputs are low.

C. For 'LS169B, $V_{ref} = 1.3$ V; for 'S168 and 'S169, $V_{ref} = 1.5$ V.

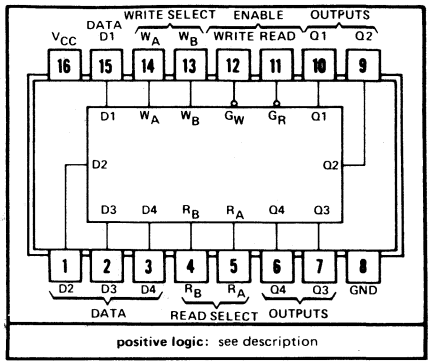
FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK

TYPES SN54170, SN54LS170, SN74170, SN74LS170
4-BY-4 REGISTER FILES WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7611349, MARCH 1974—REVISED OCTOBER 1976

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:
  Scratch-Pad Memory
  Buffer Storage between Processors
  Bit Storage in Fast Multiplication Designs
- Open-Collector Outputs with Low Maximum Off-State Current:
  '170 . . . 30 μA
  'LS170 . . . 20 μA
- SN54LS670 and SN74LS670 Are Similar But Have 3-State Outputs

SN54170, SN54LS170 . . . J OR W PACKAGE
SN74170, SN74LS170 . . . J OR N PACKAGE
(TOP VIEW)



description

The '170 and 'LS170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (30 nanoseconds typical) and the read time (25 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All '170 inputs and all inputs except the read enable and write enable of the 'LS170 are buffered to lower the drive requirements to one Series 54/74 or Series 54LS/74LS standard load, respectively. Input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54170 and SN54LS170 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 and SN74LS170 are characterized for operation from 0°C to 70°C.

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

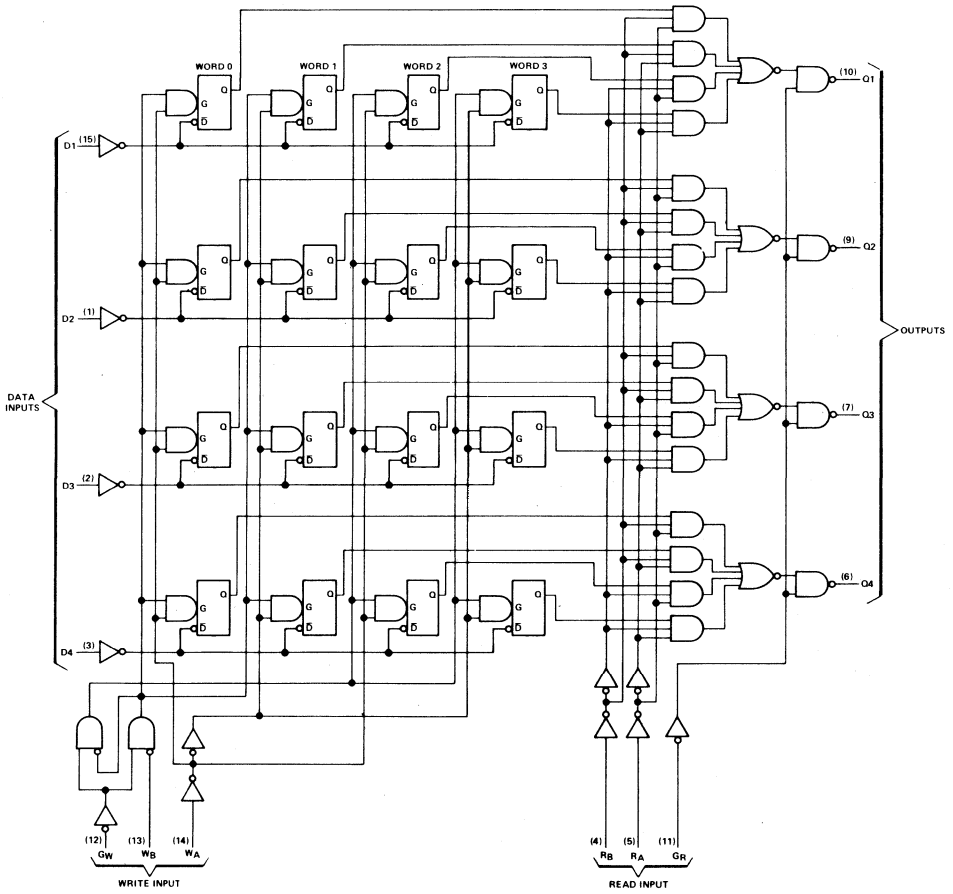
READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

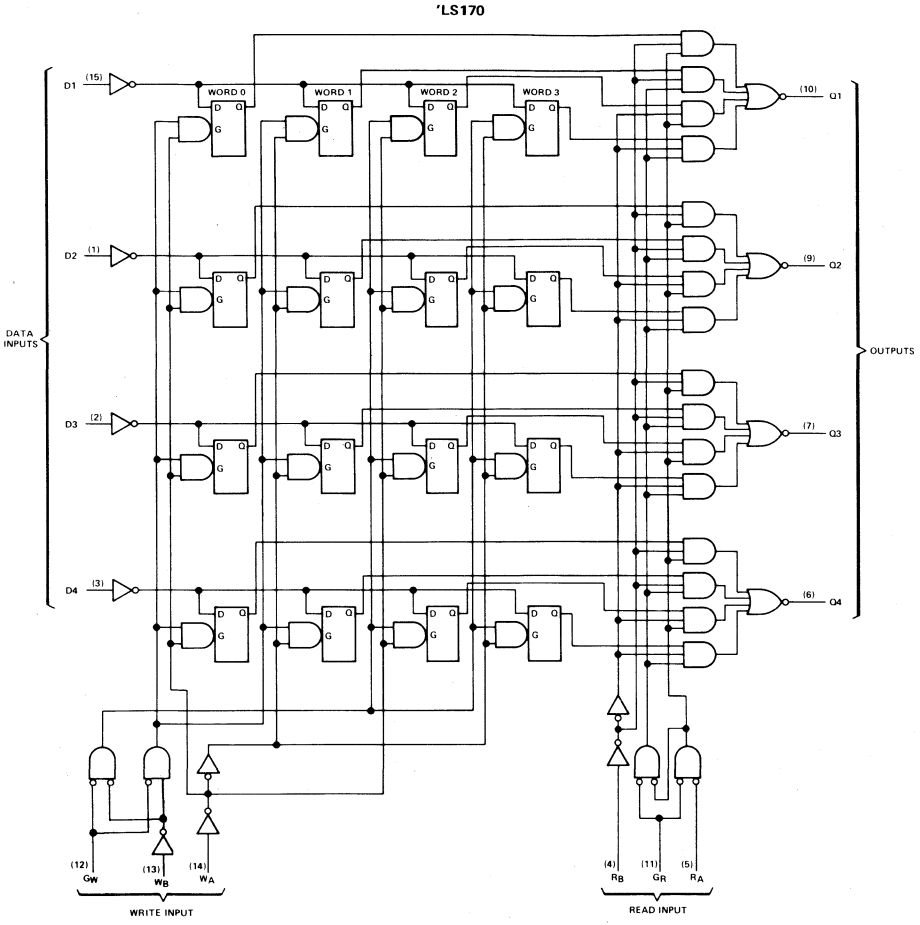
functional block diagram

'170



functional block diagram

'LS170



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: '170	5.5 V
'LS170	7 V
Off-state output voltage: '170	5.5 V
'LS170	7 V
Operating free-air temperature range: SN54170, SN54LS170 (see Note 2)	−55°C to 125°C
SN74170, SN74LS170	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A (see Note 2)		−55		125	0		70	°C

NOTES: 2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W.

3. Write select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V				30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 5	SN54170		127§	140	mA
			SN74170		127§	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Typical supply current shown is an average for 50% duty cycle.
NOTE 5: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

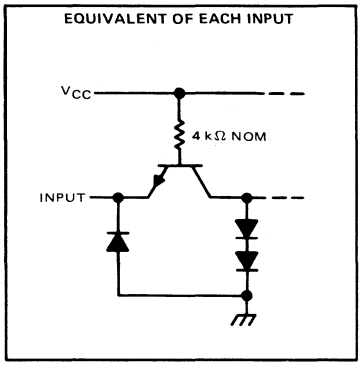
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2		10	15	ns
t_{PHL}					20	30	
t_{PLH}	Read Select	Any Q			23	35	ns
t_{PHL}					30	40	
t_{PLH}	Write enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 3		25	40	ns
t_{PHL}					34	45	
t_{PLH}	Data	Any Q			20	30	ns
t_{PHL}					30	45	

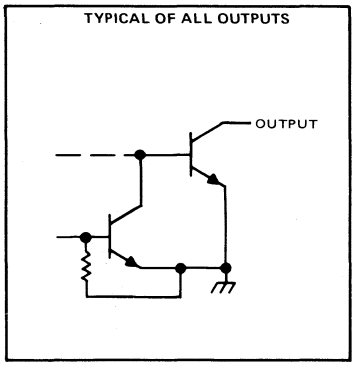
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs

'170



'170



7

recommended operating conditions

		SN54LS170			SN74LS170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{su(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

4. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS170			SN74LS170			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{OH} = 5.5 V, V_{IH} = 2 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any D, R, or W	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		G_R or G_W					0.2			0.2	
I_{IH}	High-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		G_R or G_W					40			40	
I_{IL}	Low-level input current	Any D, R, or W	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		G_R or G_W					−0.8			−0.8	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 6		25	40		25	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 6: I_{CC} is measured under the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

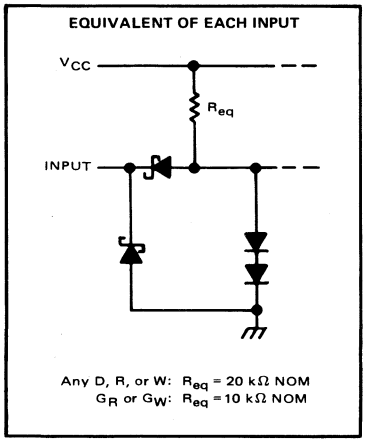
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Read select	Any Q			25	40	ns
t_{PHL}					24	40	
t_{PLH}	Write enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 3		30	45	ns
t_{PHL}					26	40	
t_{PLH}	Data	Any Q			30	45	ns
t_{PHL}					22	35	

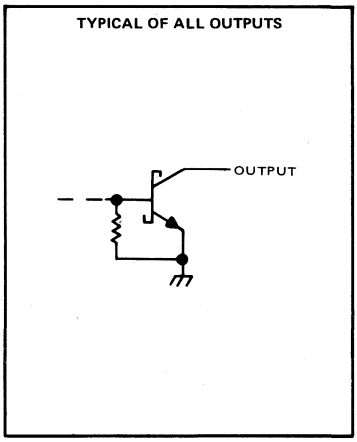
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs

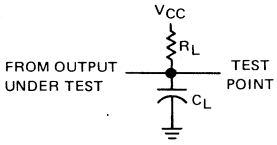
'LS170



'LS170



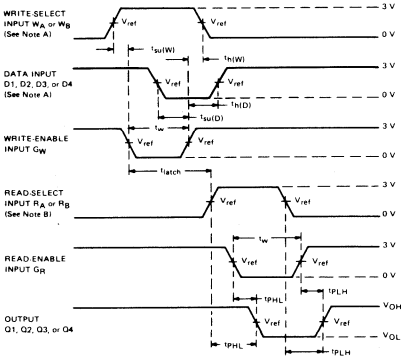
PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance

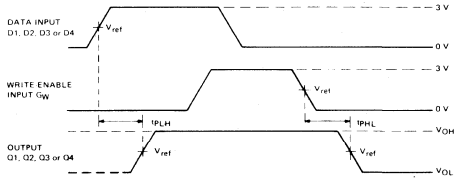
LOAD CIRCUIT

FIGURE 1

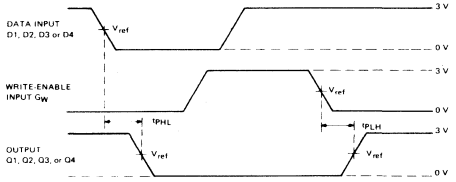


VOLTAGE WAVEFORMS

FIGURE 2



VOLTAGE WAVEFORM 1



VOLTAGE WAVEFORM 2

FIGURE 3

NOTES: A. High-level input pulses at the select and data inputs are illustrated in Figure 2; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. In Figure 3, each select address is tested. Prior to the start of each of the above tests, both write and read address inputs are stablized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.

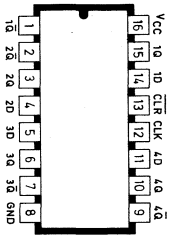
D. Input waveforms are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ⩽ 50%, t_r ⩽ 10 ns and t_f ⩽ 10 ns for '170, and t_r ⩽ 15 ns and t_f ⩽ 6 ns for 'LS170.

D. For '170, V_{ref} = 1.5 V; for 'LS170, V_{ref} = 1.3 V.

TYPES SN54LS171, SN74LS171
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

- **Contains Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Clear Inputs**
- **Individual Data Inputs to Each Flip-Flop**

SN54LS171 . . . J OR W PACKAGE
SN74LS171 . . . J OR N PACKAGE
(TO VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize the latest low-power Schottky circuitry to implement D-type flip-flop logic. They have a direct clear input and complementary outputs from each flip-flop.

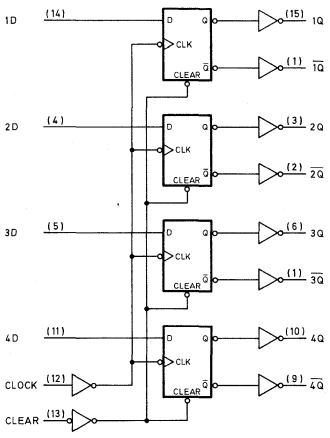
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE
(EACH FLIP-FLOP)

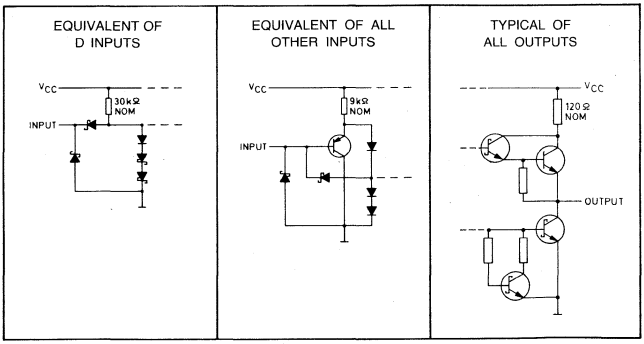
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = HIGH LEVEL (STEADY STATE)
L = LOW LEVEL (STEADY STATE)
X = IRRELEVENT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
Q_0 = THE LEVEL OF Q BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED.

functional block diagram



Schematics of inputs and outputs



Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS171			SN74LS171			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL} max	I_{OL} = 8 mA					0.35	0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	D inputs	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−0.2			−0.2	mA
I_{OS}	Short-circuit output current*		V_{CC} = MAX,	V_O = 0 V	−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs grounded, all outputs open			14	25		14	25	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, TA = 25°C.
* Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

Switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS171			UNIT
				MIN	TYP	MAX	
f max	CLK	Q, $\overline{Q}$	RL = 2 kΩ, CL = 15 pF	20	30		MHz
t_{PLH}	CLK	Q, $\overline{Q}$			15	25	ns
t_{PHL}	CLK	Q, $\overline{Q}$			18	30	ns
t_{PLH}	$\overline{CLR}$	$\overline{Q}$			18	30	ns
t_{PHL}	$\overline{CLR}$	Q			24	40	ns

recommended operating conditions

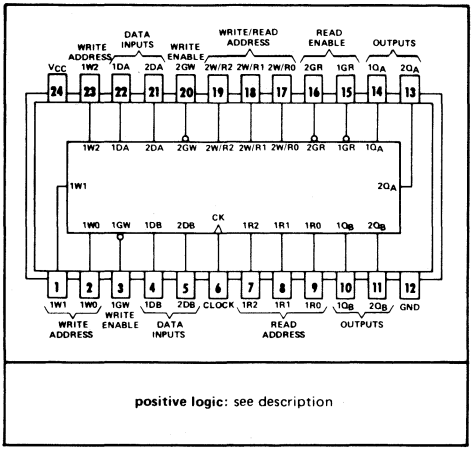
		SN54LS171			SN74LS171			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−.4			−1	mA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

TYPE SN74172
16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211744, MAY 1972 – REVISED DECEMBER 1972

- Independent Read/Write Addressing Permits Simultaneous Reading and Writing
- Organized as Eight Words of Two Bits Each
- Fast Access Times:
  From Read Enable . . . 15 ns Typical
  From Read Select . . . 33 ns Typical
- Three-State Outputs Simplify Use in Bus-Organized Systems
- Applications:
  Stacked Data Registers
  Scratch-Pad Memory
  Buffer Storage Between Processors
  Fast Multiplication Schemes

J, N OR NT DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see description

description

The SN74172, containing the equivalent of 201 gates on a monolithic chip, is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure A).

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits
2) Reading from two bits
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

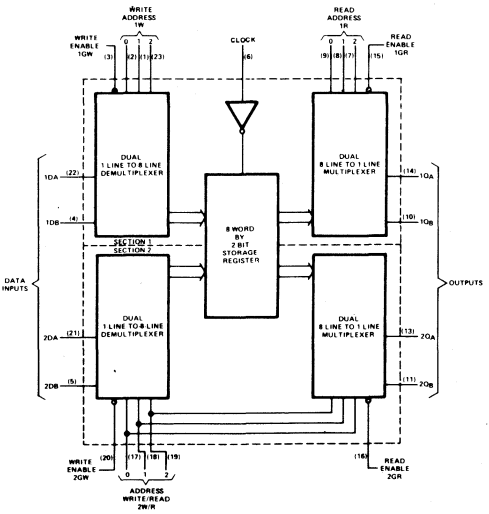


FIGURE A

description (continued)

The three-state outputs of this register file permit connection of up to 129 compatible outputs and one Series 54/74 high-logic-level load to a common system bus. The outputs are controlled by the read-enable circuitry so that they operate as standard TTL totem-pole outputs when the appropriate read-enable input is low or they are placed in a high-impedance state when the associated read-enable input is at a high logic level. To minimize the possibility that two outputs from separate register files will attempt to take a common bus to opposite logic levels, the read-enable circuitry is designed such that disable times are shorter than enable times.

All inputs are buffered to lower the drive requirements of the clock, read/write address, and write-enable inputs to one normalized Series 54/74 load, and of all other inputs to one-half of one normalized Series 54/74 load.

Functions of the inputs and outputs of the SN74172 are as shown in the following table.

FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA $\neq$ 2DA and/or 1DB $\neq$ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the high-impedance state.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}				−5.2	mA
Low-level output current, I_{OL}				16	mA
Clock frequency, f_{clock}		0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			ns
Setup time, t_{su} (see Figure 1)	Write select	$t_{w(clock)}+10$			ns
	High-level data	30			
	Low-level data	45			
	Write enable	35			
Hold time, t_h (see Figure 1)	Write select	0			ns
	Write enable	0			
Data release time, $t_{release}$ (see Figure 1)	High-level data			10	ns
	Low-level data			10	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

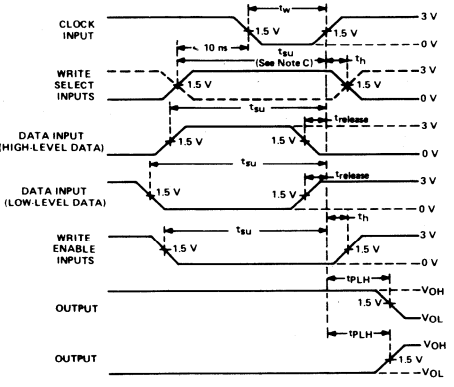
PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −5.2 mA	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 2.4 V			40	μA
			V_{CC} = MAX, V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	2W/R0, 2W/R1, 2W/R2, 1GW, 2GW, or clock	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		Any other input				−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 4.5 V, Outputs open		112	170	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

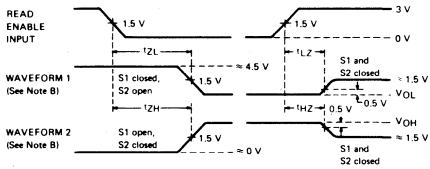
switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, See Figure 1	20			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from read select			33	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output from read select			30	45	
t_{PLH}	Propagation delay time, low-to-high-level output from clock			35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			35	50	
t_{ZH}	Output enable time to high level			14	30	ns
t_{ZL}	Output enable time to low level			16	30	
t_{HZ}	Output disable time from high level	C_L = 5 pF, See Figure 1		6	20	ns
t_{LZ}	Output disable time from low level			11	20	

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES FROM CLOCK INPUT



ENABLE AND DISABLE TIMES FROM READ ENABLE

NOTES: A. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled. Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

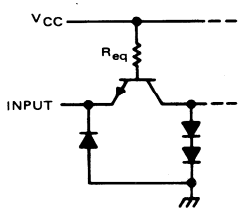
C. Write select setup time, as specified, will protect data written into previous address.

D. Load circuit is shown on page 3-10.

VOLTAGE WAVEFORMS
FIGURE 1

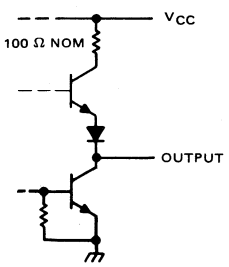
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



2W/R0, 2W/R1, 2W/R2,
1GW, 2GW, or Clock: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



TYPES SN54173, SN54LS173A, SN74173, SN74LS173A
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 11721, OCTOBER 1976—REVISED JANUARY 1981

- Three-State Outputs Interface Directly with System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:

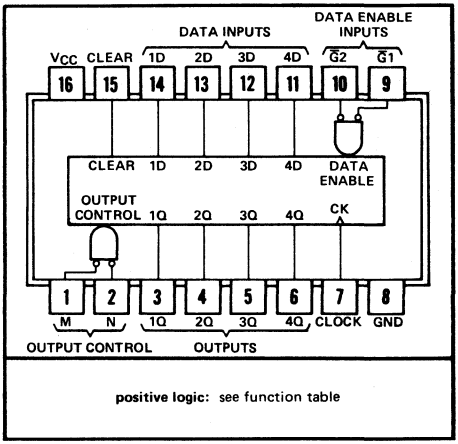
  Parallel Load
  Do Nothing (Hold)

- For Application as Bus Buffer Registers

TYPE	TYPICAL PROPAGATION DELAY TIME	MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'173	23 ns	35 MHz	250 mW
'LS173A	18 ns	50 MHz	95 mW

SN54173, SN54LS173A . . . J OR W PACKAGE
SN74173, SN74LS173A . . . J OR N PACKAGE

(TOP VIEW)



positive logic: see function table

description

The '173 and 'LS173A four-bit registers include D-type flip-flops featuring totem-pole three-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. Up to 128 of the SN74173 or SN74LS173A outputs may be connnected to a common bus and still drive two Series 54/74 or 54LS/74LS TTL normalized loads, respectively. Similarly, up to 49 of the SN54173 or SN54LS173A outputs can be connected to a common bus and drive one additional Series 54/74 or 54LS/74LS TTL normalized load, respectively. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE $\overline{G1}$	DATA ENABLE $\overline{G2}$	DATA D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

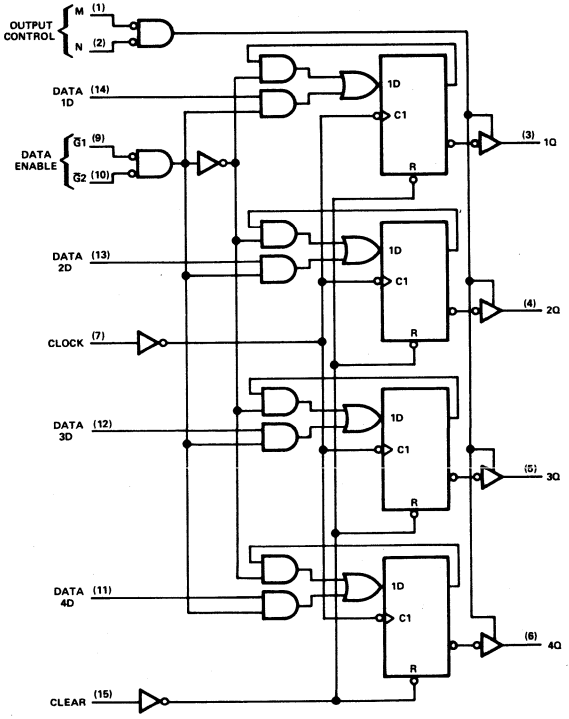
Gated enable inputs are provided on these devices for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

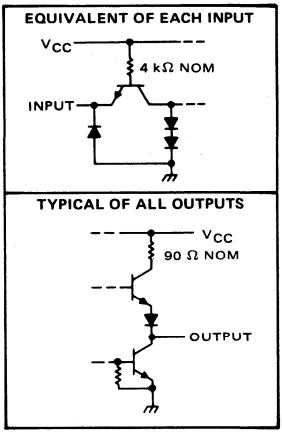
Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: '173		5.5 V
'LS173A		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54173, SN54LS173A	−55°C to 125°C
	SN74173, SN74LS173A	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

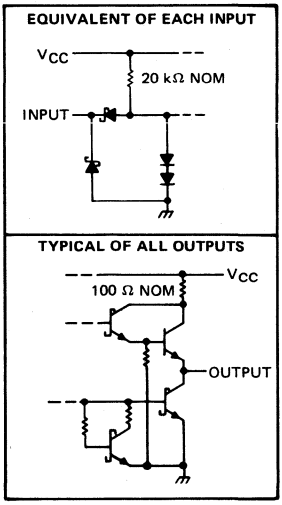
functional block diagram and schematics of inputs and outputs



'173



'LS173A



recommended operating conditions

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−5.2	mA
Low-level output current, I_{OL}				16			16	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data enable	35			35			ns
	Data	10			10			
	Clear inactive state	10			10			
Hold time, t_h	Data enable	2			2			ns
	Data	10			10			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			40	μA
			V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−70	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			50	72	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, See Note 3	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			28	43	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			19	31	
t_{PZH}	Output enable time to high level		7	16	30	ns
t_{PZL}	Output enable time to low level		7	21	30	
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Note 3	3	5	14	ns
t_{PLZ}	Output disable time from low level		3	11	20	

NOTE 3: Load circuits and voltage waveforms are shown on page 3-10.

recommended operating conditions

		SN54LS173A			SN74LS173A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Input clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data enable	35			35			ns
	Data	17			17			
	Clear inactive state	10			10			
Hold time, t_h	Data enable	0			0			ns
	Data	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS173A			SN74LS173A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = 0.8 V	I_{OL} = 24 mA					0.35	0.5	
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
		V_{IH} = 2 V	V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		19	30		19	24	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 45 pF, See Note 3	30	50		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			26	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			22	30	
t_{PZH}	Output enable time to high level			15	23	ns
t_{PZL}	Output enable time to low level			18	27	
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Note 3		11	17	ns
t_{PLZ}	Output disable time from low level			11	17	

NOTE 3: Load circuits and voltage waveforms are shown on page 3-11.

TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175 HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

BULLETIN NO. DL-S 7611803, DECEMBER 1972—REVISED OCTOBER 1976

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

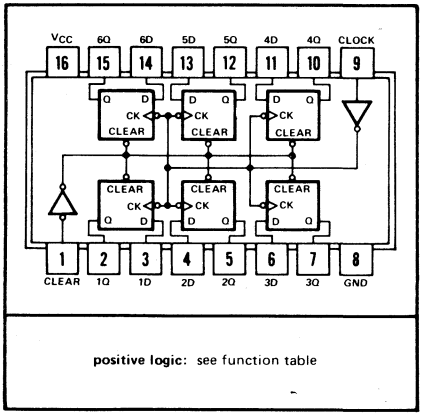
These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

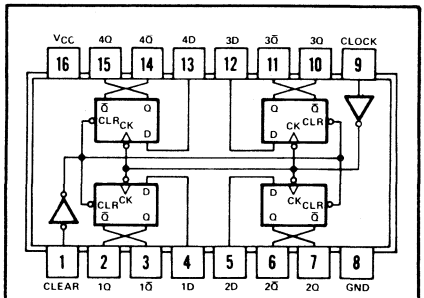
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174, SN74LS174, SN74S174 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
(TOP VIEW)

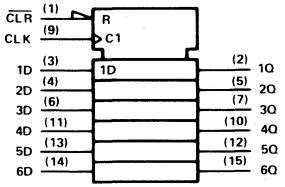


positive logic: see function table

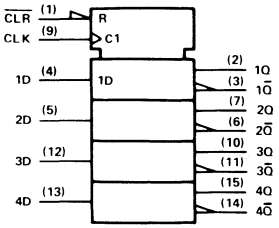
TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

logic symbols

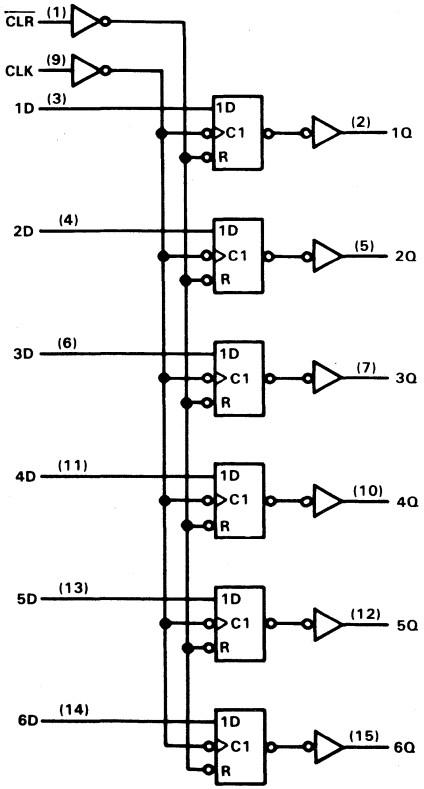
'174, 'LS174, 'S174

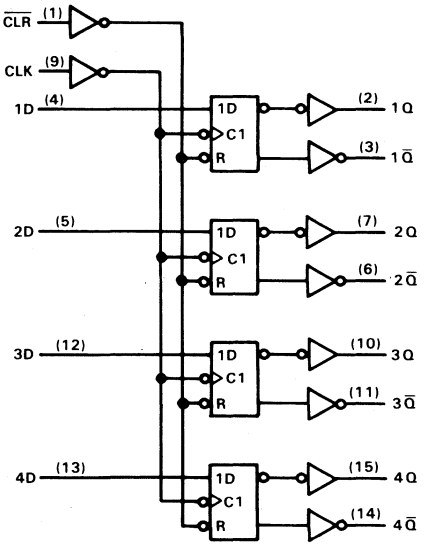


'175, 'LS175, 'S175



logic diagrams (positive logic)



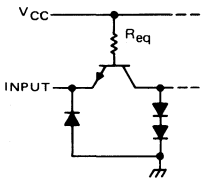


7

schematics of inputs and outputs

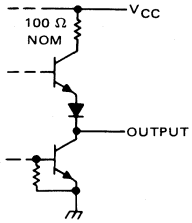
SN54174, SN54175, SN74174, SN74175

EQUIVALENT OF ALL INPUTS



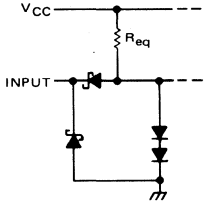
Clock, D: R_{eq} = 8 kΩ NOM
Clear: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



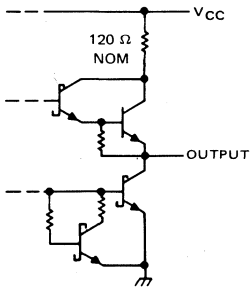
SN54LS174, SN54LS175, SN74LS174, SN74LS175

EQUIVALENT OF ALL INPUTS



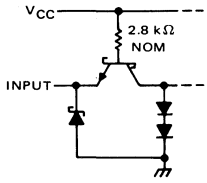
Clock: R_{eq} = 17 kΩ NOM
Clear, D: R_{eq} = 20 kΩ NOM

TYPICAL OF ALL OUTPUTS

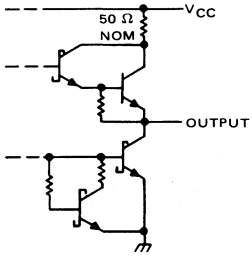


SN54S174, SN54S175, SN74S174, SN74S175

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S174, SN54S175 Circuits . . . . . −55°C to 125°C
SN74S174, SN74S175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S174, SN54S175			SN74S174, SN74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		75	0		75	MHz
Pulse width, t_w	Clock	7			7			ns
	Clear	10			10			
Setup time, t_{su}	Data input	5			5			ns
	Clear inactive-state	5			5			
Data hold time, t_h		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		90	144	mA
			'175		60	96	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 3	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output from clear (SN54S175, SN74S175 only)			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation time, high-to-low-level output from clock			11.5	17	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

REVISED DECEMBER 1980

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS174, SN54LS175 Circuits . . . . . −55°C to 125°C
SN74LS174, SN74LS175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'LS174		16	26		16	26	mA
			'LS175		11	18		11	18	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	'LS174			'LS175			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max} Maximum clock frequency	C_L = 15pF, R_L = 2kΩ, See Note 4	30	40		30	40		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clear						20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear			23	35		20	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			20	30		13	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	30		16	25	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54174, SN54175 Circuits . . . . . −55°C to 125°C
SN74174, SN74175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54174, SN54175			SN74174, SN74175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	mA
			SN74'	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		45	65	mA
			'175		30	45	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	25	35		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			24	35	ns

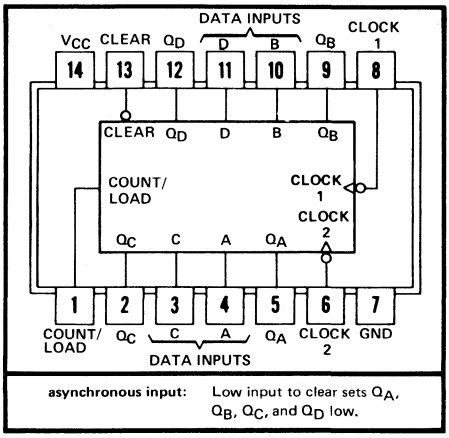
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

BULLETIN NO. DL-S 7211478, MAY 1971—REVISED DECEMBER 1972

- Reduced-Power Versions of SN54196, SN54197, SN74196, and SN74197 50-MHz Counters
- D-C Coupled Counters Designed to Replace Signetics 8280, 8281, 8290, and 8291 Counters in Most Applications
- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 35 MHz
- Input Clamping Diodes Simplify System Design

SN54176, SN54177 . . . J OR W PACKAGE
SN74176, SN74177 . . . J OR N PACKAGE
(TOP VIEW)



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

description

These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54176, SN74176) or a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 150 milliwatts. The SN54176 and SN54177 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74176 and SN74177 circuits are characterized for operation from 0°C to 70°C.

typical count configurations

SN54176 and SN74176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.

SN54176, SN74176
FUNCTION TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54177 and SN74177

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the function table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

SN54177, SN74177
FUNCTION TABLE
(See Note A)

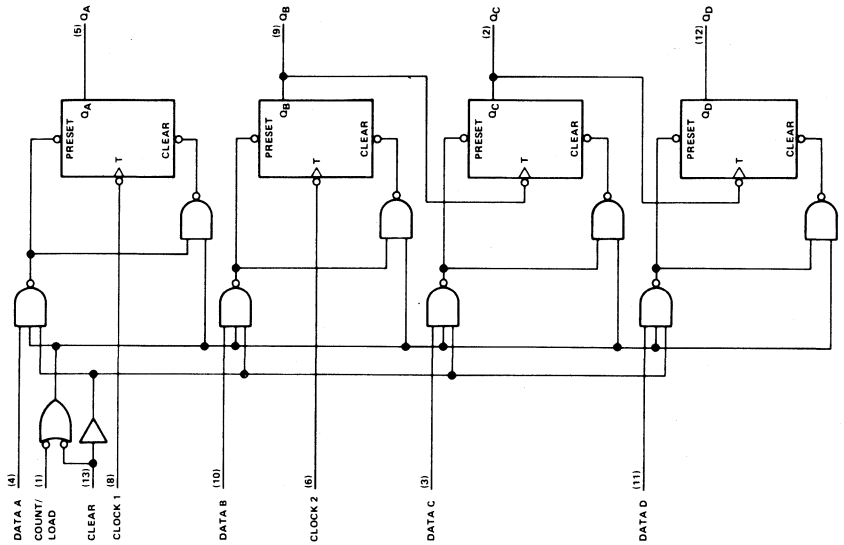
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level

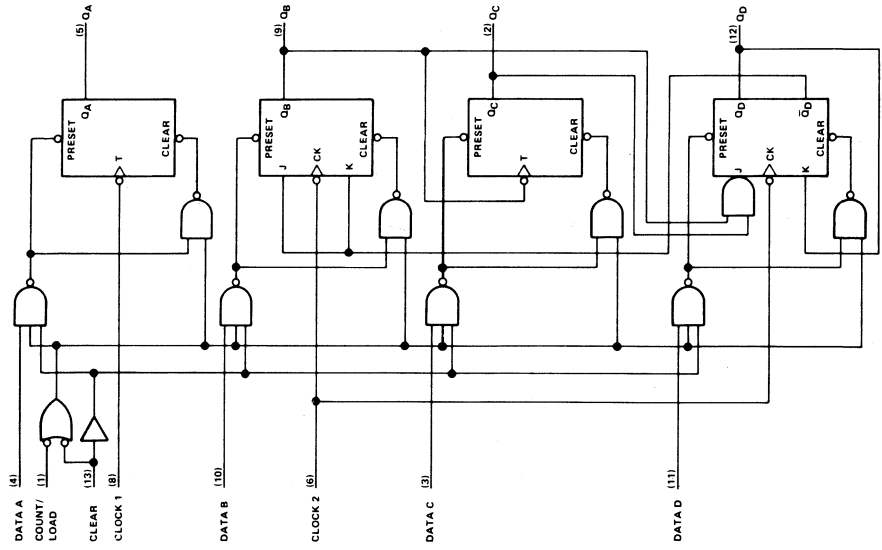
NOTE A: Output Q_A connected to clock-2 input.

functional block diagrams

SN54177, SN74177



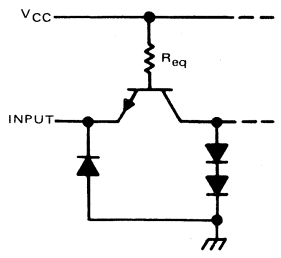
SN54176, SN74176



. . . dynamic input activated by transition from a high level to a low level

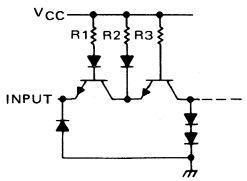
schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS



Data, Count/load: R_{eq} = 4 kΩ NOM
Clear: R_{eq} = 2 kΩ NOM

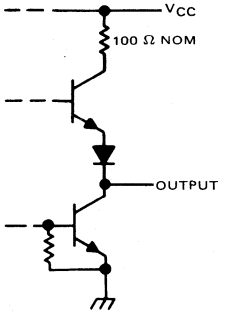
EQUIVALENT OF CLOCK INPUTS



NOMINAL VALUES OF R1, R2, and R3

INPUT	'176	'177
Clock 1	4 kΩ	4 kΩ
Clock 2	4 kΩ	6 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54176, SN54177 Circuits . . . . . −55°C to 125°C
SN74176, SN74177 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54'	4.5	5	5.5	V
	SN74'	4.75	5	5.25	
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Count frequency (see Figure 1)	Clock-1 input	0		35	MHz
	Clock-2 input	0		17.5	
Pulse width, t_w (see Figure 1)	Clock-1 input	14			ns
	Clock-2 input	28			
	Clear	20			
	Load	25			
Input hold time, t_h (see Figure 1)	High-level data	$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			
Input setup time, t_{su} (see Figure 1)	High-level data	15			ns
	Low-level data	20			
Count enable time, t_{enable} (see Note 3 and Figure 1)		25			ns
Operating free-air temperature, T_A	SN54'	−55		125	°C
	SN74'	0		70	

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54176, SN74176			SN54177, SN74177			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Clear, clock 1					80			80	
		Clock 2					120			80	
I_{IL}	Low-level input current	Data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Clear					−3.2			−3.2	
		Clock 1					−4.8			−4.8	
		Clock 2					−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			30	48		30	48	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, see figure 1

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	SN54176, SN74176			SN54177, SN74177			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	35	50		35	50		MHz
t_{PLH}	Clock 1	Q_A		8	13		8	13	ns
t_{PHL}				11	17		11	17	
t_{PLH}	Clock 2	Q_B		11	17		11	17	ns
t_{PHL}				17	26		17	26	
t_{PLH}	Clock 2	Q_C		27	41		27	41	ns
t_{PHL}				34	51		34	51	
t_{PLH}	Clock 2	Q_D		13	20		44	66	ns
t_{PHL}				17	26		50	75	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		19	29		19	29	ns
t_{PHL}				31	46		31	46	
t_{PLH}	Load	Any		29	43		29	43	ns
t_{PHL}				32	48		32	48	
t_{PHL}	Clear	Any		32	48		32	48	ns

◇f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

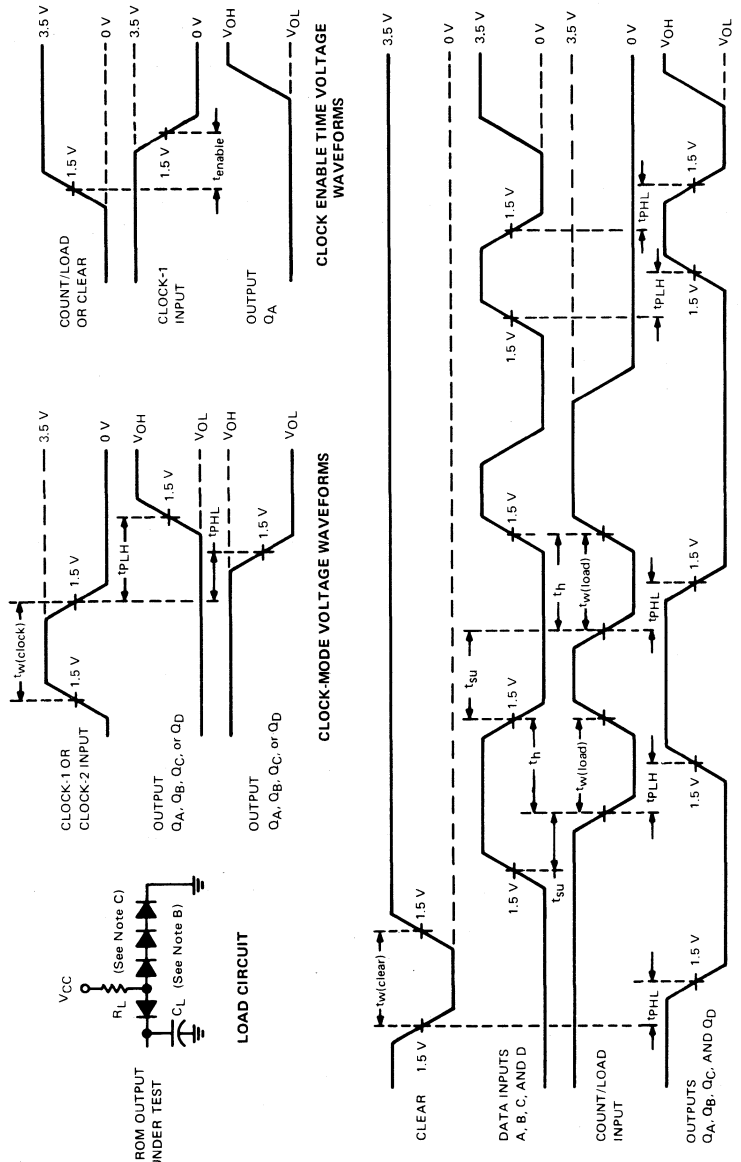


FIGURE 1

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $t_r < 5$ ns, and unless specified, $t_f < 5$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Unless otherwise specified, Q_A is connected to clock 2.

7

TYPES SN54178, SN54179, SN74178, SN74179
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7211846, DECEMBER 1972

- Typical Maximum Clock Frequency . . . 39 MHz
- Three Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Hold (Do Nothing)
- Negative-Edge-Triggered Clocking
- D-C Coupling Symplifies System Designs

description

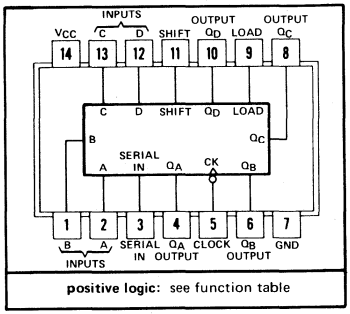
These shift registers utilize fully d-c coupled storage elements and feature synchronous parallel inputs and parallel outputs. The SN54179/SN74179 has a direct clear line and complementary output from the D flip-flop, thereby differing from the SN54178/ SN74178.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

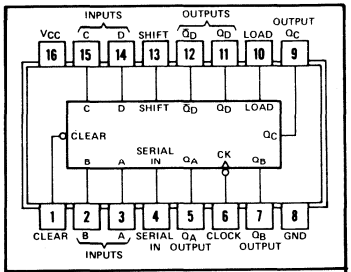
When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

SN54178 . . . J OR W PACKAGE
SN74178 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54179 . . . J OR W PACKAGE
SN74179 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

'178, '179†
FUNCTION TABLE

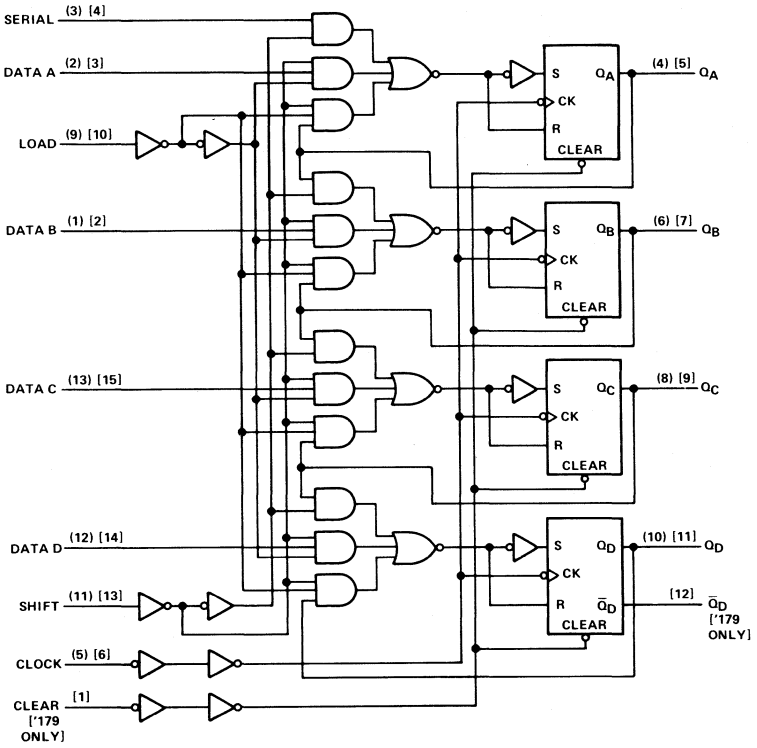
INPUTS									OUTPUTS				
CLEAR†	SHIFT	LOAD	CLOCK	SERIAL	PARALLEL A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$†
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	X	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	L	L	↓	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	L	H	↓	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

†The columns for clear, $\overline{Q}_D$, and the top line of the table apply for the '179 only.

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↓ transition of the clock.

functional block diagram

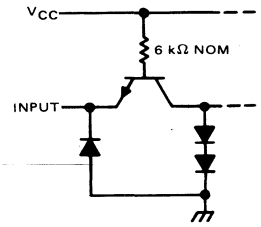
('178) ['179]



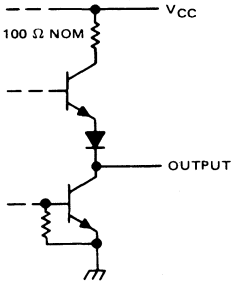
. . . Denotes input activated by a transition from a high level to a low level.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54178, SN54179 Circuits . . . . . −55°C to 125°C
SN74178, SN74179 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54178, SN54179			SN74178, SN74179			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Setup time, t_{su} (see Figure 1)	Shift (H or L) or load	35			35			ns
	Data	30			30			
	Clear-inactive-state (SN54179 and SN74179)	15			15			
Hold time at any input, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54178, SN54179			SN74178, SN74179			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		46	70		46	75	mA

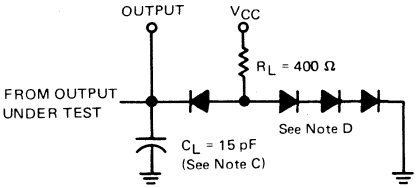
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured as follows:
a) 4.5 V is applied to serial inputs, load, shift, and clear,
b) Parallel inputs A through D are gounded,
c) 4.5 V is momentarily applied to clock which is then grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

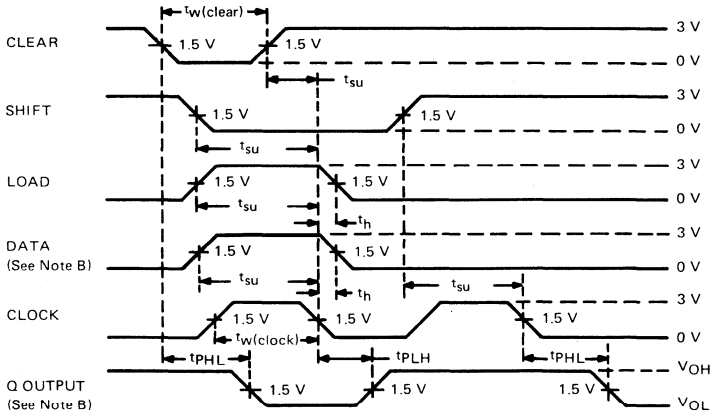
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	39		MHz
t_{PLH}	Clear	$\overline{Q}_D$			15	23	ns
t_{PHL}		Q_A, Q_B, Q_C, Q_D			24	36	
t_{PLH}	Clock	Any output			17	26	ns
t_{PHL}					23	35	

¶ f_{max} ≡ Maximum clock frequency
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PLH} ≡ Propagation delay time, low-to-high-level output

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. Data input and Q output are any related pair. Serial and other data inputs are at GND. Serial data input is tested in conjunction with Q_A output in the shift mode.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

TYPES SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7211814, DECEMBER 1972

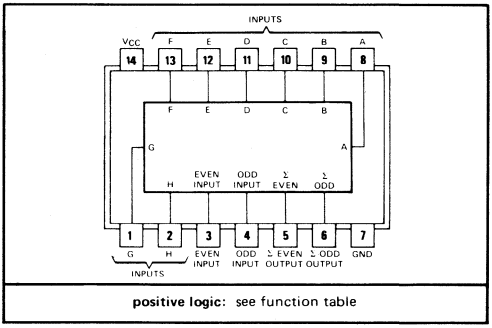
logic

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

SN54180 . . . J OR W PACKAGE
SN74180 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54180 Circuits . . . . . −55°C to 125°C
SN74180 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54180			SN74180			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Any data input	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Even or odd input				80			80	
I_{IL}	Low-level input current	Any data input	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Even or odd input				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		34	49		34	56	mA

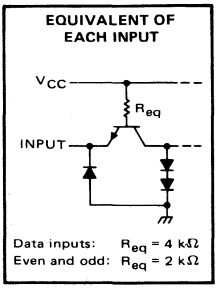
NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

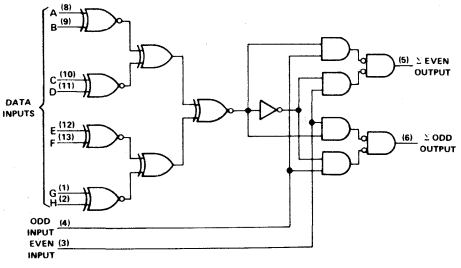
switching characteristics, V_{CC} = 5 V, T_A = 25°C

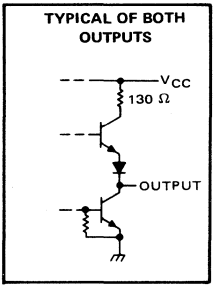
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 400 Ω, Odd input grounded, See Note 3		40	60	ns
t_{PHL}					45	68	
t_{PLH}	Data	Σ Odd			32	48	ns
t_{PHL}					25	38	
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 400 Ω, Even input grounded, See Note 3		32	48	ns
t_{PHL}					25	38	
t_{PLH}	Data	Σ Odd			40	60	ns
t_{PHL}					45	68	
t_{PLH}	Even or Odd	Σ Even or Σ Odd	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}					7	10	

NOTE 3: Load circuits and waveforms are shown on page 3-10.
¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

functional block diagram and schematics of inputs and outputs





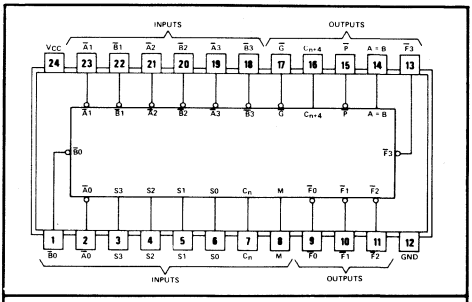


TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

BULLETIN NO. DL-S 7611831, DECEMBER 1972 – REVISED OCTOBER 1976

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

SN54181, SN54LS181, SN54S181 . . . J OR W PACKAGE
SN74181, SN74LS181, SN74S181 . . . J, N OR NT PACKAGE
(TOP VIEW)



logic: see tables 1 and 2

TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES USING '181 AND '182	ADDITION TIMES USING 'LS181 AND '182	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC/ LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2		RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

description (continued)

The '181, 'LS181, and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-high data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A–B–1, which requires an end-around or forced carry to provide A–B.

The '181, 'LS181, or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that is can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-LOW DATA (FIGURE 1)	ACTIVE-HIGH DATA (FIGURE 2)
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of –55°C to 125°C; Series 74, 74LS, and 74S devices are characterized for operation from 0°C to 70°C.

signal designations

The '181, 'LS181, and 'S181 together with the '182 and 'S182 can be used with the signal designations of either Figure 1 or Figure 2. The inversion indicators (○) and the bars over the terminal letter symbols (e.g., $\overline{C}$) each indicate that the associated input or output is active with respect to the selected function of the device when that input or output is low. That is, a low at $\overline{C}$ means "do carry" while a high means "do not carry".

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

signal designations (continued)

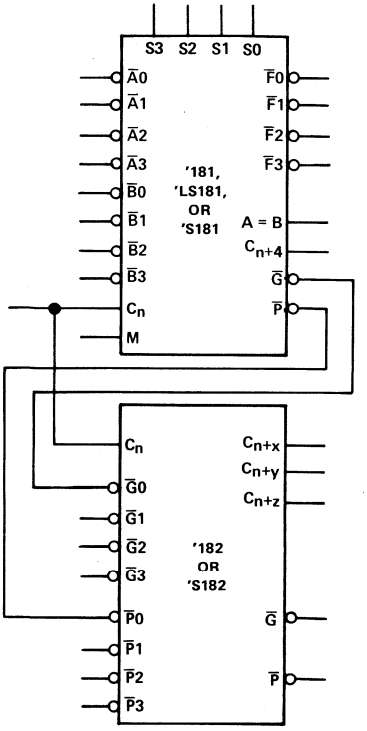


FIGURE 1
(Use with Table 1)

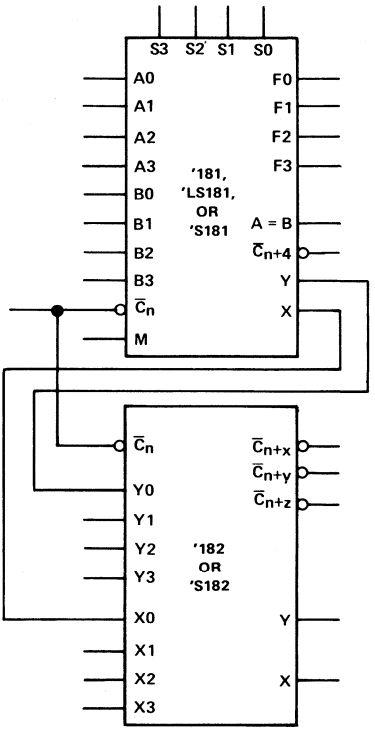


FIGURE 2
(Use with Table 2)

TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A MINUS 1	F = A
L	L	L	H	F = $\overline{A\overline{B}}$	F = AB MINUS 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1	
H	H	H	H	F = A	F = A	F = A PLUS 1

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	$\overline{C}_n$ = H (no carry)	$\overline{C}_n$ = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A PLUS 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L	H	L	L	F = $\overline{A\overline{B}}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L	H	L	H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L	H	H	L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54181 . . . . . −55°C to 125°C
SN74181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54181			SN74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54181			SN74181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Any $\overline{A}$ or $\overline{B}$ input					120			120	
		Any S input					160			160	
		Carry input					200			200	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Any $\overline{A}$ or $\overline{B}$ input					−4.8			−4.8	
		Any S input					−6.4			−6.4	
		Carry input					−8			−8	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−20		−55	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		88	127		88	140	mA
				Condition B		94	135		94	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

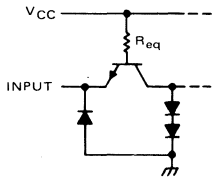
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 400 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	43	ns
t_{PHL}					27	41	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}					33	50	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		13	19	ns
t_{PHL}					12	18	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}					13	19	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}					17	25	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	42	ns
t_{PHL}					21	32	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}					32	48	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

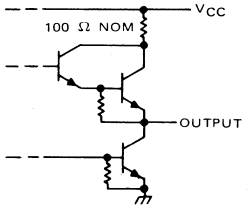
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

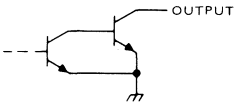


Mode control: R_{eq} = 4 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 2 kΩ NOM
Any S: R_{eq} = 1.3 kΩ NOM
C_n: R_{eq} = 1 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS181 . . . . . −55°C to 125°C
SN74LS181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54LS181			SN74LS181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS181			SN74LS181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	All outputs	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
		Output $\overline{G}$		I_{OL} = 16 mA		0.47	0.7		0.47	0.7	
		Output $\overline{P}$		I_{OL} = 8 mA		0.35	0.6		0.35	0.5	
I_I	Input current at max. input voltage	Mode input	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
		Any $\overline{A}$ or $\overline{B}$ input					0.3			0.3	
		Any S input					0.4			0.4	
		Carry input					0.5			0.5	
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
		Any $\overline{A}$ or $\overline{B}$ input					60			60	
		Any S input					80			80	
		Carry input					100			100	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		Any $\overline{A}$ or $\overline{B}$ input					−1.2			−1.2	
		Any S input					−1.6			−1.6	
		Carry input					−2			−2	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		20	32		20	34	mA
				Condition B		21	35		21	37	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

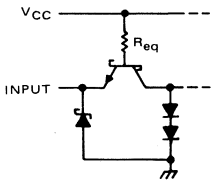
switching characteristics, V_{CC} = 5 V, T_A = 25°C, (C_L = 15 pF, R_L = 2 kΩ, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			18	27	ns
t_{PHL}					13	20	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		25	38	ns
t_{PHL}					25	38	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		27	41	ns
t_{PHL}					27	41	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		17	26	ns
t_{PHL}					13	20	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		19	29	ns
t_{PHL}					15	23	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					21	32	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, ($\overline{SUM}$ mode)		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		20	30	ns
t_{PHL}					22	33	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		21	32	ns
t_{PHL}					13	20	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					21	32	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		22	33	ns
t_{PHL}					26	38	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		33	50	ns
t_{PHL}					41	62	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

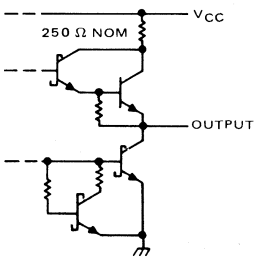
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

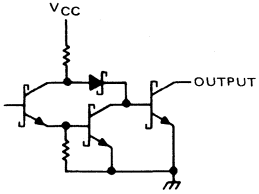


Mode control: R_{eq} = 17 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 5.67 kΩ NOM
Any S: R_{eq} = 4.25 kΩ NOM
C_n: R_{eq} = 2.86 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature: SN54S181 . . . . . −55°C to 125°C
SN74S181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each $\overline{A}$ input in conjunction with inputs S2 or S3, and to each $\overline{B}$ input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54S181			SN74S181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S181			SN74S181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX,	V_I = 2.5 V			50			50	μA
		Any $\overline{A}$ or $\overline{B}$ input					150			150	
		Any S input					200			200	
		Carry input					250			250	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX,	V_I = 0.5 V			−2			−2	mA
		Any $\overline{A}$ or $\overline{B}$ input					−6			−6	
		Any S input					−8			−8	
		Carry input					−10			−10	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	T_A = 125°C, W package only			195				mA
			V_{CC} = MAX,	See Note 3, All packages		120	220		120	220	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):
A. S0 through S3, M, and $\overline{A}$ inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.
B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.

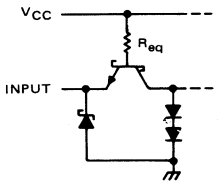
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 280 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15.5	23	ns
t_{PHL}					15.5	23	
t_{PLH}	C_n	Any $\overline{F}$	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		8	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		7.5	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	$\overline{P}$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		11	16.5	ns
t_{PHL}					11	16.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (logic mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any $\overline{A}$ or $\overline{B}$	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15	23	ns
t_{PHL}					20	30	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

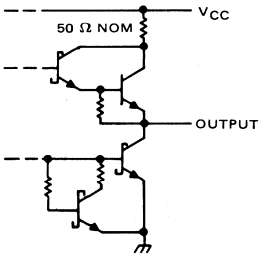
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

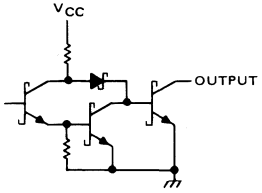


Mode control: R_{eq} = 2.8 kΩ NOM
Any $\overline{A}$ or $\overline{B}$: R_{eq} = 940 Ω NOM
Any S: R_{eq} = 700 Ω NOM
C_n: R_{eq} = 560 Ω NOM

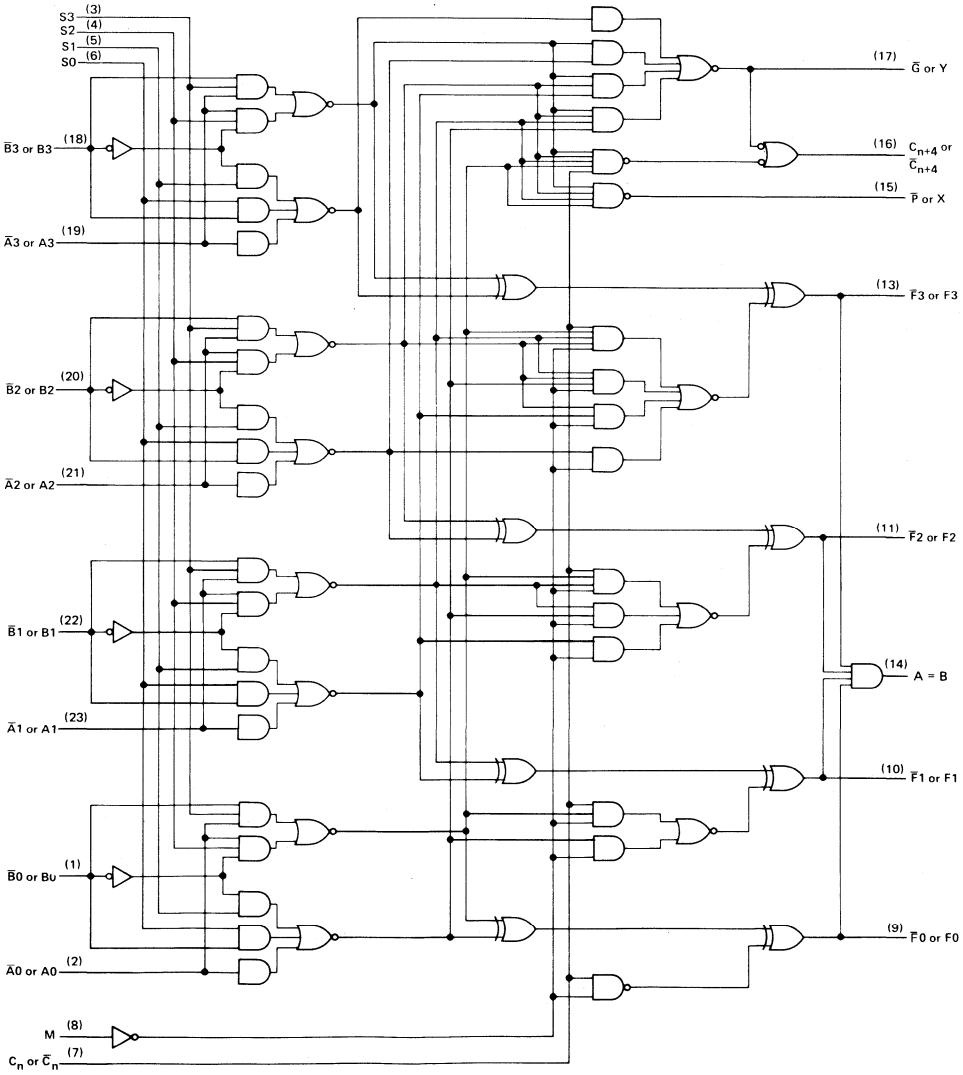
TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



functional block diagram



7

PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of Phase
t_{PHL}							
t_{PLH}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or any $\overline{F}$	In-Phase
t_{PHL}							
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$, $\overline{B}$, C_n	C_{n+4}	In -Phase
t_{PHL}							

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}							
t_{PLH}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}							

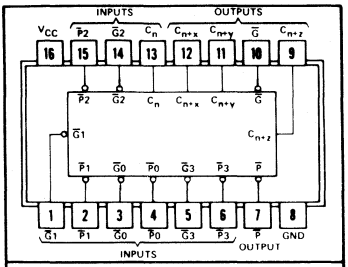
NOTE 4: Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

TYPES SN54182, SN54S182, SN74182, SN74S182
LOOK-AHEAD CARRY GENERATORS

BULLETIN NO. DL-S 7611823, DECEMBER 1972—REVISED OCTOBER 1976

- Directly Compatible for Use With:
  SN54181/SN74181, SN54LS181/SN74LS181,
  SN54S281/SN74S281, SN54S381, SN74S381,
  SN54S481/SN74S481

SN54182, SN54S182 . . . J OR W PACKAGE
SN74182, SN74S182 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function tables

PIN DESIGNATIONS

ALTERNATIVE	DESIGNATIONS†	PIN NOS.	FUNCTION
$\overline{G0}$, $\overline{G1}$, $\overline{G2}$, $\overline{G3}$	G0, G1, G2, G3	3, 1, 14, 5	CARRY GENERATE INPUTS
$\overline{P0}$, $\overline{P1}$, $\overline{P2}$, $\overline{P3}$	P0, P1, P2, P3	4, 2, 15, 6	CARRY PROPAGATE INPUTS
C_n	$\overline{C}_n$	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	$\overline{C}_{n+x}$, $\overline{C}_{n+y}$, $\overline{C}_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\overline{G}$	Y	10	CARRY GENERATE OUTPUT
$\overline{P}$	X	7	CARRY PROPAGATE OUTPUT
V_{CC}		16	SUPPLY VOLTAGE
GND		8	GROUND

†Interpretations are illustrated on page 7-273

description

The SN54182, SN54S182, SN74182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the '182 and 'S182 are:

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\,(X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\,[X1 + Y0\,(X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\,\{X2 + Y1\,[X1 + Y0\,(X0 + C_n)]\}}$$
$$Y = Y3\,(X3 + Y2)\,(X3 + X2 + Y1)\,(X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

logic

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

logic

FUNCTION TABLE
FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G}0$	$\overline{P}0$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE
FOR C_{n+y} OUTPUT

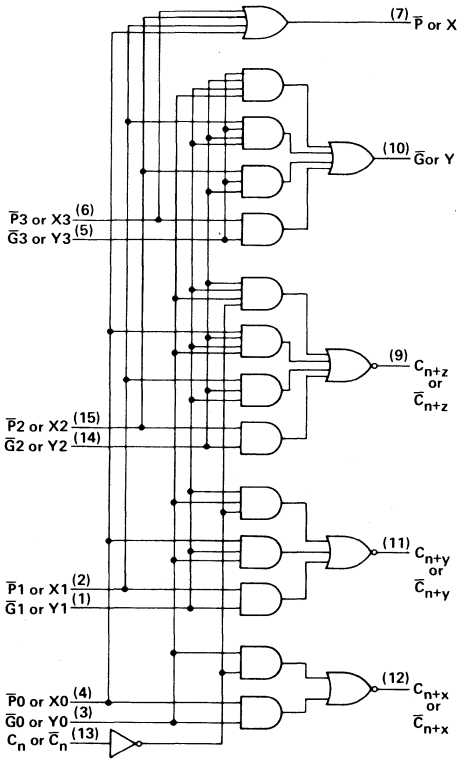
INPUTS					OUTPUT
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each $\overline{G}$ input in conjunction with any other $\overline{G}$ input or in conjunction with any $\overline{P}$ input.

recommended operating conditions

	SN54182			SN74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54182			SN74182			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	C_n input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		$\overline{P}3$ input				120			120	
		$\overline{P}2$ input				160			160	
		$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				200			200	
		$\overline{G}0$ or $\overline{G}2$ input				360			360	
		$\overline{G}1$ input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		$\overline{P}3$ input				−4.8			−4.8	
		$\overline{P}2$ input				−6.4			−6.4	
		$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				−8			−8	
		$\overline{G}0$ or $\overline{G}2$ input				−14.4			−14.4	
		$\overline{G}1$ input				−16			−16	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5 V, See Note 3		27			27		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		45	65		45	72	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 5		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S182			SN74S182			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	C_n input	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
		$\overline{P}3$ input				100			100	
		$\overline{P}2$ input				150			150	
		$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				200			200	
		$\overline{G}0$ or $\overline{G}2$ input				350			350	
		$\overline{G}1$ input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
		$\overline{P}3$ input				−4			−4	
		$\overline{P}2$ input				−6			−6	
		$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				−8			−8	
		$\overline{G}0$ or $\overline{G}2$ input				−14			−14	
		$\overline{G}1$ input				−16			−16	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5 V, See Note 3		35			35		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		69	99		69	109	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

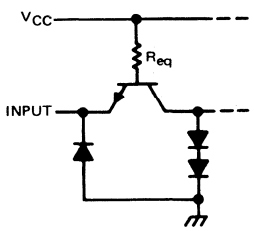
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 280 Ω, C_L = 15 pF, See Note 5		4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, P1, P2, or P3	$\overline{G}$			5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{P}$			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

schematics of inputs and outputs

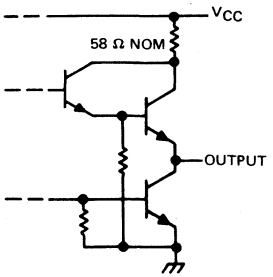
'182

EQUIVALENT OF EACH INPUT



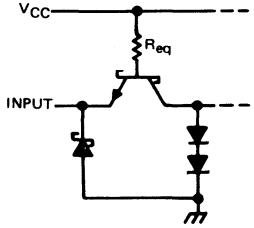
INPUT	R_{eq} NOM
C_n	2.8 kΩ
$\overline{P}3$	1.4 kΩ
$\overline{P}2$	940 Ω
$\overline{P}0$, $\overline{P}1$, $\overline{G}3$	700 Ω
$\overline{G}0$, $\overline{G}4$	400 Ω
$\overline{G}1$	350 Ω

TYPICAL OF ALL OUTPUTS



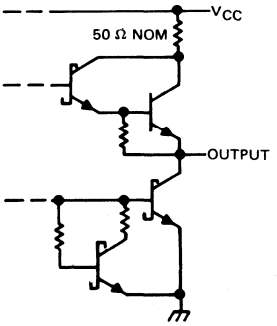
'S182

EQUIVALENT OF EACH INPUT

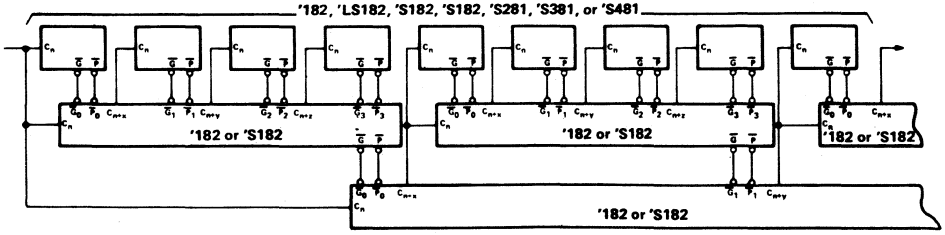


INPUT	R_{eq} NOM
C_n	2.8 kΩ
$\overline{P}3$	1.4 kΩ
$\overline{P}2$	940 Ω
$\overline{P}0$, $\overline{P}1$, $\overline{G}3$	700 Ω
$\overline{G}0$, $\overline{G}4$	400 Ω
$\overline{G}1$	350 Ω

TYPICAL OF ALL OUTPUTS



TYPICAL APPLICATION DATA



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

Remaining inputs and outputs of '181, 'LS181, 'S181 'S281, 'S381, and 'S481 are not shown.

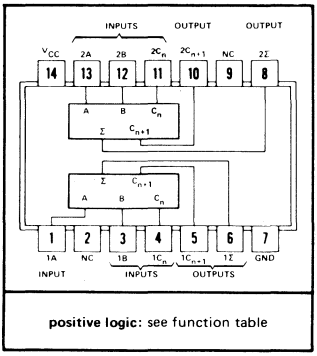
TYPES SN54LS183, SN74LS183
DUAL CARRY-SAVE FULL ADDERS

BULLETIN NO. DL-S 7611848, OCTOBER 1976

- For Use in High-Speed Wallace-Tree Summing Networks
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design

TYPES	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'LS183	15 ns	23 mW per bit

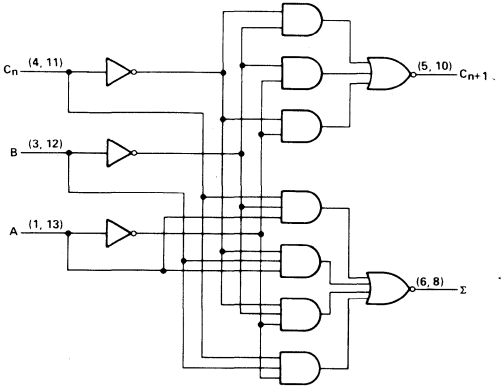
SN54LS183 . . . J OR W PACKAGE
SN74LS183 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

functional block diagram (each adder)



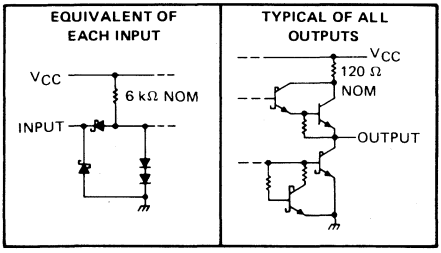
FUNCTION TABLE
(EACH ADDER)

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

H = high level, L = low level

schematics of inputs and outputs

'LS183



description

These dual full adders feature an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two gate delays. The circuits utilize high-speed, high-fan-out, transistor-transistor logic (TTL), but are compatible with both DTL and TTL families. Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54H183 Circuits . . . . . −55°C to 125°C
SN74H183 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between any two inputs to the same adder.

recommended operating conditions

	SN54H183			SN74H183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				150	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 3	SN54H183		48	69	mA
			SN74H183		48	75	
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX, See Note 4			40	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. I_{CCL} is measured with all outputs open and all inputs grounded.
4. I_{CCH} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 25 pF, R_L = 280 Ω, See Note 5		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns

NOTE 5: Load circuit and waveforms are shown on page 3-10.

Phased out types!

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS183 Circuits . . . . . −55°C to 125°C
SN74LS183 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values, except interemitter voltage, are with respect to network ground terminal.

recommended operating conditions

	SN54LS183			SN74LS183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operation free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.3			0.3	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			60			60	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.2			−1.2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX,	See Note 3		10	17		10	17	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX,	See Note 4		8	14		8	14	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. I_{CCL} is measured with all outputs open and all inputs grounded.
4. I_{CCH} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 kΩ, See Note 6		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	33	ns

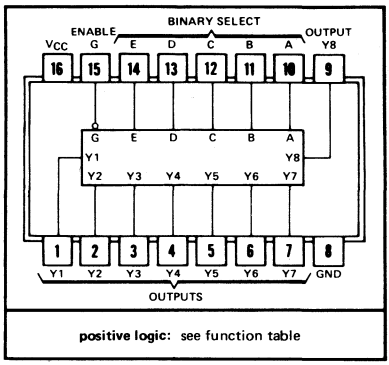
NOTE 6: Load circuit and waveforms are shown on page 3-11.

TYPES SN54184, SN54185A, SN74184, SN74185A
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

BULLETIN NO. DL-S 7211392, FEBRUARY 1971 – REVISED DECEMBER 1972

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

SN54184, SN54185A . . . J OR W PACKAGE
SN74184, SN74185A . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the function tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the '185A and all "don't care" conditions of the '184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

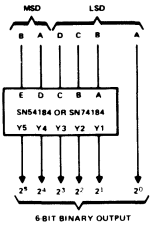
a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

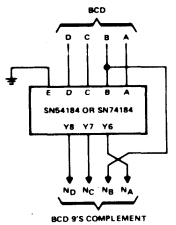
INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	56	80
3	6	140	200
4	11	196	280
5	19	280	400
6	28	364	520

SN54184 and SN74184 BCD-to-binary converters (continued)

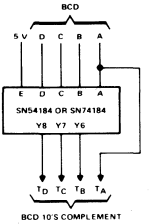
6-BIT CONVERTER



BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



FUNCTION TABLE BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table (above, right) when the devices are connected as shown above the function table.

FUNCTION TABLE BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

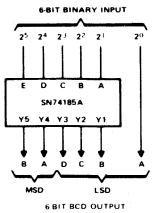
TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



FUNCTION TABLE

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 - 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 - 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 - 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 - 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 - 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 - 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 - 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 - 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 - 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 - 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 - 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 - 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 - 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 - 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 - 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 - 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 - 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 - 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 - 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 - 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 - 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 - 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 - 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 - 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 - 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 - 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 - 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 - 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 - 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 - 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 - 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 - 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

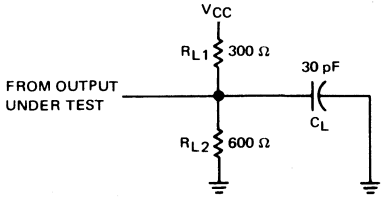
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	99	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable G	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1 and Note 2		19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable G			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select			27	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select			23	40	ns

PARAMETER MEASUREMENT INFORMATION

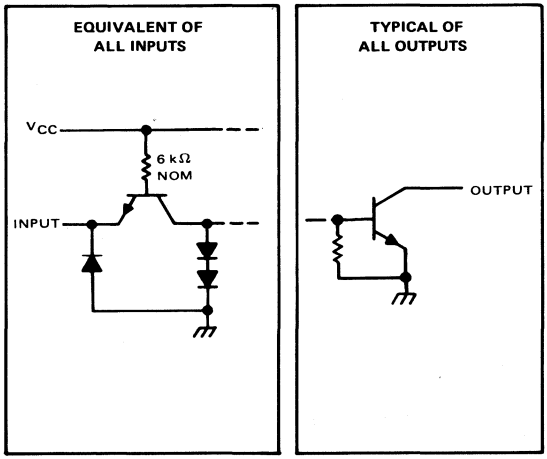


C_L includes probe and jig capacitance.

LOAD CIRCUIT FIGURE 1

NOTE 2: Voltage waveforms are shown on page 3-10.

schematics of inputs and outputs



TYPICAL APPLICATION DATA
SN54184, SN74184

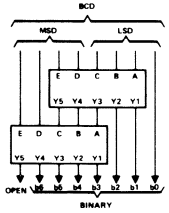


FIGURE 1–BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

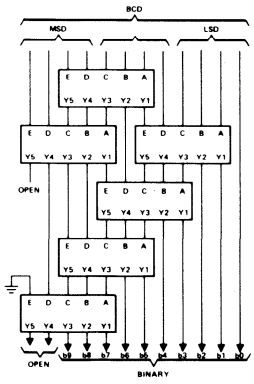


FIGURE 2–BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

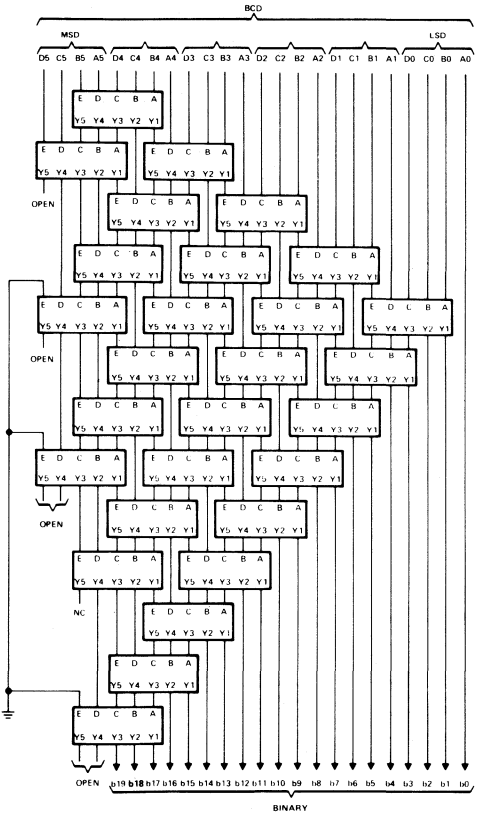


FIGURE 3–BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

MSD–most significant decade
LSD–least significant decade
Each rectangle represents an SN54184 or SN74184.

TYPICAL APPLICATION DATA
SN54185A, SN74185A

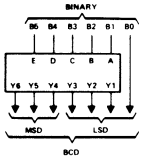


FIGURE 4–6-BIT BINARY-TO-BCD CONVERTER

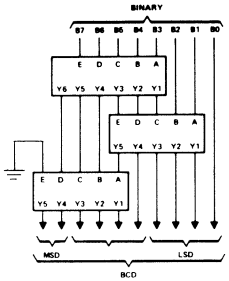


FIGURE 5–8-BIT BINARY-TO-BCD CONVERTER

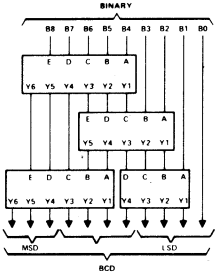


FIGURE 6–9-BIT BINARY-TO-BCD CONVERTER

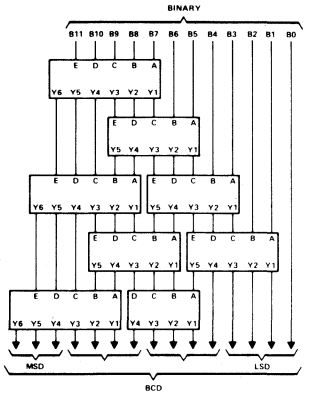


FIGURE 7–12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

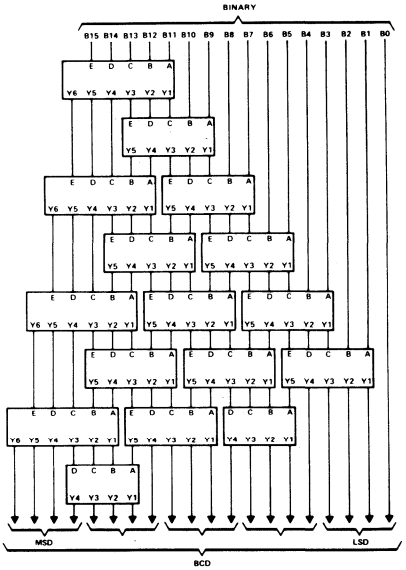


FIGURE 8–16-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

MSD—Most significant decade
LSD—Least significant decade
NOTES: A. Each rectangle represents an SN54185A or an SN74185A.
B. All unused E inputs are grounded.

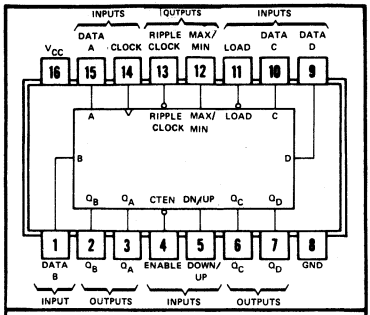
TYPES SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

BULLETIN NO. DL-S 11865, DECEMBER 1972 – REVISED DECEMBER 1980

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190, '191	20 ns	25 MHz	325 mW
'LS190, 'LS191	20 ns	25 MHz	100 mW

SN54', SN54LS' . . . J OR W PACKAGE
SN74', SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

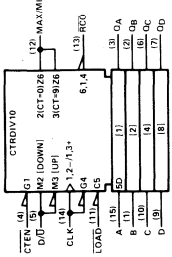
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

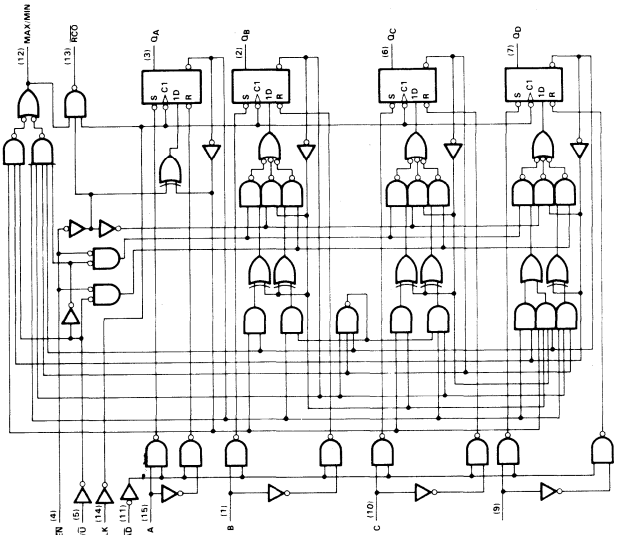
Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

functional block diagrams

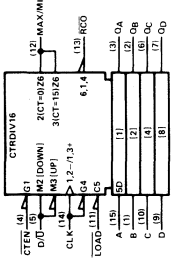
LS190 logic symbol



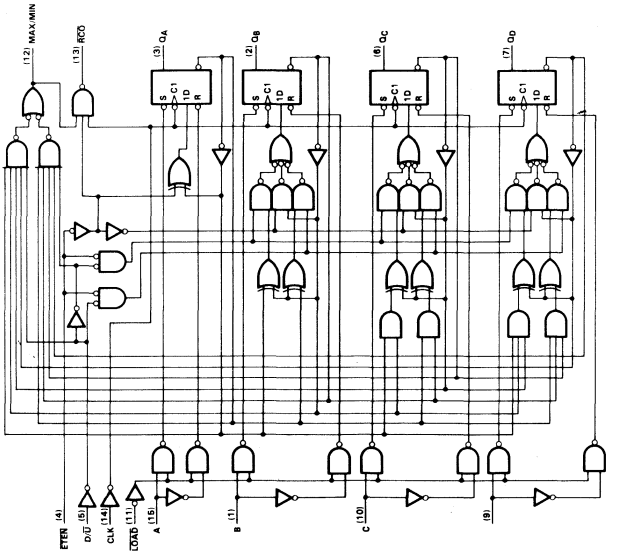
LS190 logic diagram (positive logic)



LS191 logic symbol



LS191 logic diagram (positive logic)

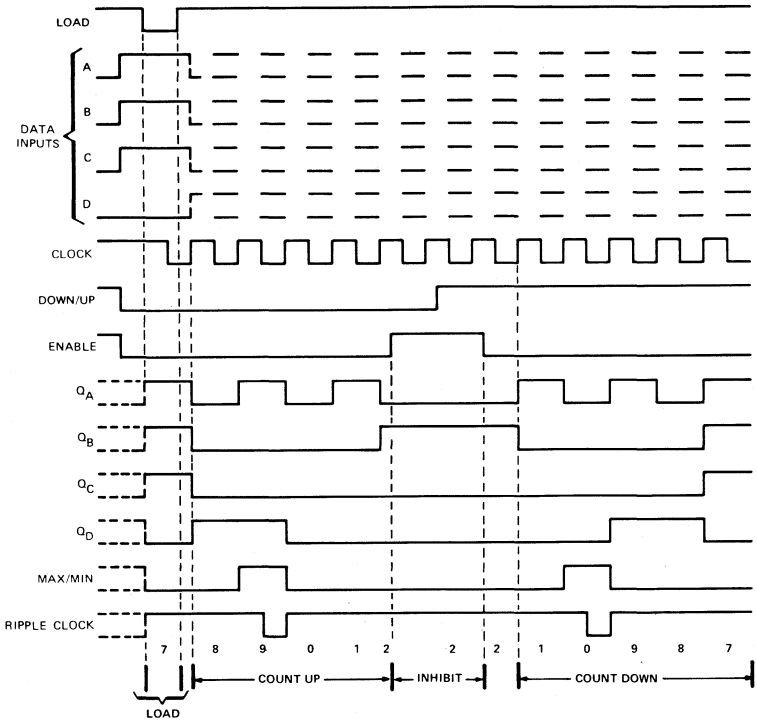


'190, 'LS190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

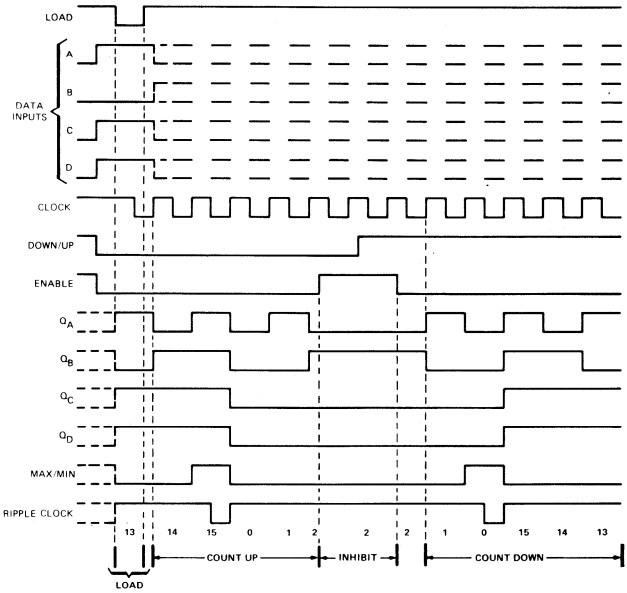


'191, 'LS191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: SN54', SN74' Circuits . . . . . 5.5 V
SN54LS', SN74LS' Circuits . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54190, SN54191			SN74190, SN74191			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Input clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	V_{CC} = MIN	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MIN			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	High-level input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current at any input except enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IH}	High-level input current at enable input				120			120	μA
I_{IL}	Low-level input current at any input except enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{IL}	Low-level input current at enable input				−4.8			−4.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	99		65	105	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

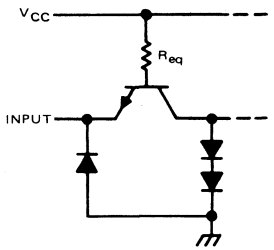
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'190, '191			UNIT
				MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

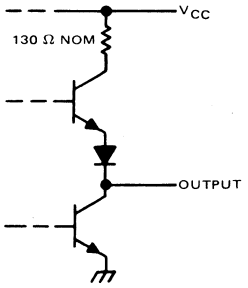
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable input: R_{eq} = 1.3 kΩ NOM
All other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN54LS190 SN54LS191			SN74LS190 SN74LS191			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)	30			30			ns
Data hold time, t_{hold}	5			5			ns
Count enable time, t_{enable} (see Note 3))	40			40			ns
Load Inactive setup time, t_{su}	30			30			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS190 SN54LS191			SN74LS190 SN74LS191			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	High-level input current at maximum input voltage	Enable	V_{CC} = MAX, V_I = 7 V				0.3			0.3	mA
		Others					0.1			0.1	
I_{IH}	High-level input current	Enable	V_{CC} = MAX, V_I = 2.7 V				60			60	μA
		Others					20			20	
I_{IL}	Low-level input current	Enable	V_{CC} = MAX, V_I = 0.4 V				−1.2			−1.2	mA
		Others					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			20	35		20	35	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTES: 2. I_{CC} is measured with all inputs grounded and all outputs open.
3. Minimum count enable time is the interval immediately preceeding the rising edge of the clock pulse during which interval the count enable input must be low to ensure counting.

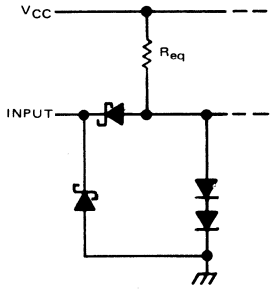
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS190, 'LS191			UNIT
				MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			20	32	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	
t_{PLH}	Enable	Ripple Clock			21	33	ns
t_{PHL}					22	33	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

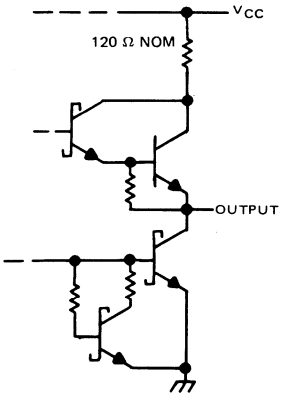
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable input: R_{eq} = 8.33 kΩ NOM
Load input: R_{eq} = 25 kΩ NOM
All other inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF ALL OUTPUTS



PARAMETER MEASUREMENT INFORMATION

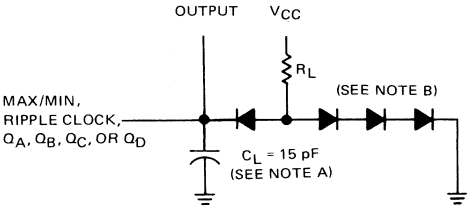


FIGURE 1–LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT

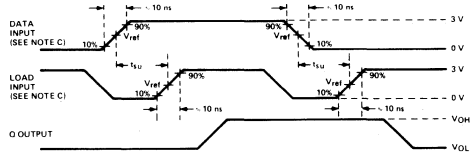
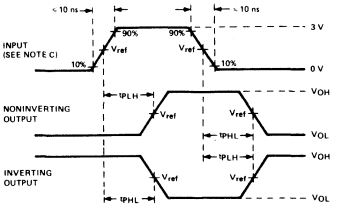


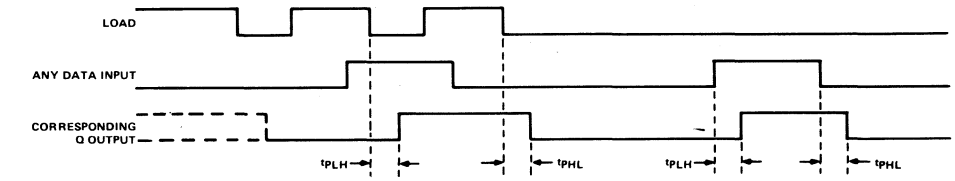
FIGURE 2–DATA SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

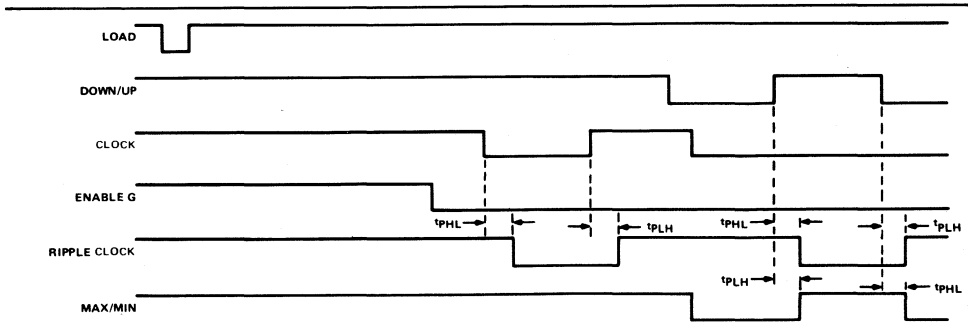
FIGURE 3–GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.5 V for '190 and '191; 1.3 V for 'LS190 and 'LS191.



NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4–LOAD TO OUTPUT AND DATA TO OUTPUT

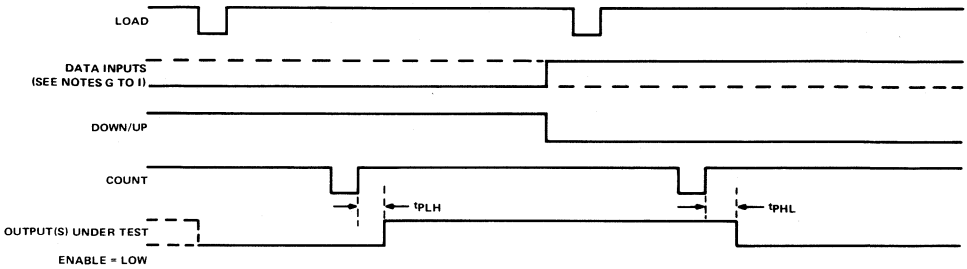


NOTE F: All data inputs are low.

FIGURE 5–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

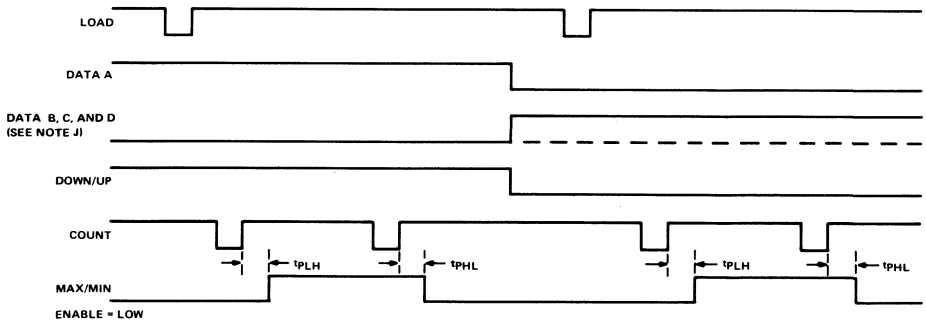
PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



NOTES: G. to test Q_A, Q_B, and Q_C outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
H. To test Q_D output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
I. To test Q_A, Q_B, Q_C, and Q_D outputs of '191 and 'LS191: All four data inputs are shown by the solid line.

FIGURE 6–CLOCK TO OUTPUT



NOTE J: Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 7–CLOCK TO MAX/MIN

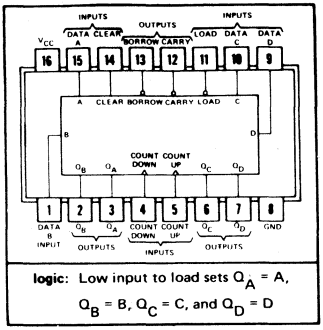
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7611828, DECEMBER 1972– REVISED OCTOBER 1976

- **Cascading Circuitry Provided Internally**
- **Synchronous Operation**
- **Individual Preset to Each Flip-Flop**
- **Fully Independent Clear Input**

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'LS192, 'LS193	32 MHz	95 mW

SN54', SN54LS'...J OR W PACKAGE
SN74', SN74LS'...J OR N PACKAGE
(TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

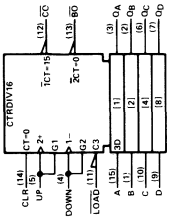
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

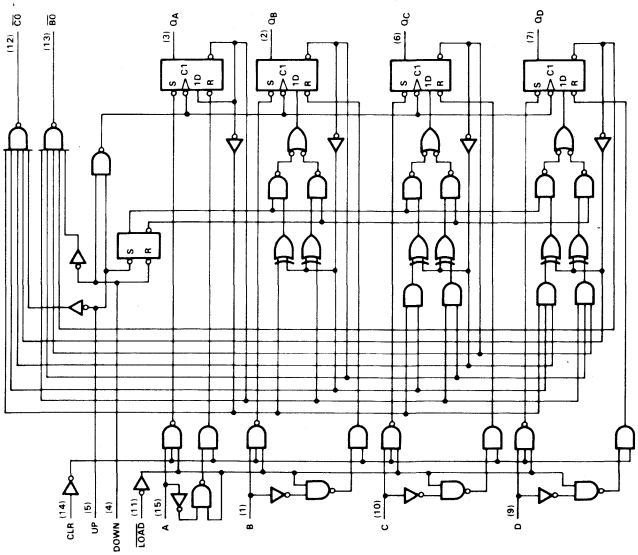
NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagrams

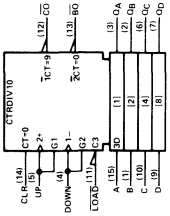
'193, 'LS193 logic symbol



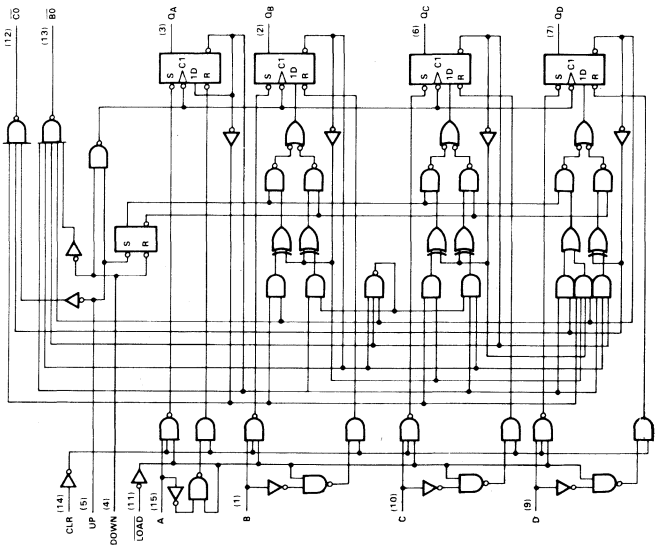
'193, 'LS193 logic diagrams (positive logic)



'192, 'LS192 logic symbol

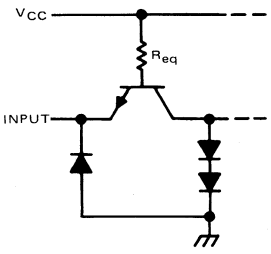


'192, 'LS192 logic diagram (positive logic)



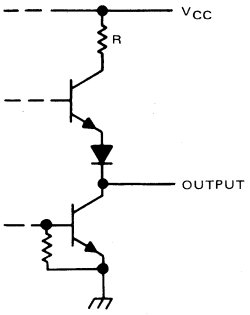
schematics of inputs and outputs

EQUIVALENT OF INPUTS
OF '192, '193



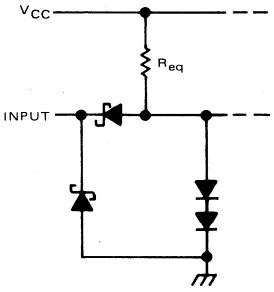
'192, '193: R_{eq} = 4 kΩ NOM

TYPICAL OF OUTPUTS
OF '192, '193



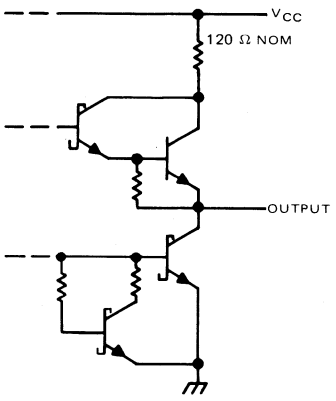
'192, '193: R = 130 Ω NOM

EQUIVALENT OF INPUTS
OF 'LS192, 'LS193



Load input: Req = 25 kΩ NOM
All other inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF OUTPUTS
OF 'LS192, 'LS193

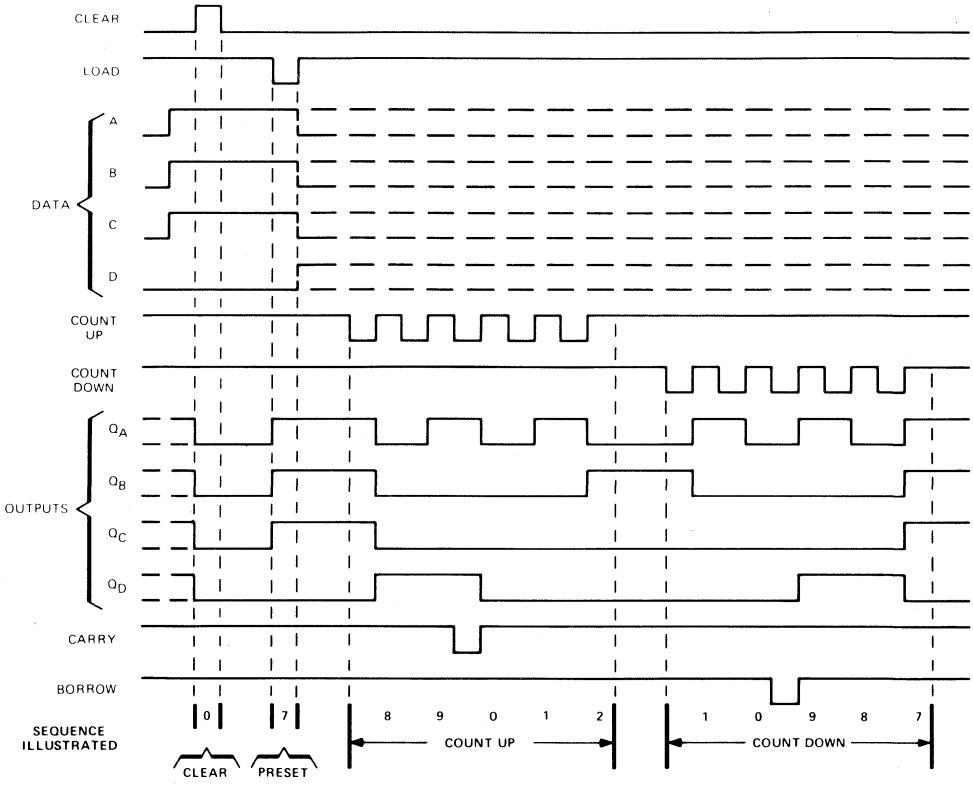


'192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



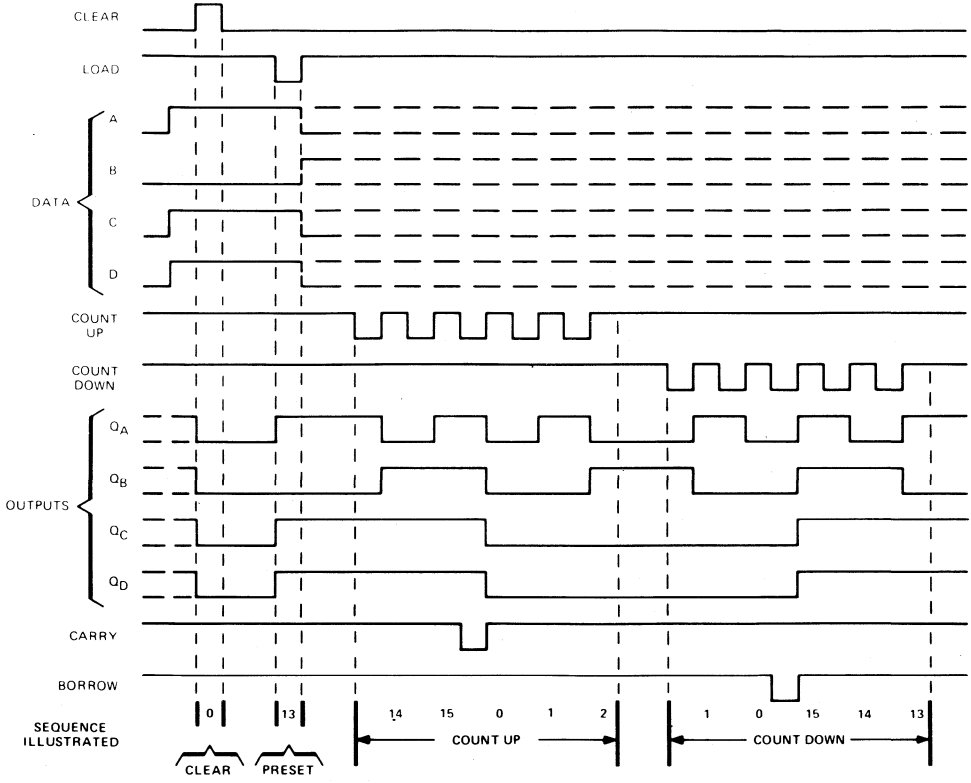
NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

	SN54192 SN54193			SN74192 SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Data hold time, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54192 SN54193			SN74192 SN74193			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2	25	32		MHz
t_{PLH}	Count-up	Carry			17	26	ns
t_{PHL}					16	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either Count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

REVISED DECEMBER 1980

recommended operating conditions

	SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Clear inactive-state setup time	40			40			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Data hold time, t_h	5			5			ns
Operating free-air temperature range, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.15	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			19	34		19	34	mA

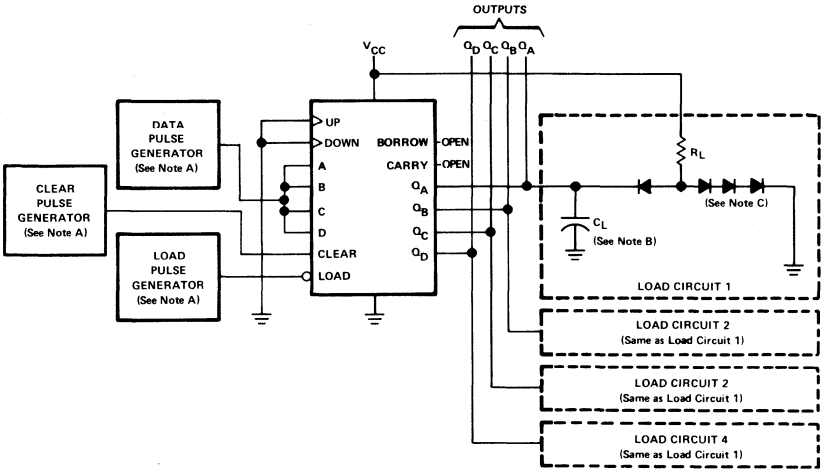
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

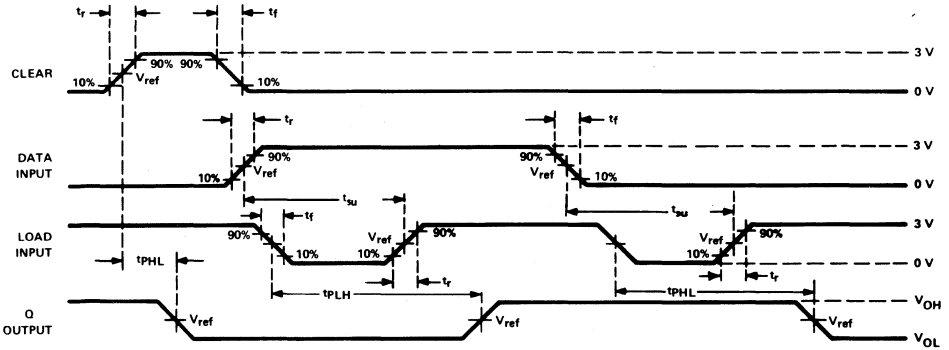
PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2	25	32		MHz
t_{PLH}	Count-up	Carry			17	26	ns
t_{PHL}					18	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					15	24	
t_{PLH}	Either Count	Q			27	38	ns
t_{PHL}					30	47	
t_{PLH}	Load	Q			24	40	ns
t_{PHL}					25	40	
t_{PHL}	Clear	Q			23	35	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

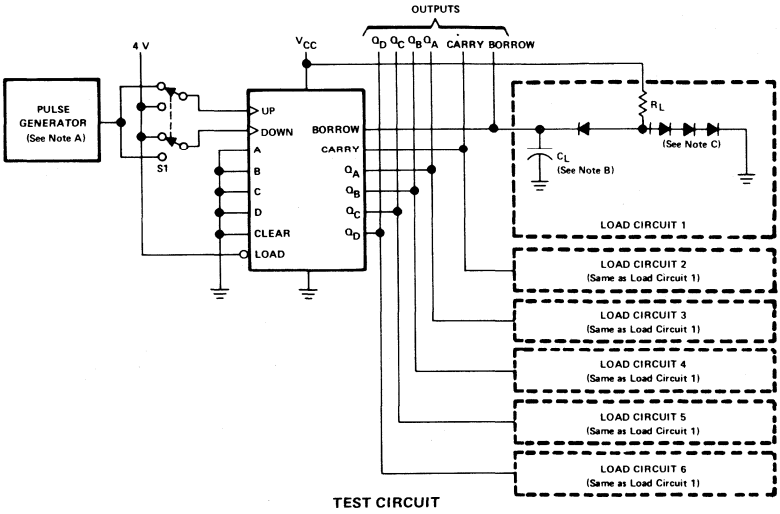


VOLTAGE WAVEFORMS

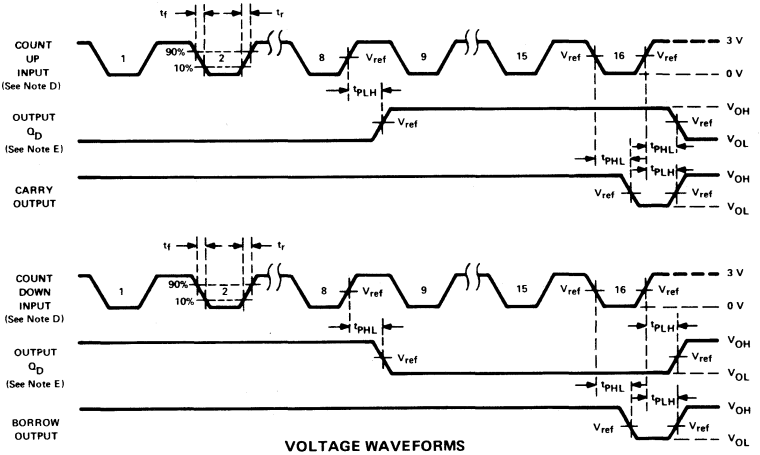
NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR $\leqslant$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 for '192, '193, 'LS192, and 'LS193.
D. t_r and $t_f \leqslant 7$ ns for '192, '193, 'LS192, and 'LS193;
E. V_{ref} is 1.5 volts for '192 and '193; 1.3 volts for 'LS192, and 'LS193.

FIGURE 1–CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 for '192, '193, 'LS192, and 'LS193.
D. Count-up and count-down pulse shown are for the '193, and 'LS193 binary counters. Count cycle for '192, and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7$ ns for '192, '193, 'LS192, and 'LS193;
G. V_{ref} is 1.5 volts for '192 and '193; 1.3 volts for LS192, and 'LS193.

FIGURE 2–PROPAGATION DELAY TIMES

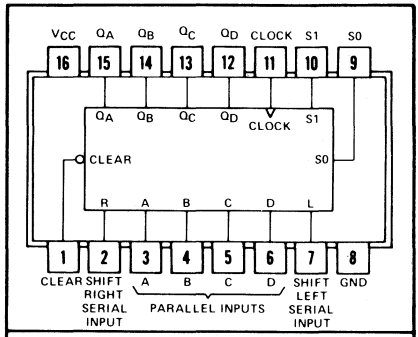
TYPES SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7611866, MARCH 1974—REVISED OCTOBER 1976

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194A	36 MHz	75 mW
'S194	105 MHz	425 mW

SN54194, SN54LS194A, SN54S194 . . . J OR W PACKAGE
SN74194, SN74LS194A, SN74S194 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transistion of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

FUNCTION TABLE

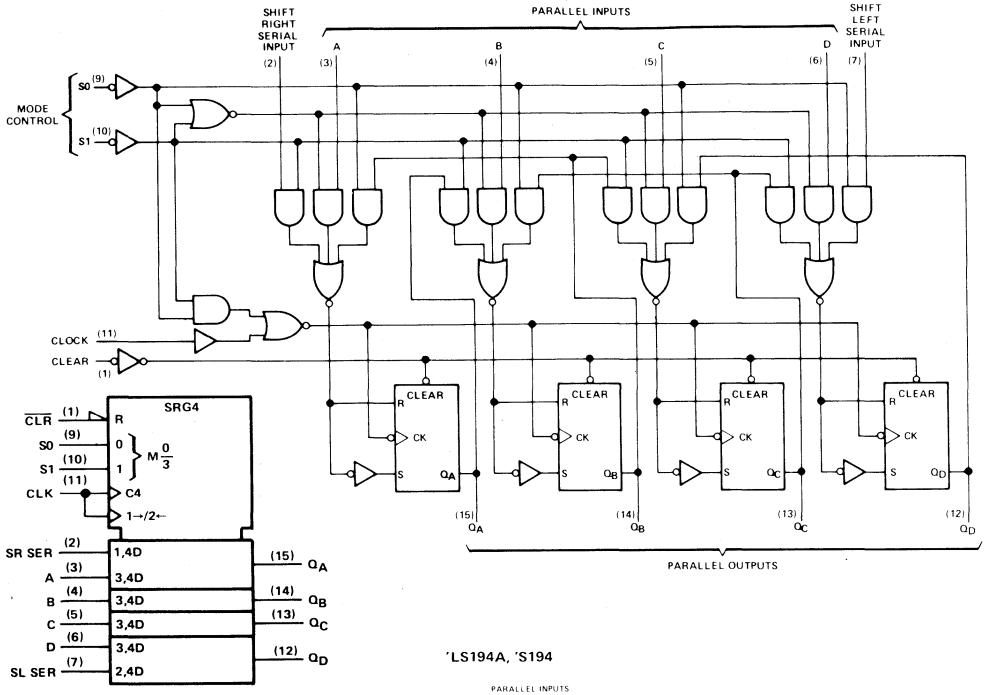
INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	See note		L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

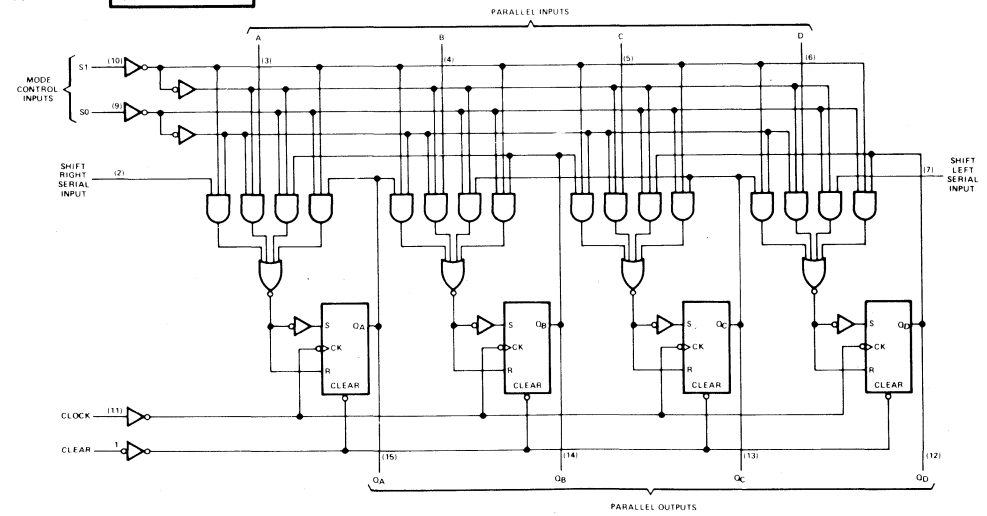
S0 or S1 of 54194/74194 should be changed only while the clock input is high. For all other types covered on this data sheet S0 = X and S1 = X for this function.

functional block diagrams

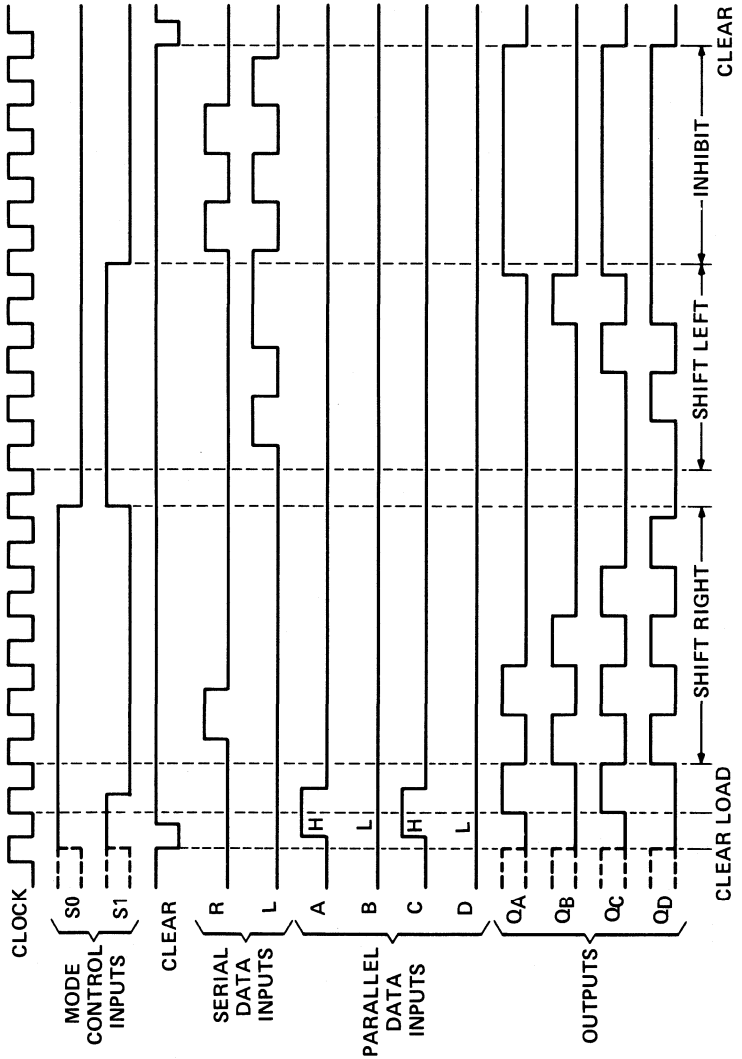
'194



'LS194A, 'S194

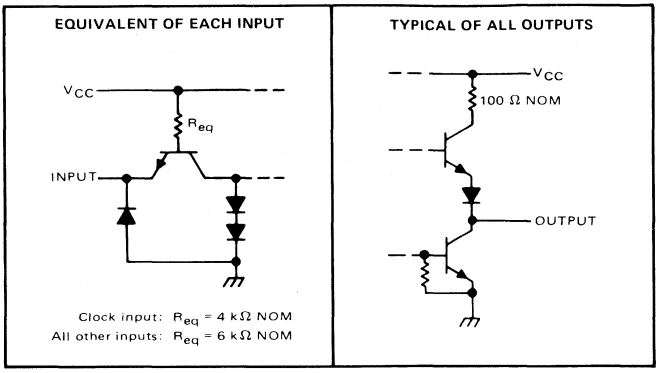


typical clear, load, right-shift, left-shift, inhibit, and clear sequences

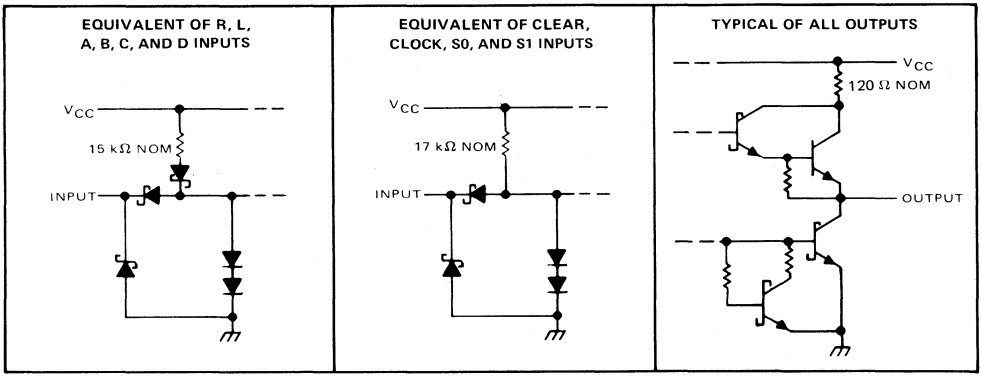


schematics of inputs and outputs

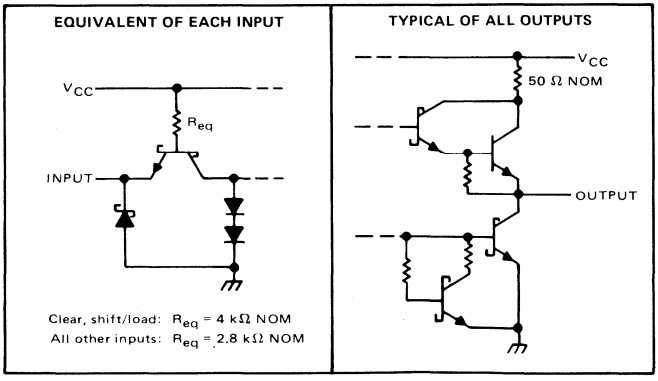
'194



'LS194A



'S194



REVISED MARCH 1974

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54194 . . . . . −55°C to 125°C
SN74194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54194			SN74194			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		39	63		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS194A . . . . . −55°C to 125°C
SN74LS194A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS194A			SN74LS194A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS194A			SN74LS194A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			15	23		15	23	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S194 . . . . . −55°C to 125°C
SN74S194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S194			SN74S194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock pulse, $t_{w(clock)}$		7			7			ns
Width of clear pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{su}	Mode control	11			11			ns
	Serial and parallel data	5			5			ns
	Clear inactive-state	9			9			ns
Hold time at any input, t_h		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

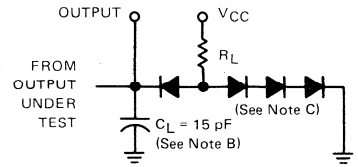
PARAMETER		TEST CONDITIONS†		SN54S194			SN74S194			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		85	135		85	135	mA
		V_{CC} = MAX, T_A = 125°C, See Note 2	W package			110				

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applies to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momemtary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Figure 1	70	105		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		4	8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		4	11	16.5	ns

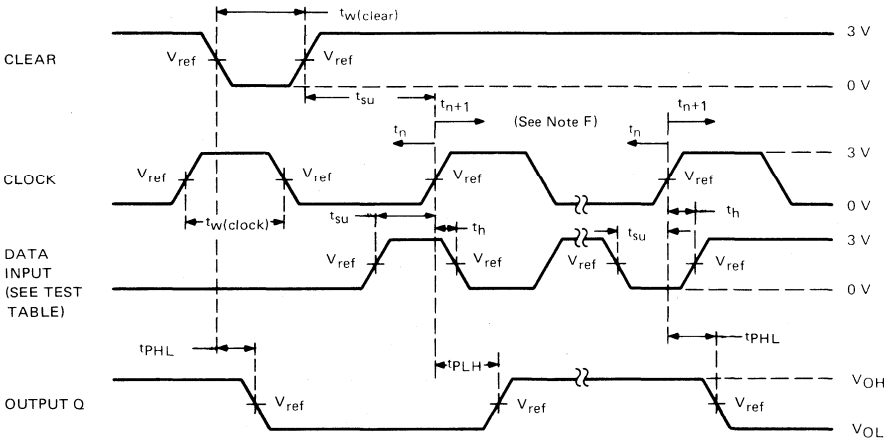
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz, For '194, $t_r \leq 7$ ns and $t_f \leq 7$ ns. For 'LS194A, $t_r \leq 15$ ns and $t_f \leq 6$ ns. For 'S194, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. A clear pulse is applied prior to each test.
E. For '194 and 'S194, $V_{ref} = 1.5$ V; for 'LS194A, $V_{ref} = 1.3$ V.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

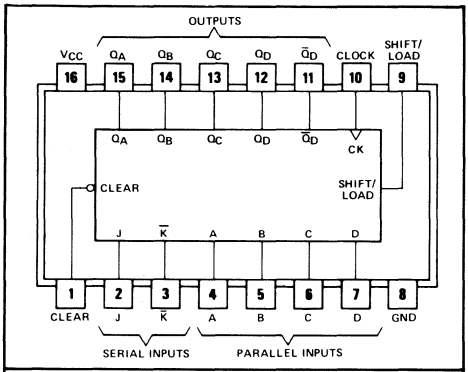
FIGURE 1–SWITCHING TIMES

TYPES SN54195, SN54LS195A, SN54S195, SN74195, SN74LS195A, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7611820, MARCH 1974—REVISED OCTOBER 1976

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High-Performance:
  Accumulators/Processors
  Serial-to-Parallel, Parallel-to-Serial Converters

SN54195, SN54LS195A, SN54S195 . . . J OR W PACKAGE
SN74195, SN74LS195A, SN74S195 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load
Shift (in the direction Q_A toward Q_D)

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195A	39 MHz	70 mW
'S195	105 MHz	350 mW

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

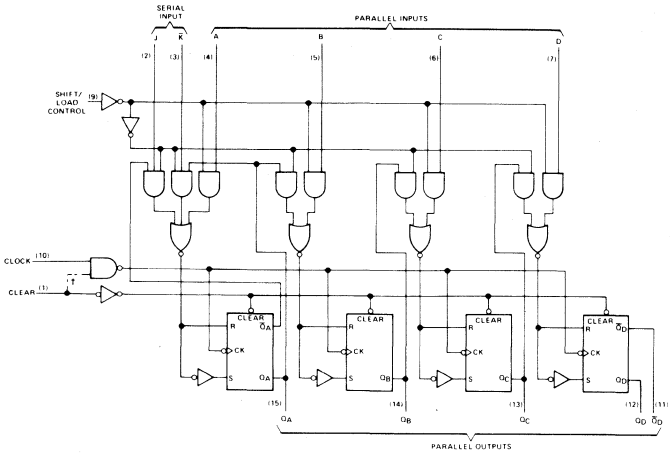
The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

FUNCTION TABLE

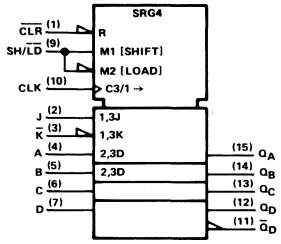
INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock

logic diagram (positive logic)

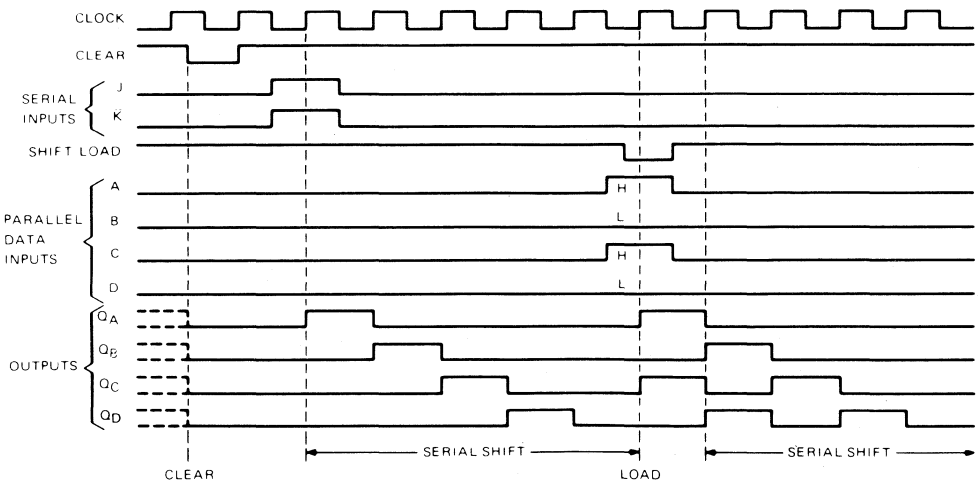


logic symbol



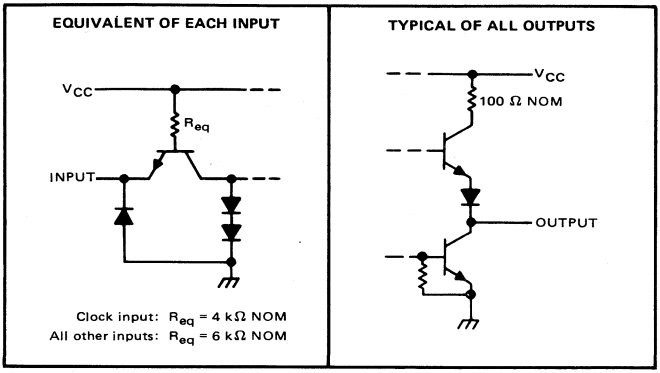
†This connection is made on '195 only.

typical clear, shift, and load sequences

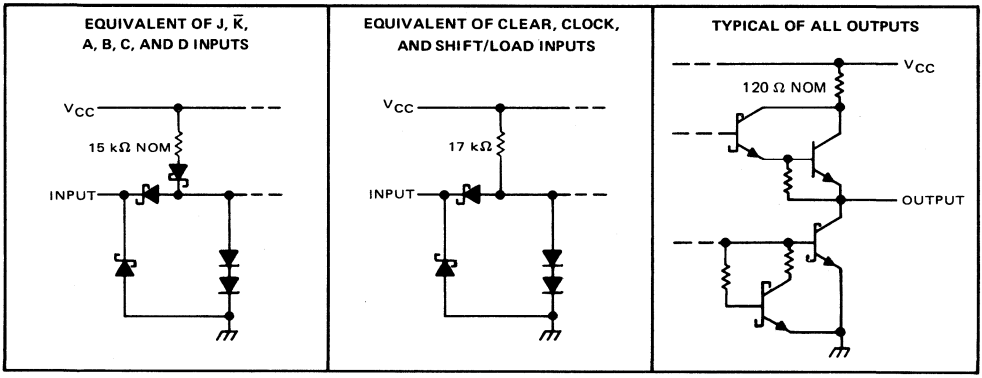


schematics of inputs and outputs

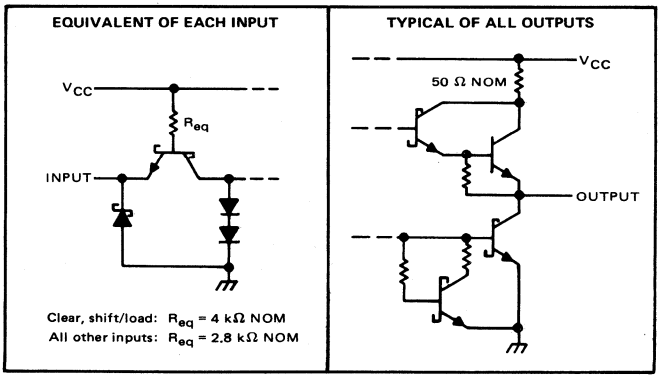
'195



'LS195A



'S195



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54195 . . . . . −55°C to 125°C
SN74195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54195			SN74195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{su} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	20			20			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				10			10	ns
Serial and parallel data hold time, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54195	−20		−57	mA
			SN74195	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS195A . . . . . −55°C to 125°C
SN74LS195A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS195A			SN74LS195A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{su} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				0			0	ns
Serial and parallel data hold time, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS195A			SN74LS195A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			14	21		14	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S195 . . . . . −55°C to 125°C
SN74S195 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S195			SN74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock input pulse, $t_{w(clock)}$		7			7			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{su} (see Figure 1)	Shift/load	11			11			ns
	Serial and parallel data	5			5			
	Clear inactive-state	9			9			
Shift/load release time, $t_{release}$ (see Figure 1)				6			6	ns
Serial and parallel data hold time, t_h (see Figure 1)		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

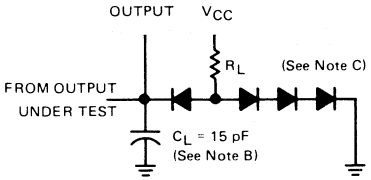
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	SN54S195	2.5	3.4		V
				SN74S195	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	SN54S195		70	99	mA
				SN74S195		70	109	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

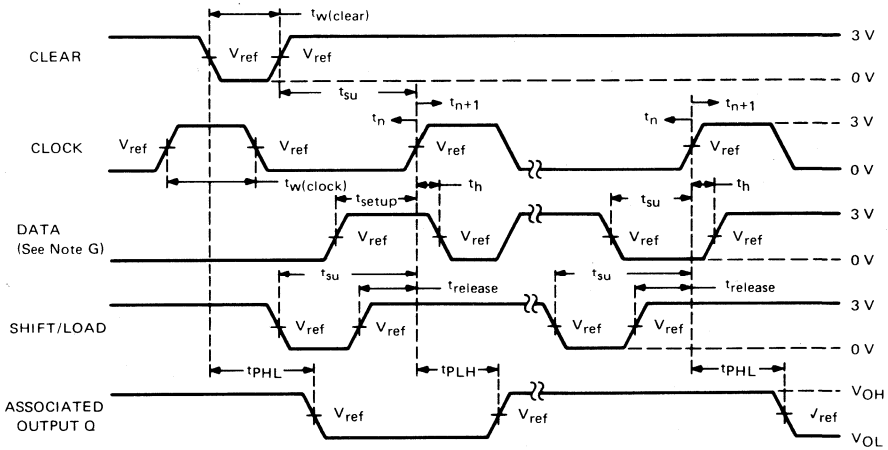
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Figure 1	70	105		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			11	16.5	ns

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz. For '195, $t_r \leq 7$ ns and $t_f \leq 7$ ns. For 'LS195A, $t_r \leq 15$ ns and $t_f \leq 6$ ns. For 'S195, $t_r = 2.5$ ns and $t_f = 2.5$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. For '195 and 'S195, $V_{ref} = 1.5$ V; for 'LS195A, $V_{ref} = 1.3$ V.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

G. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

H. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1–SWITCHING TIMES

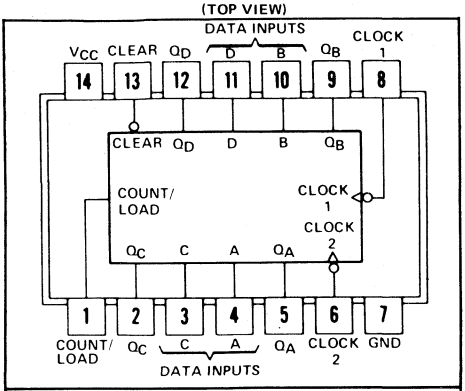
TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN54S196, SN54S197, SN74196, SN74197, SN74LS196, SN74LS197, SN74S196, SN74S197
50/30/100-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

BULLETIN NO. DL-S 7611806, OCTOBER 1976

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED COUNT FREQUENCY		TYPICAL POWER DISSIPATION
	CLOCK 1	CLOCK 2	
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	80 mW
'S196, 'S197	0-100 MHz	0-50 MHz	375 mW

SN54', SN54LS', SN54S' . . . J OR W PACKAGE
SN74', SN74LS', SN74S' . . . J OR N PACKAGE
(TOP VIEW)



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops, which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196, 'S196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197, 'S197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Series 54, 54LS, and 54S circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74LS, and 74S circuits are characterized for operation from 0°C to 70°C.

typical count configurations

'196, 'LS196, and 'S196 typical count configurations and function tables are the same as those for '176.

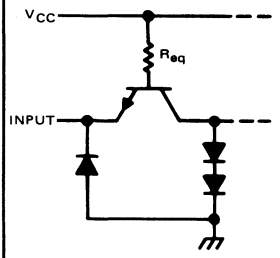
'197, 'LS197, and 'S197 typical count configurations and function tables are the same as those for '177.

functional block diagrams

'196, 'LS196, and 'S196 functional block diagram is the same as that for '176.
'197, 'LS197, and 'S197 functional block diagram is the same as that for '177.

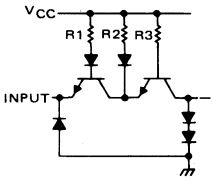
schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS



Count/load, Data: R_{eq} = 4 kΩ NOM
Clear: R_{eq} = 2 kΩ NOM

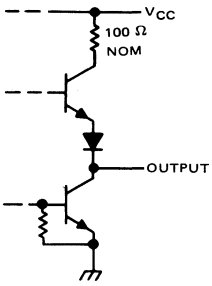
EQUIVALENT OF CLOCK INPUTS



NOMINAL VALUES OF R1, R2, and R3

INPUT	'196	'197
Clock 1	4 kΩ	4 kΩ
Clock 2	3 kΩ	6 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits . . . . . −55°C to 125°C
SN74196, SN74197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		SN54196, SN54197			SN74196, SN74197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency	Clock-1 input	0		50	0		50	MHz
	Clock-2 input	0		25	0		25	
Pulse width, t_w	Clock-1 input	10			10			ns
	Clock-2 input	20			20			
	Clear	15			15			
	Load	20			20			
Input hold time, t_h	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			$t_{w(load)}$			
Input setup time, t_{su}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (See Note 3)		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54196, SN74196			SN54197, SN74197			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		clear, clock 1					80			80	
		clock 2					120			80	
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		clear					−3.2			−3.2	
		clock 1					−4.8			−4.8	
		clock 2					−6.4			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			48	59		48	59	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196 SN74196			SN54197 SN74197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 5	50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A			7	12		7	12	ns
t_{PHL}					10	15		10	15	
t_{PLH}	Clock 2	Q_B			12	18		12	18	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Clock 2	Q_C			24	36		24	36	ns
t_{PHL}					28	42		28	42	
t_{PLH}	Clock 2	Q_D			14	21		36	54	ns
t_{PHL}					12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			16	24		16	24	ns
t_{PHL}					25	38		25	38	
t_{PLH}	Load	Any			22	33		22	33	ns
t_{PHL}					24	36		24	36	
t_{PHL}	Clear	Any			25	37		25	37	ns

◇f_{max} ≡ maximum count frequency.

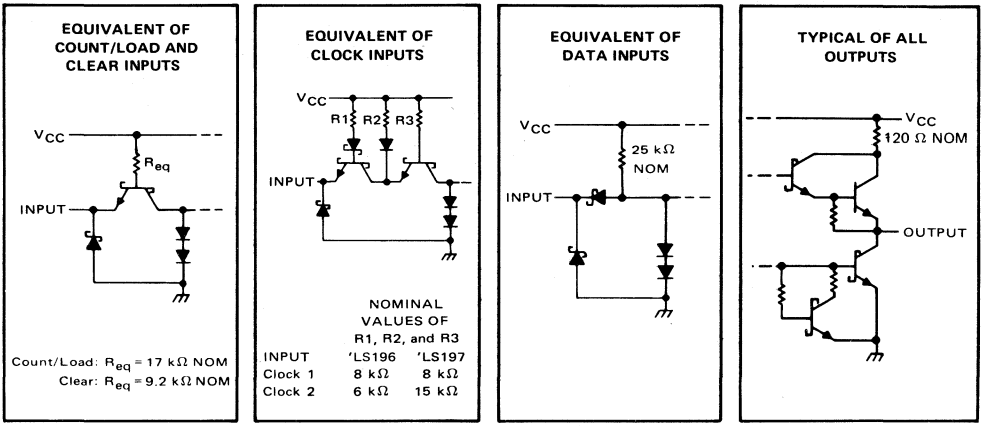
t_{PLH} ≡ propagation delay time, low-to-high-level output.

t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 5: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 (page 7-248) except that testing f_{max}, V_{IL} = 0.3 V.

REVISED OCTOBER 1976

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS196, SN54LS197 Circuits . . . . . −55°C to 125°C
SN74LS196, SN74LS197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency	Clock-1 input	0		30	0		30	MHz
	Clock-2 input	0		15	0		15	
Pulse width, t_w	Clock-1 input	20			20			ns
	Clock-2 input	30			30			
	Clear	15			15			
	Load	20			20			
Input hold time, t_h	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			$t_{w(load)}$			
Input setup time, t_{su}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (See Note 3)		30			30			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS196 SN54LS197			SN74LS196 SN74LS197			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA¶					0.35	0.5	
I_I Input current at maximum input voltage	Data, count/load	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
	Clear, clock 1					0.2			0.2	
	Clock 2 of 'LS196					0.4			0.4	
	Clock 2 of 'LS197					0.2			0.2	
I_{IH} High-level input current	Data, count/load	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
	Clear, clock 1					40			40	
	Clock 2 of 'LS196					80			80	
	Clock 2 of 'LS197					40			40	
I_{IL} Low-level Input current	Data, count/load	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Clear					−0.8			−0.8	
	Clock 1					−2.4			−2.4	
	Clock 2 of 'LS196					−2.8			−2.8	
	Clock 2 of 'LS197					−1.3			−1.3	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 4			16	27		16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

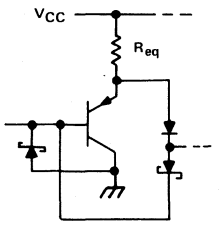
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196 SN74LS196			SN54LS197 SN74LS197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Note 6	30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A			8	15		8	15	ns
t_{PHL}					13	20		14	21	
t_{PLH}	Clock 2	Q_B			16	24		12	19	ns
t_{PHL}					22	33		23	35	
t_{PLH}	Clock 2	Q_C			38	57		34	51	ns
t_{PHL}					41	62		42	63	
t_{PLH}	Clock 2	Q_D			12	18		55	78	ns
t_{PHL}					30	45		63	95	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C Q_D			20	30		18	27	ns
t_{PHL}					29	44		29	44	
t_{PLH}	Load	Any			27	41		26	39	ns
t_{PHL}					30	45		30	45	
t_{PHL}	Clear	Any			34	51		34	51	ns

◇f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 (page 7-253) except that $t_r \leq 15$ ns, $t_f \leq 6$ ns, and V_{ref} = 1.3 V (as opposed to 1.5 V)

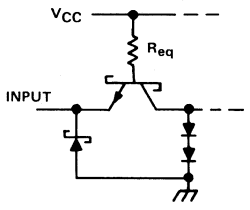
schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS



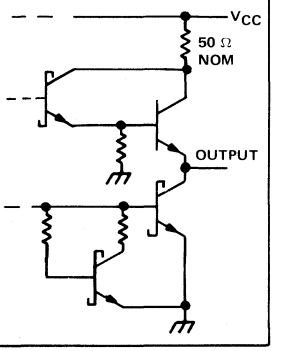
Count/Load, Clear: R_{eq} = 2.3 kΩ NOM
Data: R_{eq} = 2.8 kΩ NOM

EQUIVALENT OF CLOCK INPUT



Clock 1 R_{eq} = 1.2 kΩ NOM
Clock 2 'S196 R_{eq} = 700 Ω NOM
Clock 2 'S197 R_{eq} = 1.4 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S196, SN54S197 Circuits . . . . . −55°C to 125°C
SN74S196, SN74S197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S196, SN54S197			SN74S196, SN74S197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency	Clock-1 input	0		100	0		100	MHz
	Clock-2 input	0		50	0		50	
Pulse width, t_w	Clock-1 input	5			5			ns
	Clock-2 input	10			10			
	Clear	30			30			
	Load	5			5			
Input hold time, t_h	High-level data	3↑			3↑			ns
	Low-level data	3↑			3↑			
Input setup time, t_{su}	High-level data	6↑			6↑			ns
	Low-level data	6↑			6↑			
Count enable time, t_{enable} (see Note 3)		12			12			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: Minimum count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs are both high to permit counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54S196, SN74S196 MIN	SN54S196, SN74S196 TYP‡	SN54S196, SN74S196 MAX	SN54S197, SN74S197 MIN	SN54S197, SN74S197 TYP‡	SN54S197, SN74S197 MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		54S	2.5	3.4		2.5	3.4		V
					74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA¶					0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V					1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V					50			50	μA
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.5 V					0.75			0.75	mA
		clear						−8			−8	mA
		clock 1						−10			−6	mA
		clock 2										
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−30		−110	−30		−110	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		54S		75	110		75	110	mA
					74S		75	120		75	120	

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 20 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54S/74S loads.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S196, SN74S196 MIN	SN54S196, SN74S196 TYP	SN54S196, SN74S196 MAX	SN54S197, SN74S197 MIN	SN54S197, SN74S197 TYP	SN54S197, SN74S197 MAX	UNIT
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 280 Ω, See Note 7	100	140		100	140		MHz
t_{PLH}	Clock 1	Q_A			5	10		5	10	ns
t_{PHL}					6	10		6	10	
t_{PLH}	Clock 2	Q_B			5	10		5	10	ns
t_{PHL}					8	12		8	12	
t_{PLH}	Clock 2	Q_C			12	18		12	18	ns
t_{PHL}					16	24		15	22	
t_{PLH}	Clock 2	Q_D			5	10		18	27	ns
t_{PHL}					8	12		22	33	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			7	12		7	12	ns
t_{PHL}					12	18		12	18	
t_{PLH}	Load	Any			10	18		10	18	ns
t_{PHL}					12	18		12	18	
t_{PHL}	Clear	Any			26	37		26	37	ns

◇f_{max} ≡ maximum input county frequency.
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 7: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 on page 7-253.

TYPES SN54198, SN54199, SN74198, SN74199
8-BIT SHIFT REGISTERS

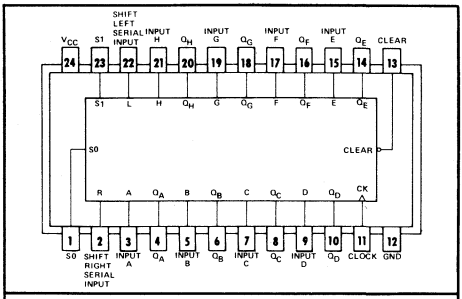
BULLETIN NO. DL-S 7611841, DECEMBER 1972—REVISED OCTOBER 1976

description

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 devices are characterized for operation from 0°C to 70°C.

SN54198 . . . J OR W PACKAGE
SN74198 . . . J, N OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

SN54198 and SN74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

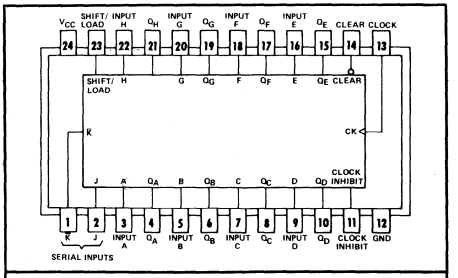
'198
FUNCTION TABLE

INPUTS							OUTPUTS
CLEAR	MODE		CLOCK	SERIAL		PARALLEL	Q_A Q_B . . . Q_G Q_H
	S_1	S_0		LEFT	RIGHT	A . . . H	
L	X	X	X	X	X	X	L L L L
H	X	X	L	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}
H	H	H	↑	X	X	a . . . h	a b g h
H	L	H	↑	X	H	X	H Q_{An} Q_{Fn} Q_{Gn}
H	L	H	↑	X	L	X	L Q_{An} Q_{Fn} Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn} Q_{Cn} Q_{Hn} H
H	H	L	↑	L	X	X	Q_{Bn} Q_{Cn} Q_{Hn} L
H	L	L	X	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

SN54199 and SN74199

SN54199 . . . J OR W PACKAGE
SN74199 . . . J, N OR NT PACKAGE
(TOP VIEW)



positive logic: see function table

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the function table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

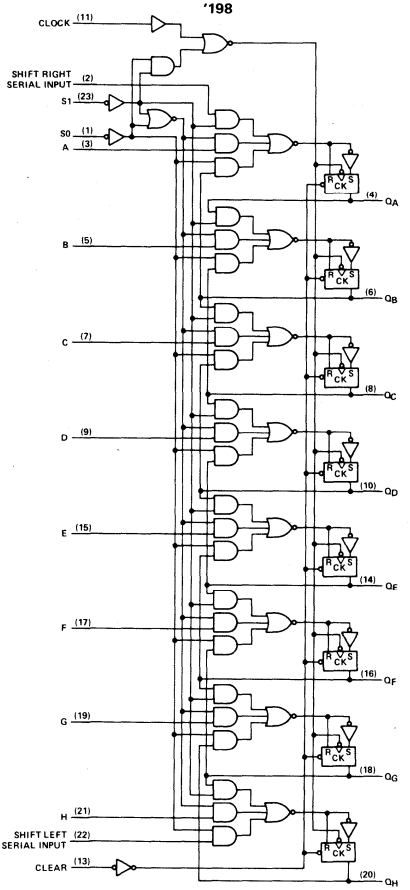
'199
FUNCTION TABLE

INPUTS							OUTPUTS			
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A . . . H	Q_A	Q_B	Q_C . . .	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c	h
H	H	L	↑	L	H	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

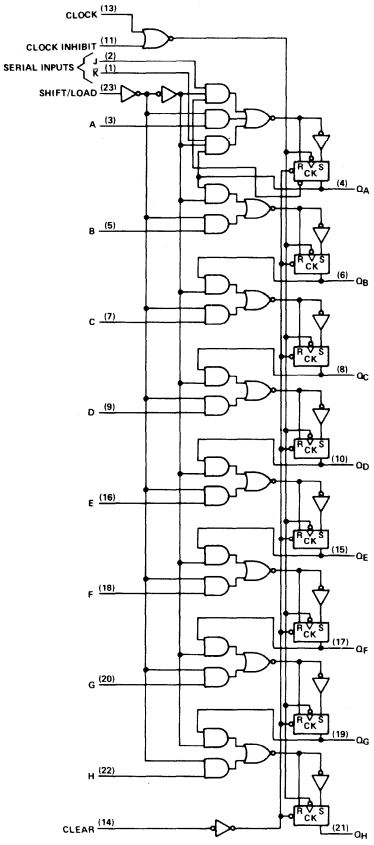
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{C0} . . . Q_{H0} = the level of Q_A, Q_B, or Q_C thru Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn} . . . Q_{Gn} = the level of Q_A or Q_B thru Q_G, respectively, before the most-recent ↑ transition of the clock.

functional block diagrams

'198

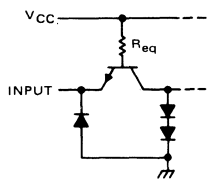


'199



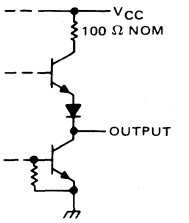
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Clear, A thru H: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



TEXAS INSTRUMENTS
INCORPORATED
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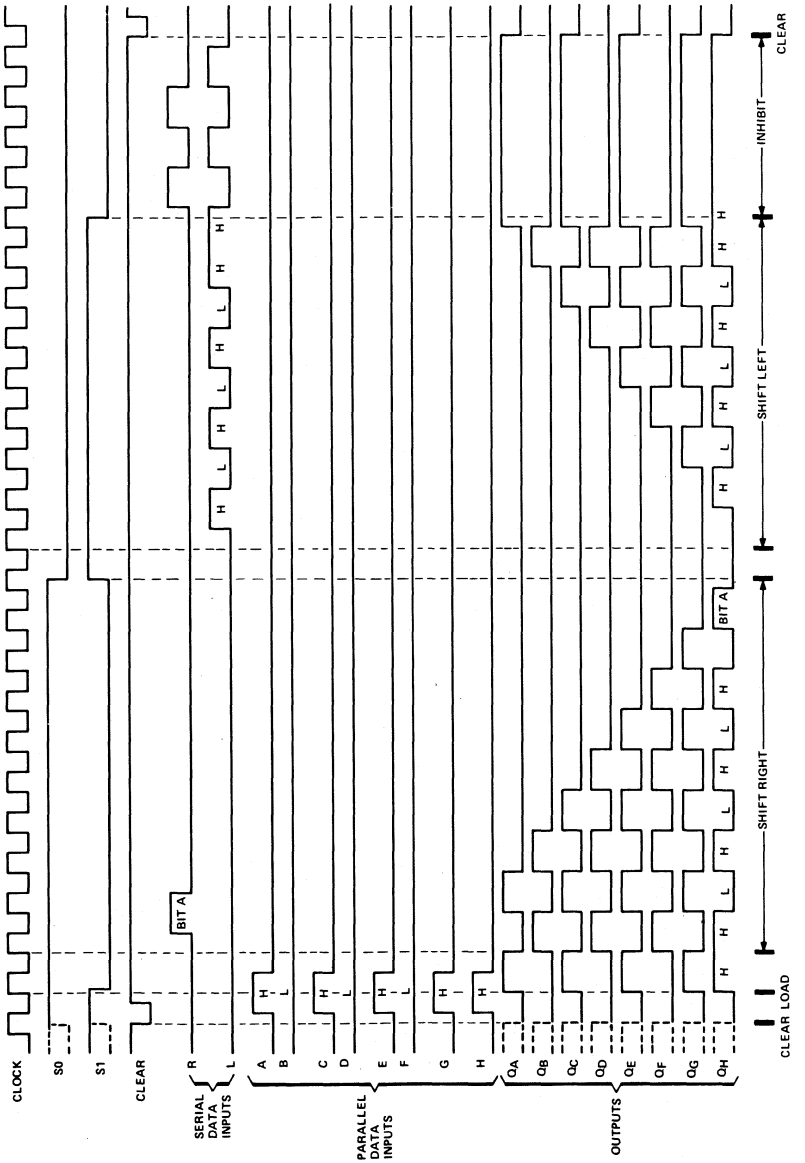
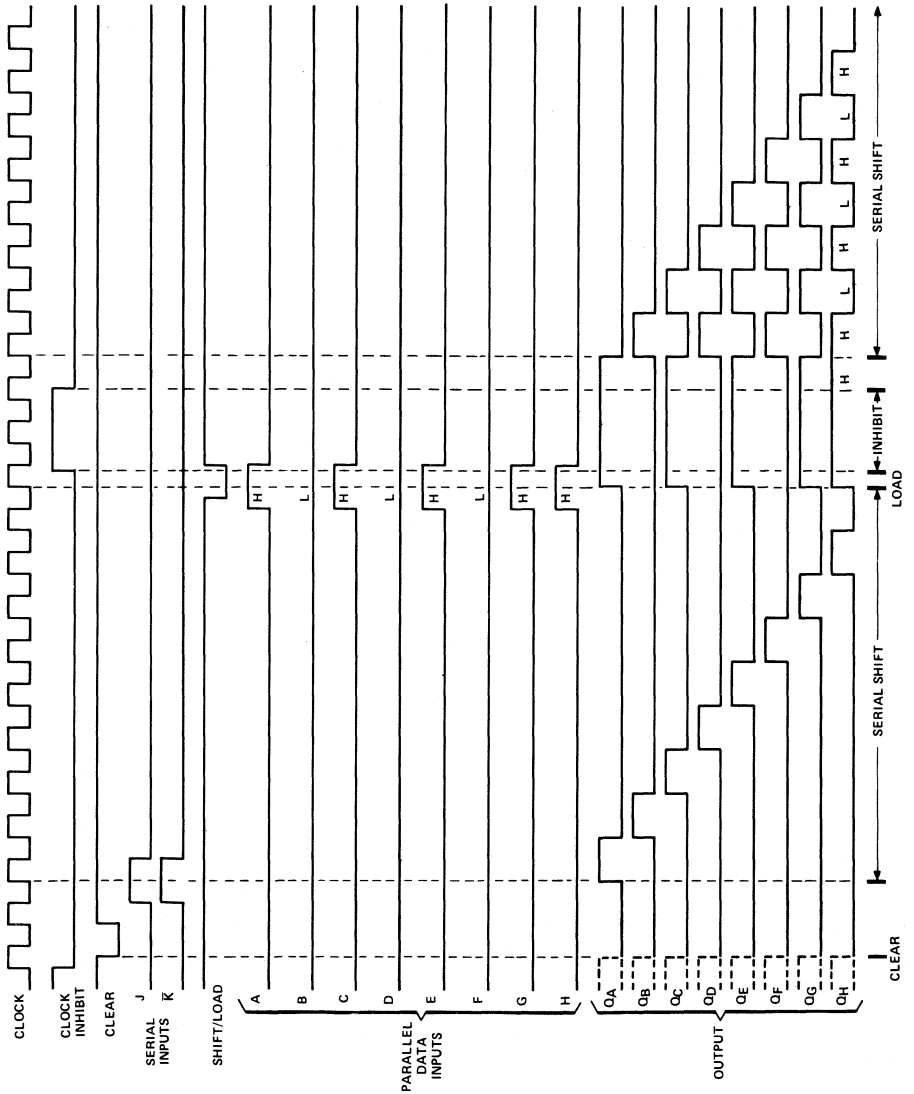
SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



SN54199, SN74199

typical clear, shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54198 SN54199			SN74198 SN74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{su}	30			30			ns
Data setup time, t_{su} (see Figure 1)	20			20			ns
Hold time at any input, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54198 SN54199			SN74198 SN74199			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		90	127		90	127	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock inhibit, Clear, Shift/Load

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	26	ns

PARAMETER MEASUREMENT INFORMATION

SN54198, SN74198

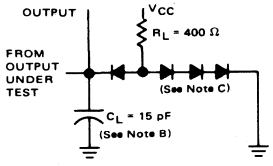
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

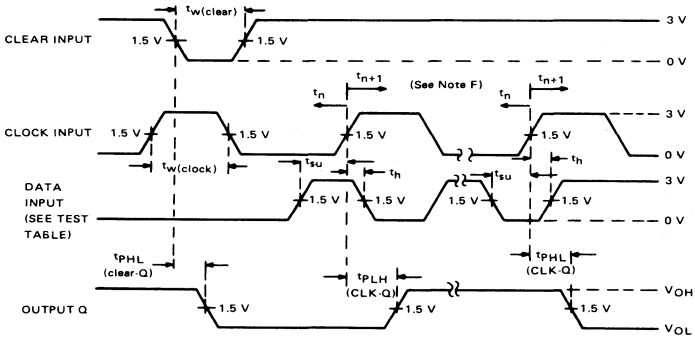
SN54199, SN74199

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{K}$	4.5 V	Q_H at t_{n+8}



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

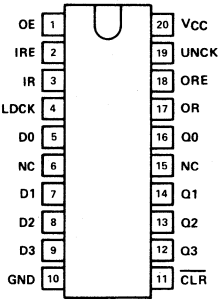
FIGURE 1

TYPES SN54LS222, SN54LS224, SN54LS227, SN54LS228, SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 ASYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

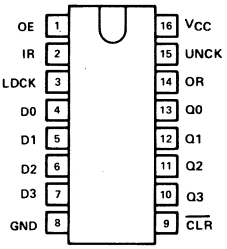
D2616, JANUARY 1981

- Independent Asynchronous Inputs and Outputs
- 16 Words of 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates from 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Optimum PC Board Layout
- Expandable Using External Gating

SN54LS222, SN54LS227 . . . J PACKAGE
SN74LS222, SN74LS227 . . . J OR N PACKAGE
(TOP VIEW)



SN54LS224, SN54LS228 . . . J PACKAGE
SN74LS224, SN74LS228 . . . J OR N PACKAGE
(TOP VIEW)



NC = No internal connection

description

These 64-bit memories are Low-Power Schottky memory arrays organized as 16 words of 4 bits each. They can be expanded in multiples of 15m+1 words or 4n bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) but some external gating is required (see Figure 1). For longer words using the 'LS224 or 'LS228, the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

TYPE	INPUT-READY ENABLE AND OUTPUT-READY ENABLE	OUTPUT
'LS222	Yes	3-State
'LS224	No	3-State
'LS227	Yes	Open-collector
'LS228	No	Open-collector

operation

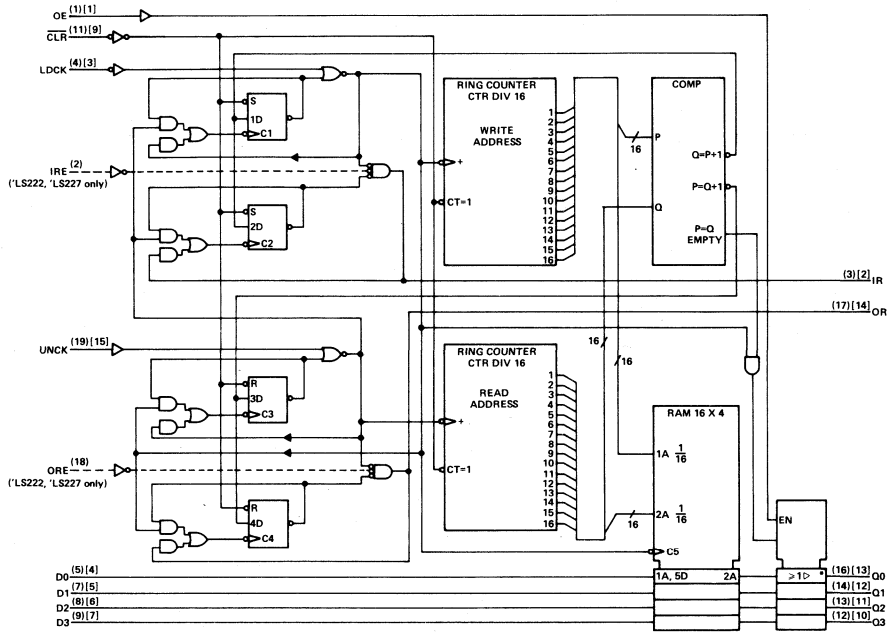
A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFO's are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word. Data is written into the memory on a high-to-low transition at the load clock input (LDCK) and read out on a low-to-high transition at the unload clock input (UNCK).

The memory is full when the number of words clocked in exceeds the number of words clocked out by 16. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory (see timing diagram) is monitored by the input ready (IR) and output ready (OR) flags that indicate "not full" and "not empty" conditions. The IR output will be high only when the memory is not full and the LDCK input is low. The OR output will be high only when the memory is not empty and UNCK is high.

A high-to-low transition at the clear ($\overline{CLR}$) input resets the internal stack control counters and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when output enable (OE) is low. OE does not affect the IR and OR outputs.

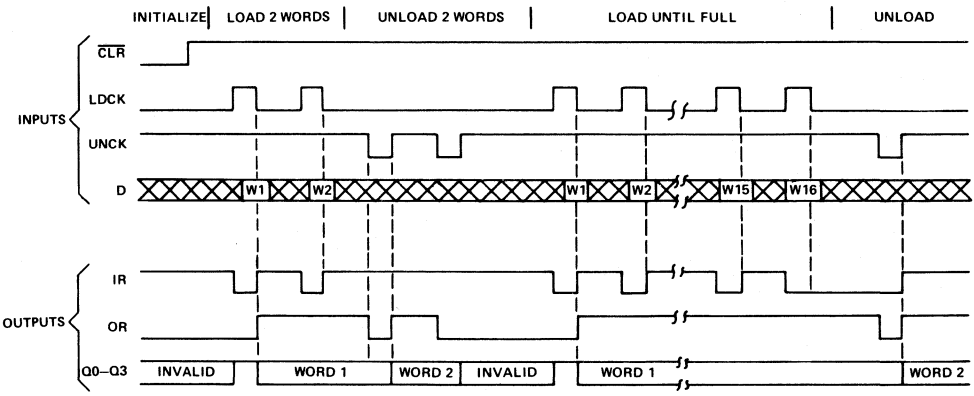
functional block diagram (positive logic)



*'LS222 and 'LS224 have 3-state (▽) outputs.
'LS227 and 'LS228 have open-collector (◇) outputs.

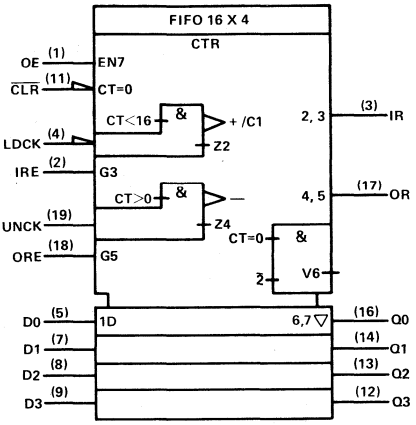
('LS222 and 'LS227 pin numbers)
['LS224 and 'LS228 pin numbers]

timing diagram

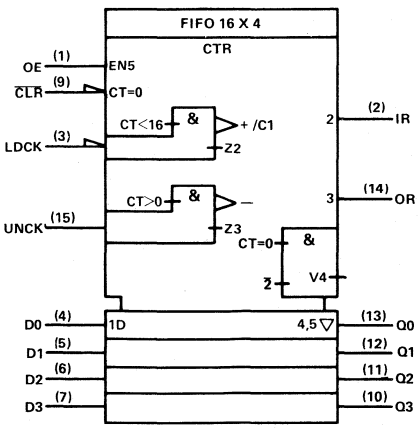


logic symbols

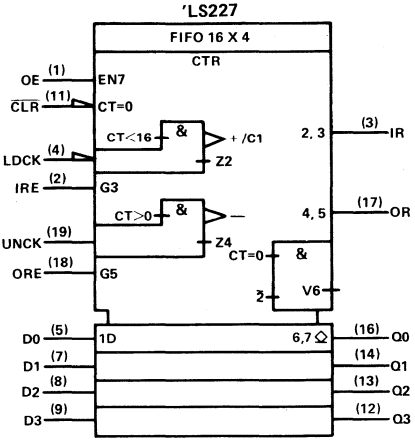
'LS222



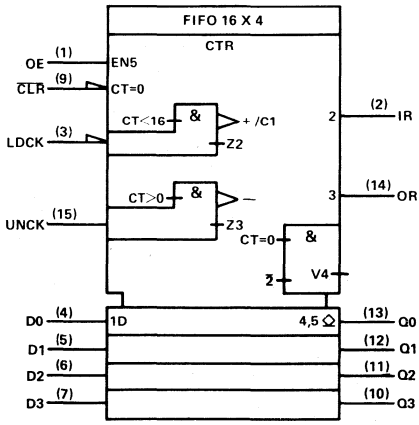
'LS224



'LS227



'LS228



These symbols are functionally accurate but do not show the details of implementation; for these, see the functional block diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at that time. Output data is invalid when the counter content is 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)		7 V
Input voltage:		7 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54LS222, SN54LS224, SN54LS227, SN54LS228	−55°C to 125°C
	SN74LS222, SN74LS224, SN74LS227, SN74LS228	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q			−1			−2.6	mA
	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C
	LDCK ↓	60			60			ns
Pulse width Tw	UNCK ↑	30			30			ns
	CLR	20			20			ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		IR, OR	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL} max	I_{OL} = 24 mA					0.35	0.5	
		IR, OR		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q	V_{IL} = V_{IL} max	V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit current§	Q	V_{CC} = MAX		−30		−130	−30		−130	mA
		IR, OR			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84	135		84	135	mA
				Outputs low		87	155		87	155	
				Outputs disabled		89	155		89	155	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

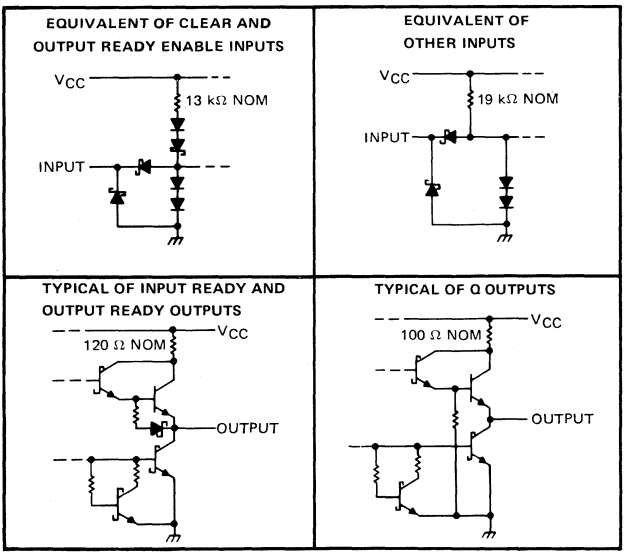
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS222			'LS224			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE↑	IR	R_L = 2 kΩ, C_L = 15 pF, See Note 2		21	35				ns
t_{PHL}	IRE↓	IR			10	15				ns
t_{PLH}	ORE↑	OR			21	35				ns
t_{PHL}	ORE↓	OR			10	15				ns
t_{PLH}	LDCK↓	IR			25	40		25	40	ns
t_{PHL}	LDCK↑	IR			31	50		31	50	ns
t_{PLH}	LDCK↓	OR			45	70		45	70	ns
t_{PLH}	UNCK↑	OR			28	45		28	15	ns
t_{PHL}	UNCK↓	OR			26	45		26	45	ns
t_{PLH}	UNCK↑	IR			45	70		45	70	ns
t_{PLH}	$\overline{CLR}$↓	IR			33	55		33	55	ns
t_{PHL}	$\overline{CLR}$↓	OR			23	40		23	40	ns
t_{PLH}	LDCK↓	Q	R_L = 667 Ω, C_L = 45 pF, See Note 2		45			45		ns
t_{PHL}	LDCK↓	Q			34	50		34	50	ns
t_{PLH}	UNCK↑	Q			48	80		48	80	ns
t_{PHL}	UNCK↑	Q			46	70		46	70	ns
t_{PZL}	OE↑	Q			23	35		23	35	ns
t_{PZH}	OE↑	Q			21	35		21	35	ns
t_{PLZ}	OE↓	Q	R_L = 667 Ω, C_L = 5 pF, See Note 2		15	30		15	30	ns
t_{PHZ}	OE↓	Q			22	30		22	30	ns

NOTE 2: For load circuits and voltage waveforms, see page 3-11

7

schematics of inputs and outputs



recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q			5.5			5.5	V
High-level output current, I_{OH}	IR, OR			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	IR, OR			4			8	
Setup time, t_{su}	D to LDCK ↓	50			50			ns
Hold time, t_h	D from LDCK↓	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C
	LDCK ↓	60			60			ns
Pulse width Tw	UNCK ↑	30			30			ns
	CLR	20			20			ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	IR, OR	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −400 μA, V_{IL} = V_{IL} max		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V, V_{IL} = V_{IL} max				100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		IR, OR		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	IR, OR	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		84			84	135	mA
				Outputs low		87			87	155	
				Outputs disabled		89			89	155	

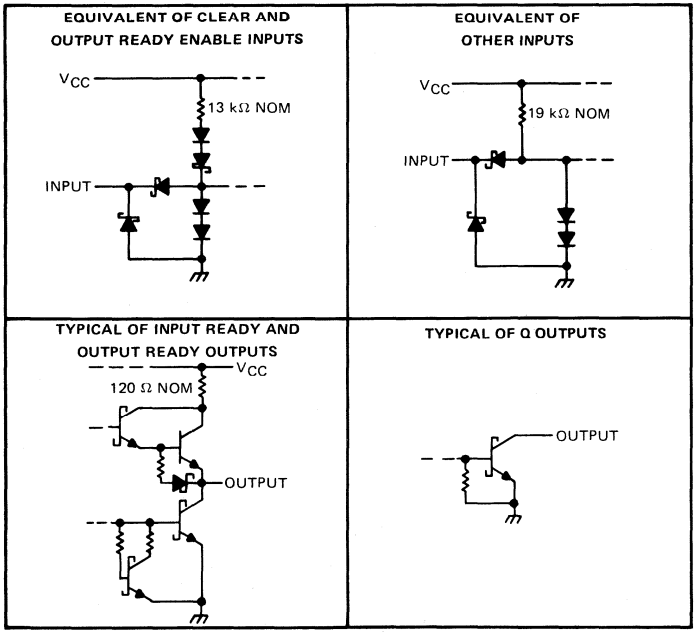
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	TEST CONDITIONS	'LS227			'LS228			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE ↑	IR			23	35				ns
t_{PHL}	IRE ↓	IR			10	15				ns
t_{PLH}	ORE ↑	OR			23	35				ns
t_{PHL}	ORE ↓	OR			10	15				ns
t_{PLH}	LDCK ↓	IR	R_L = 2 kΩ,		27	40		27	40	ns
t_{PHL}	LDCK ↑	IR	C_L = 15 pF,		32	50		32	50	ns
t_{PLH}	LDCK ↓	OR	See Note 2		52	70		52	70	ns
t_{PLH}	UNCK ↑	OR			31	45		31	45	ns
t_{PHL}	UNCK ↓	OR			26	45		26	45	ns
t_{PLH}	UNCK ↑	IR			49	70		49	70	ns
t_{PLH}	$\overline{CLR}$ ↓	IR			36	55		36	55	ns
t_{PHL}	$\overline{CLR}$ ↓	OR			24	40		24	40	ns
t_{PLH}	LDCK ↓	Q			54			54		ns
t_{PHL}	LDCK ↓	Q			41	50		41	50	ns
t_{PLH}	UNCK ↑	Q	R_L = 667 Ω,		62	80		62	80	ns
t_{PHL}	UNCK ↑	Q	C_L = 45 pF,		53	70		53	71	ns
t_{PLH}	OE ↓	Q	See Note 2		23	30		23	30	ns
t_{PHL}	OE ↑	Q			25	35		25	35	ns

NOTE 2: For load circuits and voltage waveforms, see page 3-11.

schematics of inputs and outputs



TYPICAL APPLICATIONS INFORMATION

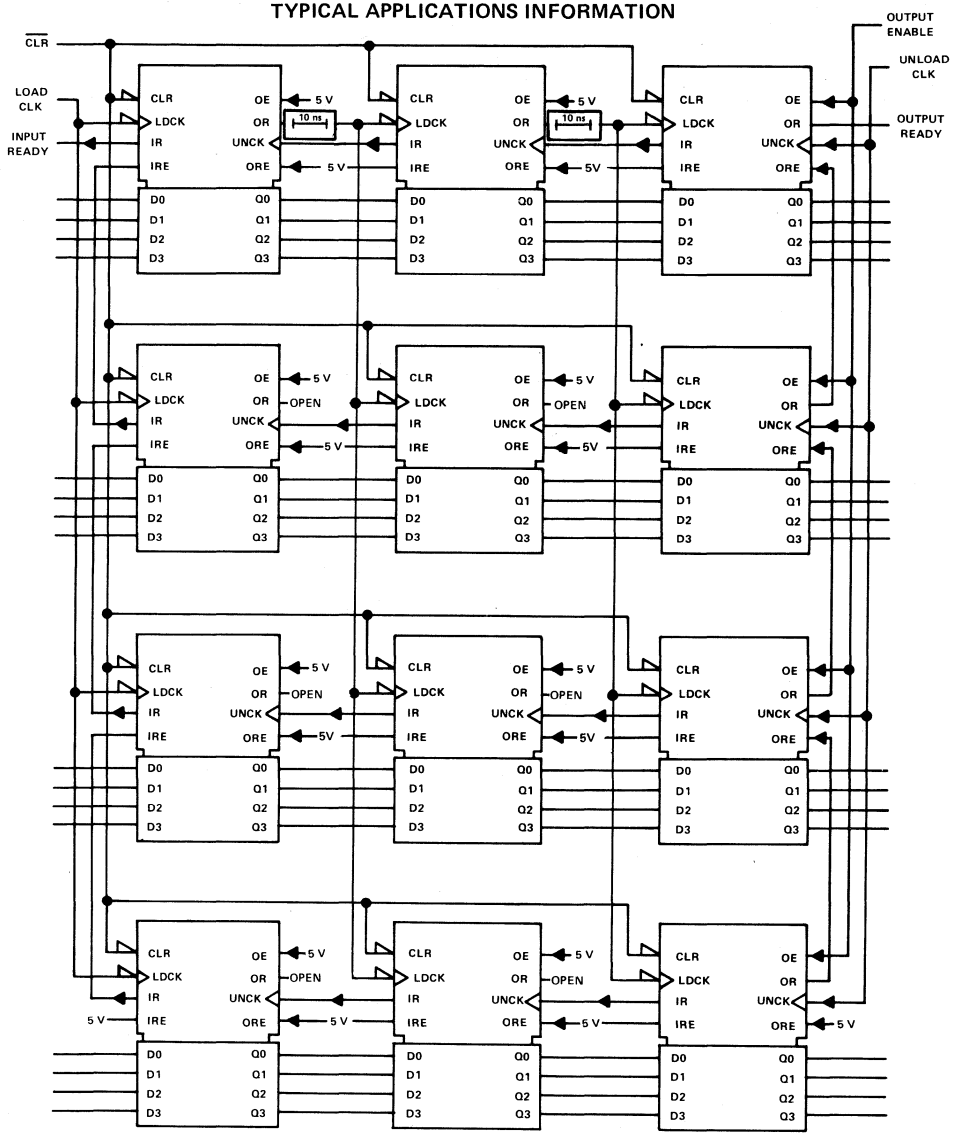


FIGURE 1–46-WORD BY 16-BIT EXPANSION USING 'LS222

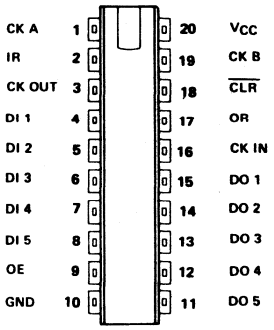
10 ns ≡ Noninverting delay ≥ 10 ns (e.g., 2 stages of 'LS04), 2 places.

TYPE SN74S225
16 x 5 ASYNCHRONOUS FIRST-IN/FIRST-OUT MEMORY

SEPTEMBER 1976 – REVISED JUNE 1979

- **Independent Synchronous Inputs and Outputs**
- **Organized as 16-Words of 5 Bits**
- **DC to 10-MHz Data Rate**
- **3-State Data Outputs**
- **20-Pin, 300-mil, High-Density Package**

SN74S225 . . . J OR N PACKAGE
(TOP VIEW)



Pin assignments are same for all packages

description

This 80-bit active-element memory is a monolithic Schottky-clamped tansistor-transistor logic (STTL) array organized as 16 words of five-bits each. A memory system using the SN74S225 can easily be expanded in multiples of 16 words or of 5 bits as shown in Figure 2. The three-state outputs controlled by a single enable, OE, make bus connection and multiplexing easy.

operation

A FIFO is a memory storage device which allows data to be written into and/or read from its array at independent data rates. The 'S225 is a FIFO which will process data at any desired clock rate from DC to 10 MHz. The data is processed in a parallel format, word by word.

Reading or writing is done independently utilizing separate synchronous data clocks. Data may be written into the array on the low-to-high transition of either load clock input. Data may be read out of the array on the low-to-high transition of the unload clock input (normally high). When writing data into the FIFO one of the load clock inputs must be held high while the other strobes in the data. This arrangement allows either load clock to function as an inhibit for the other.

Status of the 'S225 is provided by three outputs. Input ready monitors the status of the last word location and signifies when the memory is full. This output is high whenever the memory is available to accept any data. The unload clock output also monitors the last word location. This output generates a low-logic-level pulse (synchronized to the internal clock pulse) when the location is vacant. The third status output, output ready, is high when the first word location contains valid data and unload clock input is high. When unload clock input is low, output ready will be low. The first word location is defined as the location from which data is provided to the outputs.

The data outputs are noninverted with respect to the data inputs and are three-state with a common control input, output enable. When output enable is low, the data outputs are enabled to function as totem-pole outputs. A high-logic-level forces each data output to a high-impedance state while all other inputs and outputs remain active.

The clear input invalidates all data stored in the memory array by clearing the control logic and setting output ready to a low-logic-level on the high-to-low transition of a low-active pulse. The data outputs do not change as a result of the clear input; however, the output ready at a low-logic-level signifies invalid data.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

FUNCTION TABLES

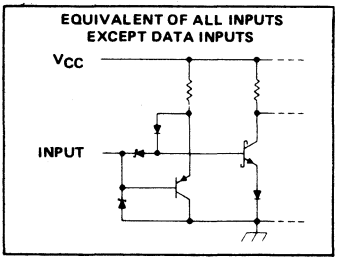
Table 1 – Input Functions

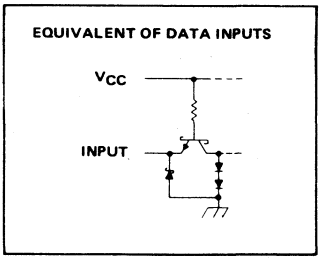
Input	Pin	Description
CK A	1	Load Clock A
DI 1 - DI 5	4-8	Data Inputs
$\overline{OE}$	9	Output Enable
CK IN	16	Unload Clock Input
$\overline{CLR}$	18	Clear
CK B	19	Load Clock B
GND	10	Ground pin
V_{CC}	20	Supply Voltage

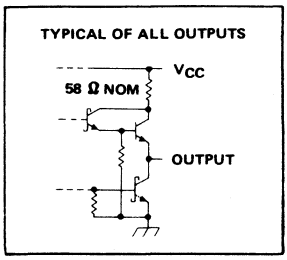
Table 2 – Output Functions

Output	Pin	Description
IR	2	Input Ready
CK OUT	3	Unload Clock Output
DO 5-DO 1	11 - 15	Data Outputs
OR	17	Output Ready

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (see Note 1) . . . . . 7 V
Input Voltage . . . . . 5.5 V
Off-State Output Voltage . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . – 65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	All Outputs Except Data			–3.2	mA
	Data Outputs			–6.5	
Low-level output current, I_{OL}	All Outputs Except Data			8	mA
	Data Outputs			16	
Pulse Width	Load Clock A or B, t_w (high)	25			ns
	Unload Clock Input, t_w (low)	7			
	Clear, t_w (low)	40			
Setup Time	Data to Load Clock, t_{su} (DIi) See Note 2	–20↑			ns
	Clear Release to Load Clock, t_{su}	25↑			
Hold Time Data from Load Clock, t_h(DIi)		70↑			ns
Operating free-air temperature, T_A		0		70	C

NOTE 2: Data must be setup within 15 ns after the load clock positive transition.
↑ = The arrow indicates that the low-to-high transition of the load clock is used for reference.

7

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = 18 mA			–1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	2.9		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX		0.35	0.50	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_O = 0.5 V			–50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Data In	V_{CC} = MAX, V_I = 2.7 V			40	μA
		All Inputs Except Data In				25	
I_{IL}	Low-level input current	Data In	V_{CC} = MAX, V_I = 0.5 V			–1	mA
		All Inputs Except Data In				–250	μA
I_{OS}	Short-circuit output current §		V_{CC} = MAX	–30		–100	mA
I_{CC}	Supply Current		V_{CC} = MAX, See Note 3		80	120	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Duration of the short circuit should not exceed one second.
NOTE 3: I_{CC} is measured with all inputs grounded and the output open.

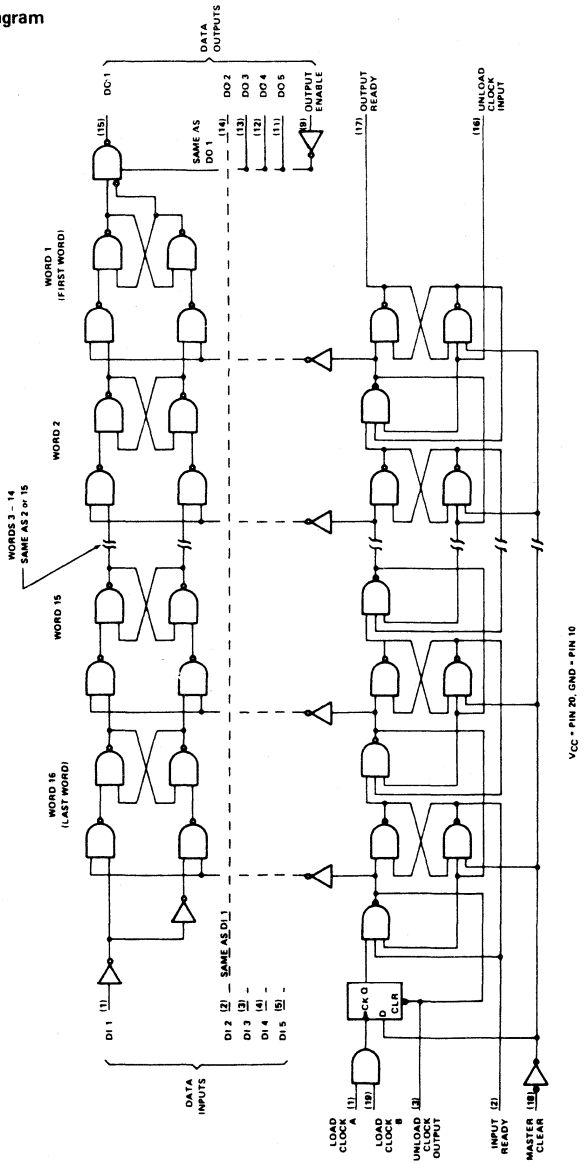
switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETERS△	FROM	TO	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
f_{max}	CK A		C_L = 30 pF, R_L = 300 Ω, See Note 4	10	20		MHz
f_{max}	CK B			10	20		MHz
f_{max}	CK IN			10	20		MHz
t_w	CK OUT			7	14		ns
t_{PXZ}	$\overline{OE}$	DOi	C_L = 5 pF		10	25	ns
t_{PZX}			C_L = 30 pF, R_L = 300 Ω, See Note 4		25	40	
t_{PLH}	CK IN	DOi			50	75	ns
t_{PHL}					50	75	
t_{PLH}	CK A or CK B	OR			190	300	ns
t_{PLH}	CK IN	OR			40	60	ns
t_{PHL}					30	45	
t_{PHL}	$\overline{CLR}$	OR			35	60	ns
t_{PHL}	CK A or CK B	CK OUT			25	50	ns
t_{PHL}	CK IN	CK OUT			270	400	ns
t_{PHL}	CK A or CK B	IR			55	75	ns
t_{PLH}	CK IN	IR			255	400	ns
t_{PLH}	$\overline{CLR}$	IR			16	35	ns
t_{PLH}	OR↑	DOi			10	20	ns

△ f_{max} ≡ maximum clock frequency.
t_w ≡ pulse width (output)
↑ ↓ ≡ The arrow indicates that the low-to-high (↑) or high-to-low (↓) transition of the output ready (OR) output is used for reference.
t_{PLH} ≡ propagation delay time, low-to-high level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 4: Load circuit and voltage waveforms are shown on page 1-14.

functional block diagram



TYPICAL WAVEFORMS FOR A 16-WORD FIFO

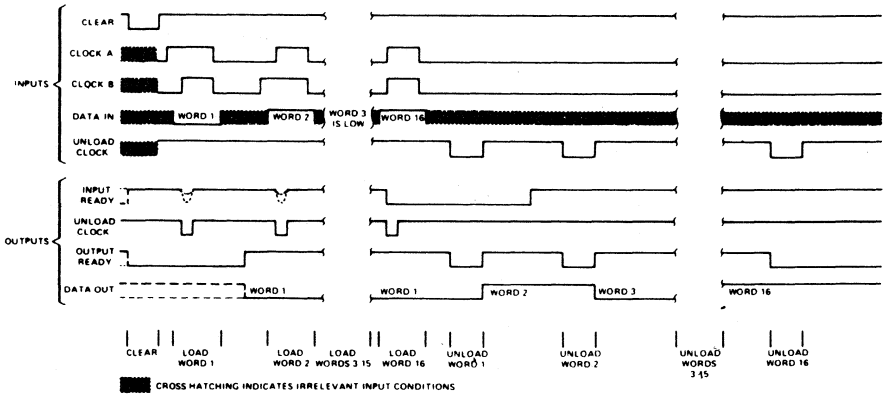


FIGURE 1 – TYPICAL WAVEFORMS FOR A 16-WORD FIFO

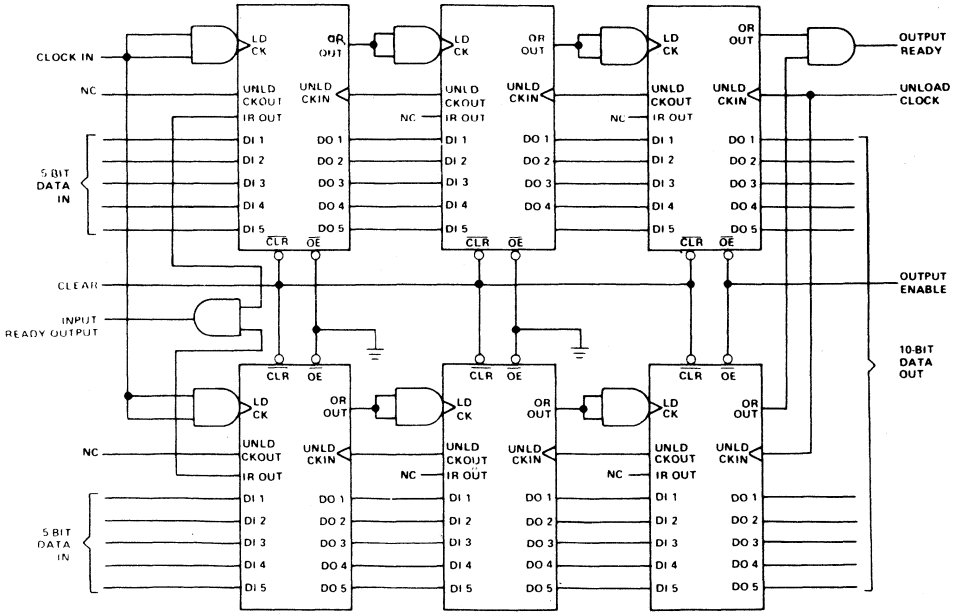


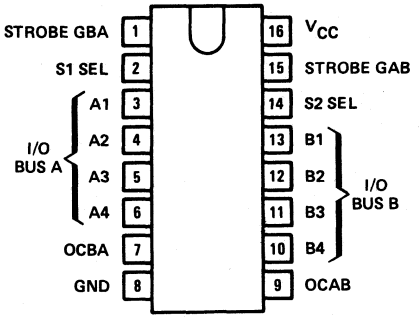
FIGURE 2 – EXPANDING THE 'S225 FIFO (48 WORDS OF 10 BITS SHOWN)

TYPES SN54S226, SN74S226
4-BIT PARALLEL LATCHED BUS TRANSCEIVERS

BULLETIN NO. DL-S 12477, OCTOBER 1976—REVISED AUGUST 1979

- Universal Transceivers for Implementing System Bus Controllers
- Dual-Rank 4-Bit Transparent Latches Provide:
  - Exchange of Data Between 2 Buses In One Clock Pulse
  - Bus-to-Bus Isolation
  - Rapid Data Transfer
  - Full Storage Capability
- Hysteresis at Data Inputs Enhances Noise Rejection
- Separate Output-Control Inputs Provide Independent Enable/Disable for Either Bus Output
- 3-State Outputs Drive Bus Lines Directly

SN54S226 . . . J PACKAGE
SN74S226 . . . J OR N PACKAGE
(TOP VIEW)



description

These high-performance Schottky† TTL quadruple bus transceivers employ dual-rank bidirectional four-bit transparent latches and feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The bus-management functions implemented and the high-impedance controls offered provide the designer with a controller/transceiver that interfaces and drives system bus-organized lines directly. They are particularly attractive for implementing:

Bidirectional bus transceivers
Data-bus controllers

The bus-management functions, under control of the function-select (S1, S2) inputs, provide complete data integrity for each of the four modes described in the function table. Directional transparency provides for routing data from or to either bus, and the dual store and dual readout capabilities can be used to perform the exchange of data between the two bus lines in the equivalent of a single clock pulse. Storage of data is accomplished by selecting the latch function, setting up the data, and taking the appropriate strobe input low. As long as the strobe is held high, the data is latched for the selected function. Further control is offered through the availability of independent output controls that can be used to enable or disable the outputs as shown in the output-control function table, regardless of the latch function in process. Store operations can be performed with the outputs disabled to a high impedance (Hi-Z). In the Hi-Z state the inputs/outputs neither load nor drive the bus lines significantly. The p-n-p inputs feature typically 400 millivolts of hysteresis to enhance noise rejection.

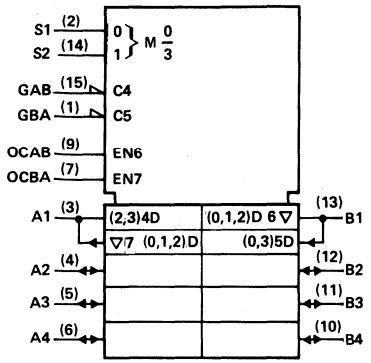
BUS-MANAGEMENT FUNCTION TABLE

MODE CONTROLS		STROBES		A-TO-B LATCHES		B-TO-A LATCHES		OPERATION
S2	S1	GAB	GBA	1	2	1	2	
L	L	X	L	Latch	Trans	Trans	Trans	Pass B to A
			H			Latch	Trans	Read out stored data
L	H	X	X	Latch	Trans	Latch	Trans	Read out stored data
H	L	L	X	Trans	Trans	Latch	Trans	Pass A to B
		H		Latch	Trans			Read out stored data
H	H	L	L	Trans	Latch	Trans	Latch	Read in both buses
		H	H	Latch	Latch	Latch	Latch	Store bus data

H = high level L = low level X = irrelevant Latch = latched Trans = transparent

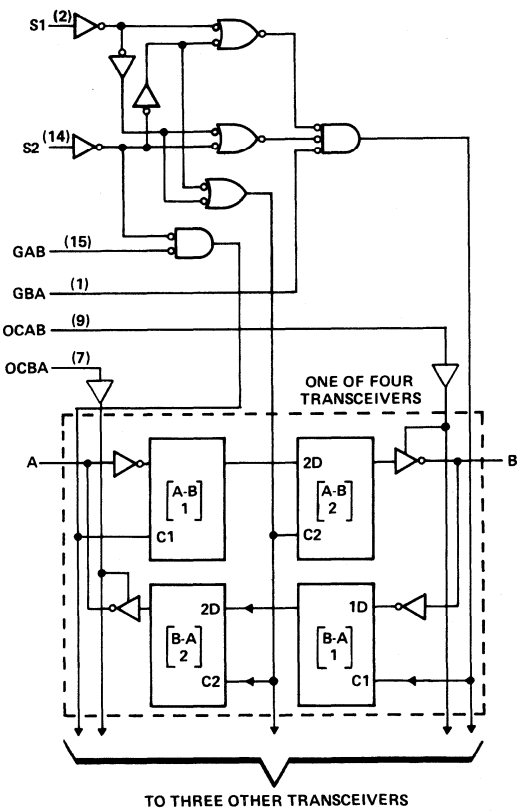
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S226 (see Note 2)	−55°C to 125°C
SN74S226	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.

recommended operating conditions

		SN54S226			SN74S226			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−6.5			−10.3	mA
Width of strobe pulse		30			20			ns
Setup time, t_{su}	To Strobe	30↑			20↑			ns
	To Select	30			20			
Hold time, t_h	To Strobe	0↑			0↑			ns
	To Select	0			0			
Operating free-air temperature, T_A (see Note 2)		−55		125	0		70	°C

↑ The arrow indicates that the low-to-high transition of the strobe input is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S226	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.3		V
		SN74S226	V_{IL} = 0.8 V, I_{OH} = MAX	2.4	2.9		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 15 mA			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V			100	μA
I_{IL}	Low-level input current	OCAB, OCBA	V_{CC} = MAX, V_I = 0.5 V			−0.38	mA
		All other inputs				−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−50		−180	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		125	185	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 2. An SN54S226 in the J package operating at temperatures above 113°C requires a heat-sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 48°C/W.
3. I_{CC} is measured with all inputs (and outputs) grounded.

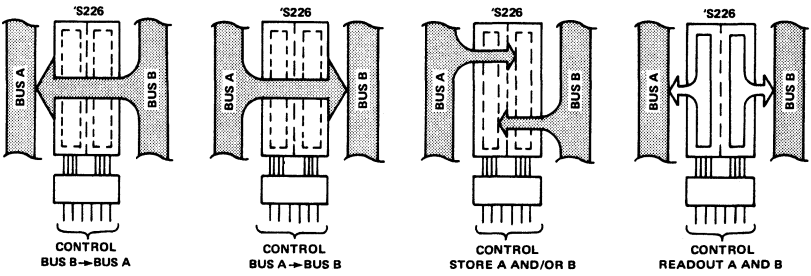
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A	C_L = 50 pF, R_L = 280 Ω, See Note 4		20	30	ns
t_{PHL}					15	30	
t_{PLH}	Select	Any			25	37	ns
t_{PHL}					19	30	
t_{PLH}	Strobe GBA or GAB	A or B			25	37	ns
t_{PHL}					19	30	
t_{PZH}	Output Control OCBA or OCAB	A or B			12	20	ns
t_{PZL}					12	20	
t_{PHZ}	Output Control OCBA or OCAB	A or B	C_L = 5 pF, R_L = 280 Ω, See Note 4		10	15	ns
t_{PLZ}					10	15	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low level
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 4: Load circuits and voltage waveforms are shown on page 3-11.

applications

The following examples demonstrate four fundamental bus-management functions that can be performed with the 'S226. Exchange of data on the two bus lines can be accomplished with a single high-to-low transition at S2 when S1 is high.

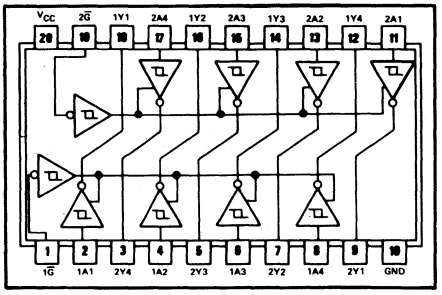


TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

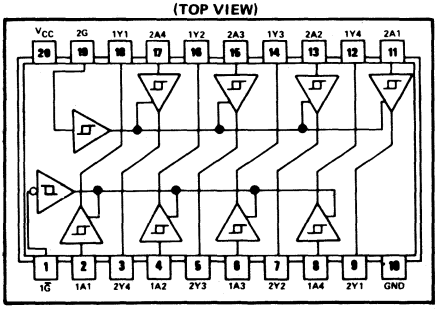
	Typical I_{OL} (Sink Current)	Typical I_{OH} (Source Current)	Typical Propagation Delay Times		Typical Enable/ Disable Times	Typical Power Dissipation (Enabled)	
			Inverting	Noninverting		Inverting	Noninverting
SN54LS'	12 mA	−12 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN74LS'	24 mA	−15 mA	10.5 ns	12 ns	18 ns	130 mW	135 mW
SN54S'	48 mA	−12 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW
SN74S'	64 mA	−15 mA	4.5 ns	6 ns	9 ns	450 mW	538 mW

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **P-N-P Inputs Reduce D-C Loading**
- **Hysteresis at Inputs Improves Noise Margins**

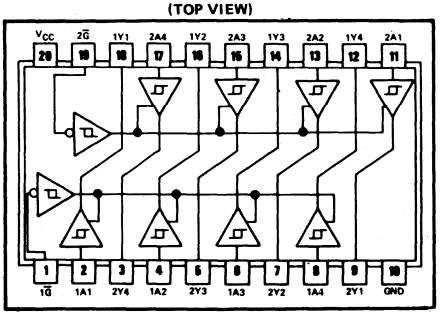
SN54LS240, SN54S240 . . . J
SN74LS240, SN74S240 . . . J OR N
(TOP VIEW)



SN54LS241, SN54S241 . . . J
SN74LS241, SN74S241 . . . J OR N
(TOP VIEW)



SN54LS244 . . . J
SN74LS244 . . . J OR N
(TOP VIEW)



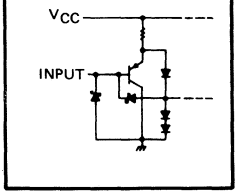
description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

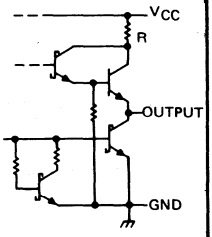
schematics of inputs and outputs

'LS240, 'LS241, 'LS244

EQUIVALENT OF EACH INPUT



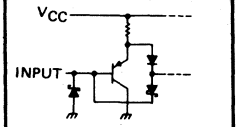
TYPICAL OF ALL OUTPUTS



'LS240, 'LS241, 'LS244;
R = 50 Ω NOM
'S240, 'S241:
R = 25 Ω NOM

'S240 'S241

EQUIVALENT OF EACH INPUT



recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	All		17	27		17	27	mA
		Outputs low		'LS240		26	44		26	44	
				'LS241, 'LS244		27	46		27	46	
		All outputs disabled		'LS240		29	50		29	50	
				'LS241, 'LS244		32	54		32	54	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS240			'LS241, 'LS244			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	18		12	18	ns
t_{PZL}	Output enable time to low level				20	30		20	30	ns
t_{PZH}	Output enable time to high level				15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		15	25	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
Operating free-air temperature, T_A (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'S240			'S241			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	SN74S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.7			2.7			V
		SN54S' and SN74S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		SN54S' and SN74S'	V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			V
			V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.55			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_I = 0.5 V			−400			−400	μA
		Any G					−2			−2	mA
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	SN54S'		80	123		95	147	mA
				SN74S'		80	135		95	160	
		Outputs low		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	
		Outputs disabled		SN54S'		100	145		120	170	
				SN74S'		100	150		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

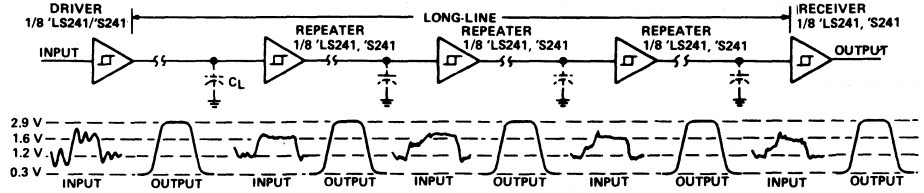
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

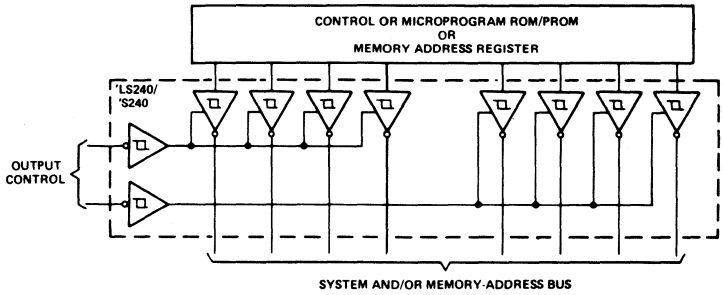
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'S240			'S241			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 4	R_L = 90 Ω,		4.5	7		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				4.5	7		6	9	ns
t_{PZL}	Output enable time to low level				10	15		10	15	ns
t_{PZH}	Output enable time to high level				6.5	10		8	12	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 4	R_L = 90 Ω,		10	15		10	15	ns
t_{PHZ}	Output disable time from high level				6	9		6	9	ns

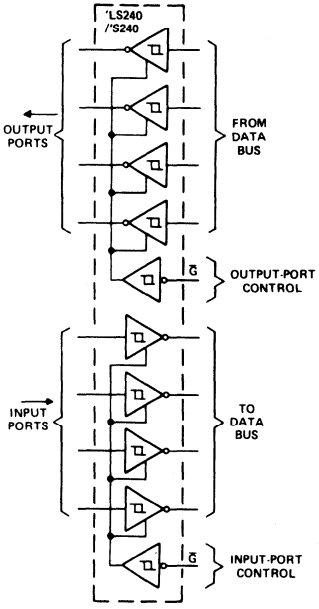
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.



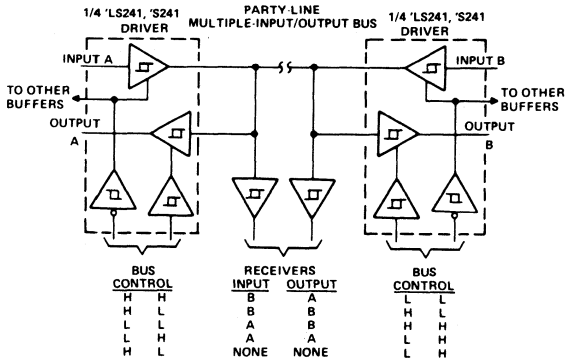
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS241, 'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

External resistance between any input of the 'S240 or 'S241 and ground or V_{CC} must not exceed 40 kΩ.

- Two-Way Asynchronous Communication Between Data Buses
- P-N-P Inputs Reduce D-C Loading
- Hysteresis (Typically 400 mV) at Inputs Improves Noise Margin

description

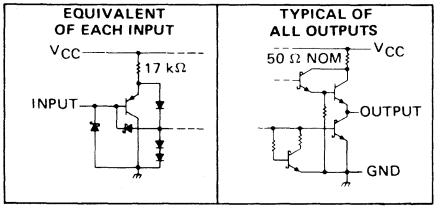
These four-data-line transceivers are designed for asynchronous two-way communications between data buses. The SN74LS' can be used to drive terminated lines down to 133 ohms.

FUNCTION TABLE (EACH TRANSCEIVER)

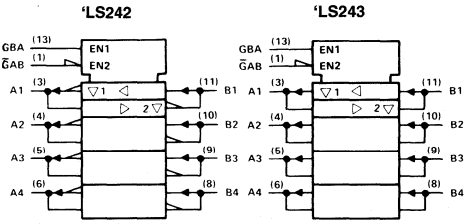
CONTROL INPUTS		'LS242 DATA PORT STATUS		'LS243 DATA PORT STATUS	
$\overline{G}AB$	GBA	A	B	A	B
H	H	$\overline{O}$	I	O	I
L	H	*	*	*	*
H	L	ISOLATED		ISOLATED	
L	L	I	$\overline{O}$	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.
I = Input, O = Output, $\overline{O}$ = Inverting Output.

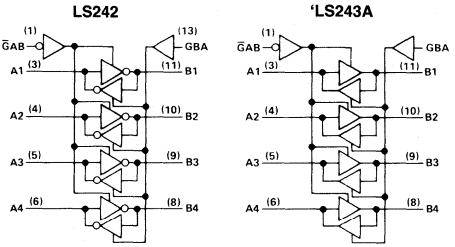
schematics of inputs and outputs



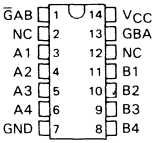
logic symbol



logic diagrams (positive logic)



SN54' . . . J PACKAGE
SN74' . . . N PACKAGE
(TOP VIEW)



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.1		2.4	3.1		V
			V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$AB or GBA		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A inputs	V_{CC} = MAX,	V_I = 0.4 V, $\overline{G}$AB and GBA at 0 V			−0.2			−0.2	mA
		B inputs	V_{CC} = MAX,	V_I = 0.4 V, $\overline{G}$AB and GBA at 4.5 V			−0.2			−0.2	
		$\overline{G}$AB or GBA	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open, See Note 2	'LS242, 'LS243		22	38		22	38	mA
		Outputs low		'LS242, 'LS243		29	50		29	50	
		All outputs disabled		'LS242		29	50		29	50	
				'LS243		32	54		32	54	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

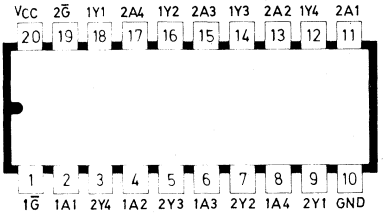
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'LS242 MIN	'LS242 TYP	'LS242 MAX	'LS243 MIN	'LS243 TYP	'LS243 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 667 Ω, See Note 3		9	14		12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18		12	18	ns
t_{PZL}	Output enable time to low level			20	30		20	30	ns
t_{PZH}	Output enable time to high level			15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Note 3		15	25		15	25	ns
t_{PHZ}	Output disable time from high level			10	18		10	18	ns

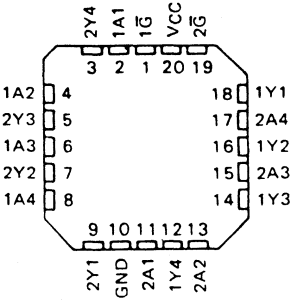
NOTE 3: Load circuit and waveforms are shown on page 3-11.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce DC Loading
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54S244 . . . J PACKAGE
SN74S244 . . . N PACKAGE
(TOP VIEW)



SN54S244 . . . FC PACKAGE
SN74244 . . . FN PACKAGE
(TOP VIEW)

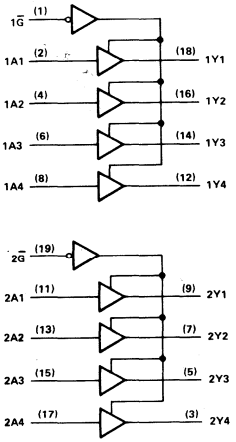


description

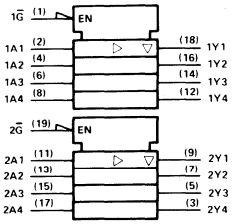
These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'ALS240, 'ALS241, 'AS240, and 'AS241, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

The SN54S244 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74S244 is characterized for operation from 0°C to 70°C.

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

recommended operating conditions

PARAMETER	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			48			64	mA
External resistance between any input or V_{CC} and ground			40			40	kΩ
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S244J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'S244			UNIT
					MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = 18 mA			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN,		0.2	0.4		V
V_{OH}	High-level output voltage	SN74S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.7			V
		SN74S' and SN54S'	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		
			V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.55	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.5 V			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current	Any A	V_{CC} = MAX,	V_I = 0.5 V			−400	μA
		Any G or $\overline{G}$					−2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−50		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	SN54S'		95	147	mA
				SN74S'		95	160	
I_{CCL}		Outputs low		SN54S'		120	170	
				SN74S'		120	180	
I_{CCZ}		Outputs disabled		SN54S'		120	170	
				SN74S'		120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C

PARAMETER		TEST CONDITIONS		'S244			UNIT
				MIN	TYP*	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, See Note 3	R_L = 90 Ω, V		6	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output				6	9	ns
t_{PZL}	Output enable time to low level				10	15	ns
t_{PZH}	Output enable time to high level				8	12	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 3	R_L = 90 Ω,		10	15	ns
t_{PHZ}	Output disable time from high level				6	9	ns

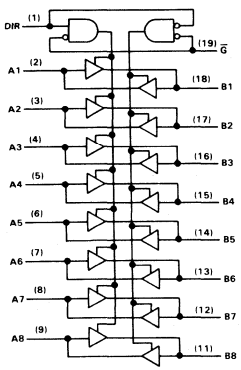
NOTE 3: Load circuit and waveforms are shown on page 3-10.

TYPES SN54LS245, SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

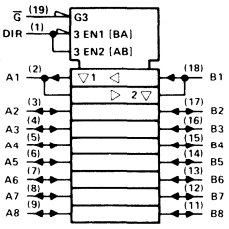
- **Bi-directional Bus Transceiver in a High-Density 20-Pin Package**
- **3-State Outputs Drive Bus Lines Directly**
- **P-N-P Inputs Reduce D-C Loading on Bus Lines**
- **Hysteresis at Bus Inputs Improve Noise Margins**
- **Typical Propagation Delay Times, Port-to-Port . . . 8 ns**
- **Typical Enable/Disable Times . . . 17 ns**

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
SN54LS245	12 mA	−12 mA
SN74LS245	24 mA	−15 mA

logic diagram (positive logic)



logic symbol



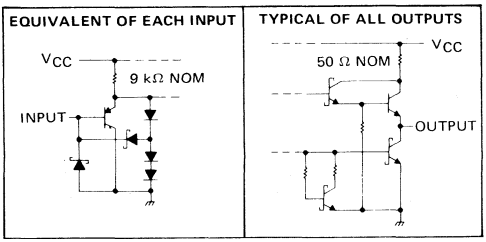
description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

The SN54LS245 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS245 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE

ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS245 . . . . . −55°C to 125°C
SN74LS245 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Off state output voltage . . . . . 5·5V

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

PARAMETER	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS245			SN74LS245			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A or B input	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{G}$ at 2 V	V_O = 2.7 V			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−200			−200	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	µA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Total, outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF,	R_L = 667 Ω,	See Note 2		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	12	ns
t_{PZL}	Output enable time to low level					27	40	ns
t_{PZH}	Output enable time to high level					25	40	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	R_L = 667 Ω,	See Note 2		15	25	ns
t_{PHZ}	Output disable time from high level					15	25	ns

NOTE 2: Load circuit and waveforms are shown on page 1-15.

TYPES SN54246 THRU SN54249, SN54LS247 THRU SN54LS249, SN74246 THRU SN74249, SN74LS247 THRU SN74LS249 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

BULLETIN NO. DL-S 7612078, MARCH 1974– REVISED OCTOBER 1976

'246, '247, 'LS247 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'248, 'LS248 feature

- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'249, 'LS249 feature

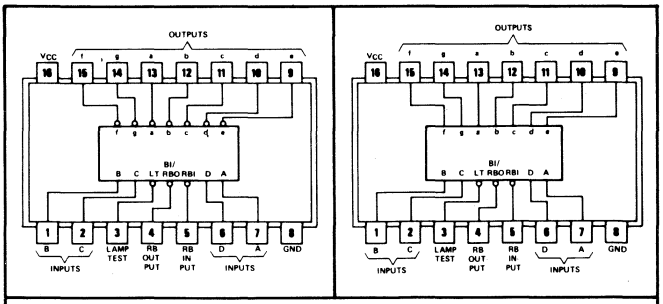
- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

- All Circuit Types Feature Lamp Intensity Modulation Capability

TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54246	low	open-collector	40 mA	30 V	320 mW	J, W
SN54247	low	open-collector	40 mA	15 V	320 mW	J, W
SN54248	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, W
SN54249	high	open-collector	10 mA	5.5 V	265 mW	J, W
SN54LS247	low	open-collector	12 mA	15 V	35 mW	J, W
SN54LS248	high	2-kΩ pull-up	2 mA	5.5 V	125 mW	J, W
SN54LS249	high	open-collector	4 mA	5.5 V	40 mW	J, W
SN74246	low	open-collector	40 mA	30 V	320 mW	J, N
SN74247	low	open-collector	40 mA	15 V	320 mW	J, N
SN74248	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW	J, N
SN74249	high	open-collector	10 mA	5.5 V	265 mW	J, N
SN74LS247	low	open-collector	24 mA	15 V	35 mW	J, N
SN74LS248	high	2-kΩ pull-up	6 mA	5.5 V	125 mW	J, N
SN74LS249	high	open-collector	8 mA	5.5 V	40 mW	J, N

'246, '247, 'LS247 (TOP VIEW)

'248, '249, 'LS248, 'LS249 (TOP VIEW)



positive logic: see function tables

description

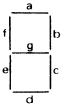
The '246 through '248 are electrically and functionally identical to the SN5446A/SN7446A, SN5447A/SN7447A, and SN5448/SN7448, respectively, and have the same pin assignments as their equivalents. Also the 'LS247 and 'LS248 are electrically and functionally identical to the SN54LS47/SN74LS47 and SN54LS48/SN74LS48, respectively, and have the same pin assignments as their equivalents. They can be used interchangeably in present or future designs to offer designers a choice between two indicator fonts. The '249 and 'LS249 are 16-pin versions of the 14-pin SN5449 and SN54LS49/SN74LS49, respectively. Included in the '249 and 'LS249 circuits is the full functional capability for lamp test and ripple blanking, which is not available in the '49 and 'LS49 circuits. The '46A, '47A, '48, '49, 'LS47, 'LS48, and 'LS49 compose the b and the q without tails and the '246 through '249 and 'LS247, 'LS248, and 'LS249

description (continued)

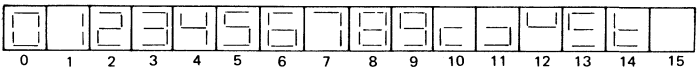
compose the 6 and the 9 with tails. Composition of all other characters, including display patterns for BCD inputs above nine, is identical. The '246, '247, and 'LS247 feature active-low outputs designed for driving indicators directly, and the '248, '249, 'LS248, and 'LS249 feature active-high outputs for driving lamp buffers. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown below. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

All of these circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS devices are characterized for operation from 0°C to 70°C.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'246, '247, 'LS247
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'248, '249, 'LS248, 'LS249
FUNCTION TABLE

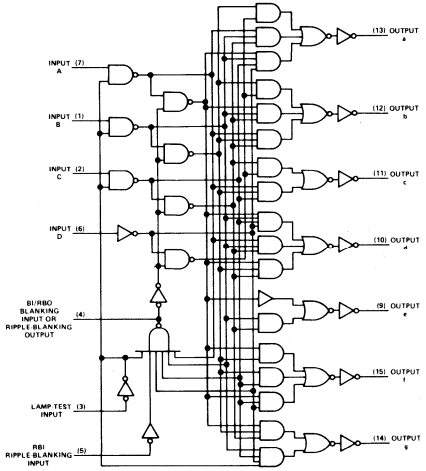
DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	1
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

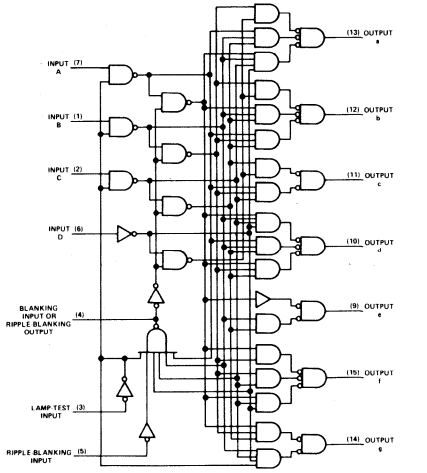
NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'246, '247, 'LS247



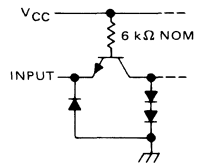
'248, '249, 'LS248, 'LS249



schematics of inputs and outputs

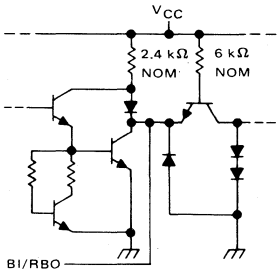
'246, '247, '248, '249

EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



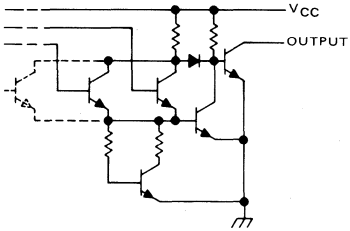
'246, '247, '248, '249

EQUIVALENT OF BI/RBO



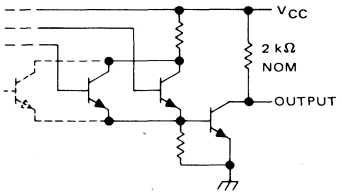
'246, '247

TYPICAL OF OUTPUTS a THRU g



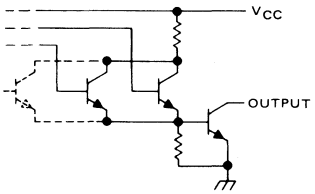
'248

TYPICAL OF OUTPUTS a THRU g



'249

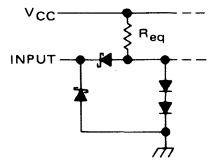
TYPICAL OF ALL OUTPUTS



schematics of inputs and outputs

'LS247, 'LS248, 'LS249

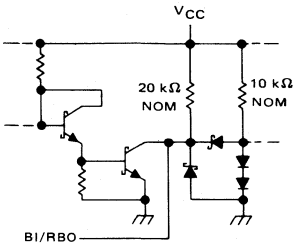
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



LT and RBI: R_{eq} = 20 kΩ NOM
A, B, C, and D: R_{eq} = 25 kΩ NOM

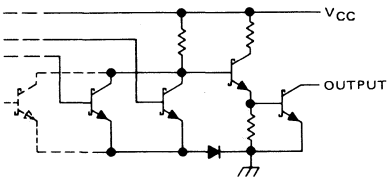
'LS247, 'LS248, 'LS249

EQUIVALENT OF BI/RBO



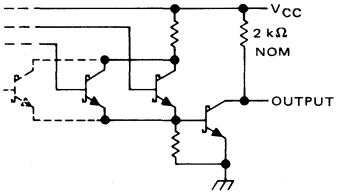
'LS247

TYPICAL OF OUTPUTS a THRU g



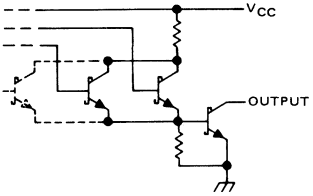
'LS248

TYPICAL OF OUTPUTS a THRU g



'LS249

TYPICAL OF OUTPUTS a THRU g



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54246, SN54247 . . . . . −55°C to 125°C
SN74246, SN74247 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54246			SN54247			SN74246			SN74247			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	BI/RBO			−200			−200			−200			−200	μA
Low-level output current, I_{OL}	BI/RBO			8			8			8			8	mA
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA	2.4	3.7		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.27	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 40 mA		0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		BI/RBO				−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX			−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		64	103	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 120 Ω, See Note 3			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS247 . . . . . −55°C to 125°C
SN74LS247 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS247			SN74LS247			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			15			15	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS247			SN74LS247			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MIN V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 15 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54248 . . . . . −55°C to 125°C
SN74248 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54248			SN74248			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			−400			−400	μA
	BI/RBO			−200			−200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V,	2.4	4.2		V
		BI/RBO	V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.7		
I_O	Output current	a thru g	V_{CC} = MIN, V_O = 0.85 V, Input conditions as for V_{OH}	−1.3	−2		mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX		0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		BI/RBO				−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX			−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		53	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 1 kΩ, See Note 5			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS248 . . . . . −55°C to 125°C
SN74LS248 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS248			SN74LS248			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			−100			−100	μA
	BI/RBO			−50			−50	
Low-level output current, I_{OL}	a thru g			2			6	mA
	BI/RBO			1.6			3.2	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS248			SN74LS248			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	a thru g and BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	2.4	4.2		2.4	4.2		V
I_O	Output current	a thru g	V_{CC} = MIN, Input conditions as for V_{OH}	V_O = 0.85 V,	−1.3	−2		−1.3	−2		mA
V_{OL}	Low-level output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 2 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 6 mA					0.35	0.5	
		BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any input except BI/BRO	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		25	38		25	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 4 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	C_L = 15 pF, R_L = 6 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 6: Load circuit and voltage waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54249 . . . . . −55°C to 125°C
SN74249 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54249			SN74249			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}	BI/RBO			−200			−200	μA
Low-level output current, I_{OL}	a thru g			10			10	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.7		V
I_{OH}	High-level output current	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX		0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		BI/RBO				−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX			−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		53	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 667 Ω, See Note 5			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Current forced into any output in the offstate . . . . . 1 mA
Operating free-air temperature range: SN54LS249 . . . . . −55°C to 125°C
SN74LS249 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS249			SN74LS249			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	a thru g			5.5			5.5	V
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	a thru g			4			8	mA
	BI/RBO			1.6			3.2	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS249			SN74LS249			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
I_{OH}	High-level output current	a thru g	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
		a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		8	15		8	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, R_L = 2 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input	C_L = 15 pF, R_L = 6 kΩ, See Note 6			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 6: Load circuit and voltage waveforms are shown on page 3-11.

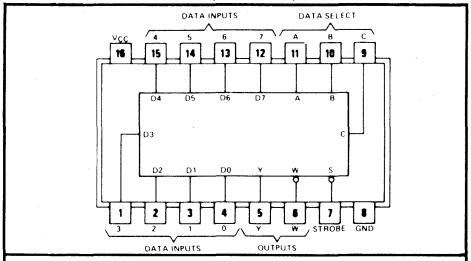
TYPES SN54251, SN54LS251, SN54S251, SN74251, SN74LS251 (TIM9905), SN74S251 DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7611834, DECEMBER 1972—REVISED OCTOBER 1976

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL and DTL Circuits

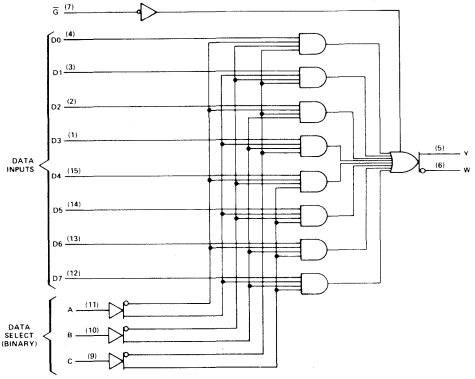
TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL AVG PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
SN54251	49	17 ns	250 mW
SN74251	129	17 ns	250 mW
SN54LS251	49	17 ns	35 mW
SN74LS251	129	17 ns	35 mW
SN54S251	39	8 ns	275 mW
SN74S251	129	8 ns	275 mW

SN54251, SN54LS251, SN54S251 . . . J OR W PACKAGE
SN74251, SN74LS251, SN54S251 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

functional block diagram



description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the 'average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54251 . . . . . −55°C to 125°C
SN74251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

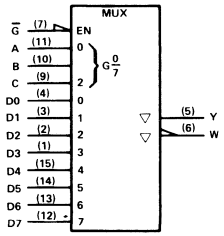
	SN54251			SN74251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−5.2	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			40	µA
			V_O = 0.4 V			−40	
V_O	Output clamp voltage	V_{CC} = MAX, V_{IH} = 4.5 V	I_O = −12 mA			−1.5	V
			I_O = 12 mA			V_{CC}+1.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open	All inputs at 4.5 V,		38	62	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

logic symbol



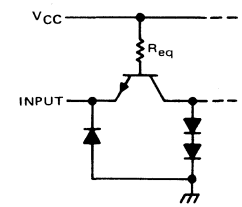
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 50 pF, R_L = 400 Ω, See Note 2		29	45	ns
t_{PHL}					28	45	
t_{PLH}	A, B, or C (3 levels)	W			20	33	ns
t_{PHL}					21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{ZH}	Strobe	Y			17	27	ns
t_{ZL}					26	40	
t_{ZH}	Strobe	W			17	27	ns
t_{ZL}					24	40	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 400 Ω, See Note 2		5	8	ns
t_{LZ}					15	23	
t_{HZ}	Strobe	W			5	8	ns
t_{LZ}					15	23	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: See load circuits and waveforms on page 3-10.

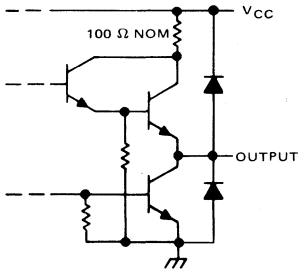
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Select: R_{eq} = 6 kΩ NOM
Other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS251 . . . . . 55°C to 125°C
SN74LS251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS251			SN74LS251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS251			SN74LS251			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	Low-level voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = VIL max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Strobe input			−0.2			−0.2	mA
						−0.4			−0.4	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	Condition A		6.1	10		6.1	10	mA
			Condition B		7.1	12		7.1	12	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:
A. Strobe grounded.
B. Strobe at 4.5 V.

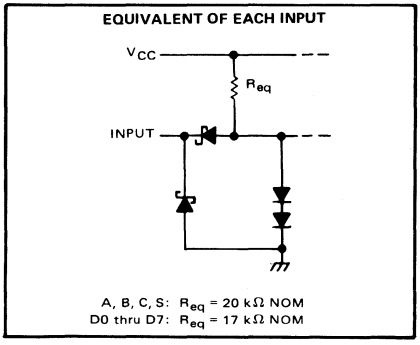
switching characteristics, V_{CC} = 5 V, T_A = 25°C

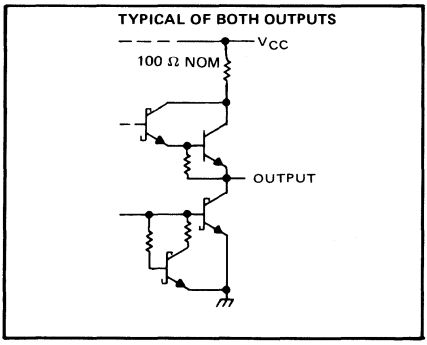
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 4		29	45	ns
t_{PHL}					28	45	
t_{PLH}	A, B, or C (3 levels)	W			20	33	ns
t_{PHL}					21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{ZH}	Strobe	Y			30	45	ns
t_{ZL}					26	40	
t_{ZH}	Strobe	W			17	27	ns
t_{ZL}					24	40	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 4		30	45	ns
t_{LZ}					15	25	
t_{HZ}	Strobe	W			37	55	ns
t_{LZ}					15	25	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level

NOTE 4: See load circuits and waveforms on page 3-11.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S251 . . . . . −55°C to 125°C
SN74S251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S251			SN74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		SN54S'	2.4	3.4		V
				SN74S'	2.4	3.2		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V				50	μA
			V_O = 0.5 V				−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open	All inputs at 4.5 V,			55	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

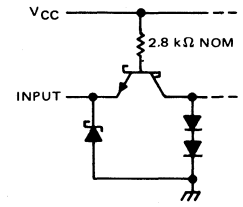
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 2		12	18	ns
t_{PHL}					13	19.5	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	
t_{ZH}	Strobe	Y	C_L = 50 pF, R_L = 280 Ω, See Note 2		13	19.5	ns
t_{ZL}					14	21	
t_{ZH}	Strobe	W			13	19.5	ns
t_{ZL}					14	21	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 280 Ω, See Note 2		5.5	8.5	ns
t_{LZ}					9	14	
t_{HZ}	Strobe	W			5.5	8.5	ns
t_{LZ}					9	14	

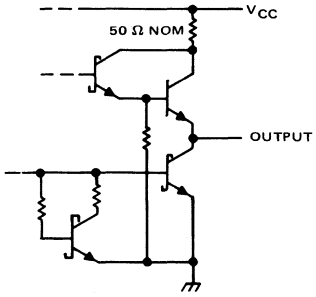
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: See load circuits and waveforms on page 3-10.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS

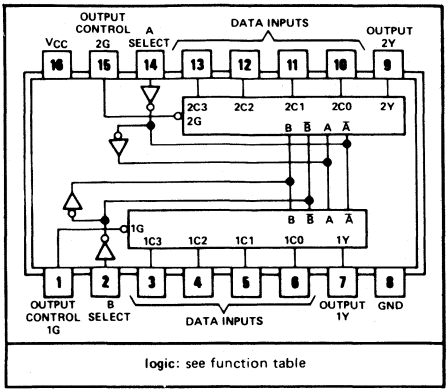


TYPES SN54LS253, SN74LS253
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7611790, SEPTEMBER 1972—REVISED OCTOBER 1976

- Three-State Version of SN54LS153/SN74LS153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
  Data Input to Output . . . 12 ns
  Control Input to Output . . . 16 ns
  Select Input to Output . . . 21 ns
- Fully Compatible with Most TTL and DTL Circuits
- Low Power Dissipation . . . 35 mW Typical (Enabled)

SN54LS253 . . . J OR W PACKAGE
SN74LS253 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

7

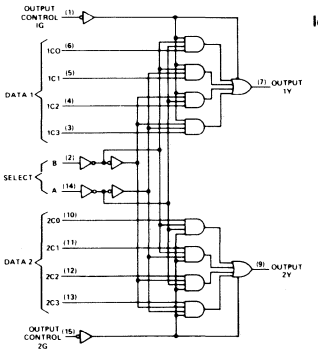
logic

FUNCTION TABLE

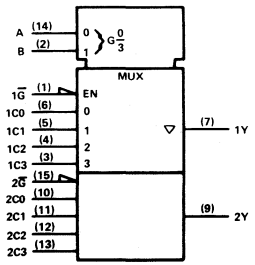
SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

functional block diagram



logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS253 . . . . . −55°C to 125°C
SN74LS253 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS253			SN74LS253			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS253			SN74LS253			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_{OZ}	Off-State (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
			G input			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Condition A		7	12		7	12	mA
			Condition B		8.5	14		8.5	14	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration for the short-circuit should exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

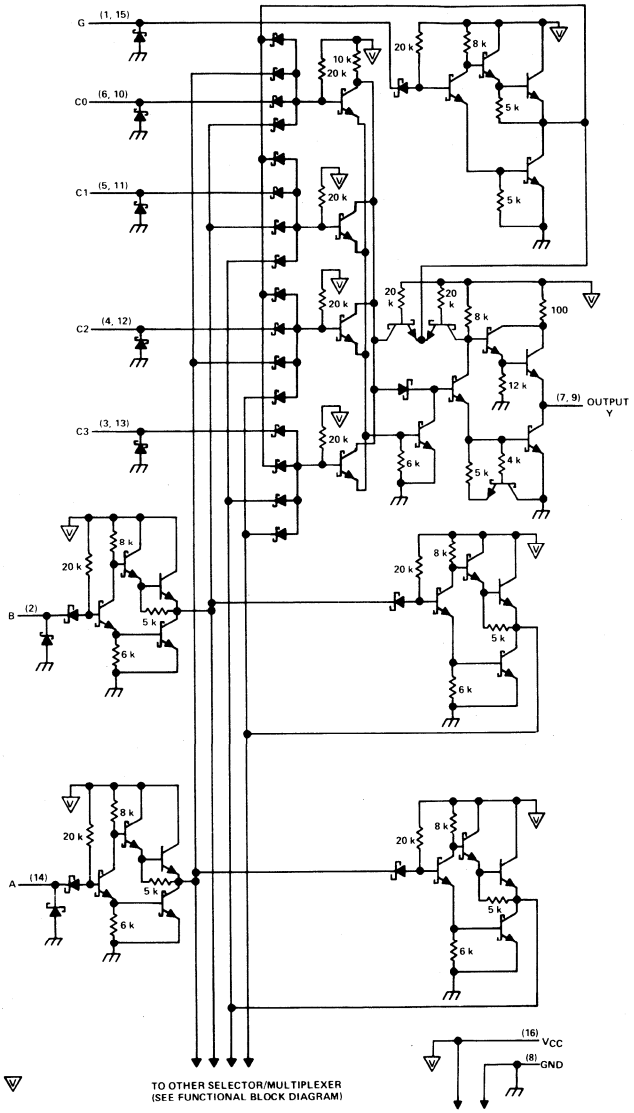
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 3		17	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			30	45	ns
t_{PHL}					21	32	
t_{ZH}	Output Control	Y			15	28	ns
t_{ZL}					15	23	
t_{HZ}	Output Control	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 3		27	41	ns
t_{LZ}					18	27	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level

NOTE 3: Load circuit and waveforms are shown on page 3-11.

schematic (each selector/multiplexer, and the common select section)



▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

TYPES SN54LS257B, SN54LS258B, SN54S257, SN54S258, SN74LS257B, SN74LS258B, SN74S257, SN74S258 QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7611734, OCTOBER 1976 – REVISED DECEMBER 1983

- Three-State Outputs Interface Directly with System Bus
- 'LS257B and 'LS258B Offer Three Times the Sink-Current Capability of the Original 'LS257 and 'LS258
- Same Pin Assignments as SN54LS157, SN74LS157, SN54S157, SN74S157, and SN54LS158, SN74LS158, SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems

	AVERAGE PROPAGATION DELAY FROM DATA INPUT	TYPICAL POWER DISSIPATION◇
'LS257B	12 ns	60 mW
'LS258B	12 ns	60 mW
'S257	4.8 ns	320 mW
'S258	4 ns	280 mW

◇Off state (worst case)

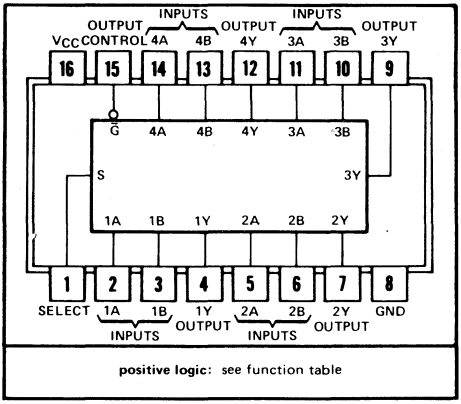
description

These Schottky-clamped high-performance multiplexers feature three-state outputs that can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

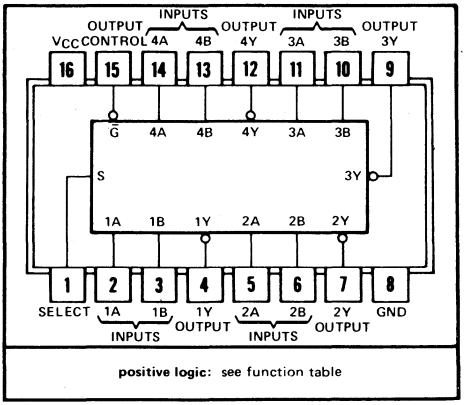
Series 54LS and 54S are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S are characterized for operation from 0°C to 70°C.

SN54LS257B, SN54S257 . . . J OR W PACKAGE
SN74LS257B, SN74S257 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS258B, SN54S258 . . . J OR W PACKAGE
SN74LS258B, SN74S258 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

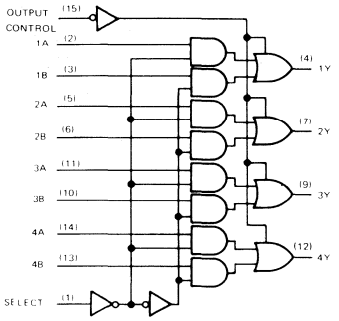
FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	'LS257B 'S257	'LS258B 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

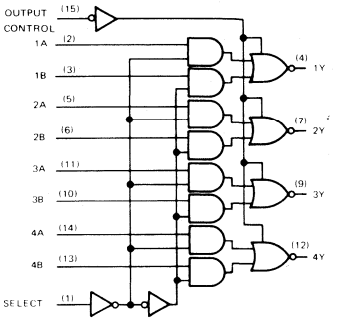
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

functional block diagrams

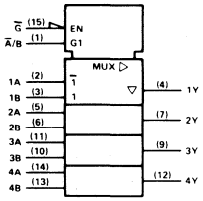
'LS257B, 'S257



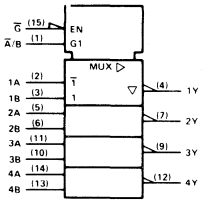
'LS258B, 'S258



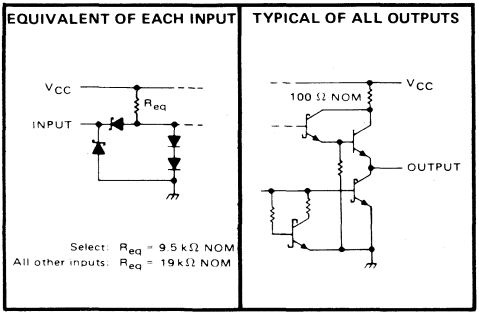
LS257B



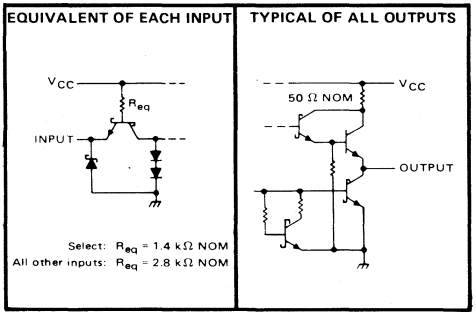
LS258B



'LS257B, 'LS258B



'S257, 'S258



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS257B, 'LS258B Circuits	7 V
'S257, 'S258 Circuits	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS', SN54S' Circuits	−55°C to 125°C
SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−20			−20	μA
I_I	Input current at maximum input voltage	S input	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		Any other					0.1			0.1	
I_{IH}	High-level input current	S input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Any other					20			20	
I_{IL}	Low-level input current	A or B input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Any other					−0.2			−0.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	All outputs high	V_{CC} = MAX, See Note 2	'LS257B		8	12		8	12	mA
		All outputs low				12	18		12	18	
		All outputs off				13	19		13	19	
		All outputs high		'LS258B		6	9		6	9	
		All outputs low				10	15		10	15	
		All outputs off				11	16		11	16	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS257B			'LS258B			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	Any	C_L = 45 pF, See Note 3		8	13		7	12	ns
t_{PHL}					10	15		11	17	
t_{PLH}	Select	Any			16	21		14	21	ns
t_{PHL}					17	24		19	24	
t_{PZH}	Output Control	Any			15	30		15	30	ns
t_{PZL}					17	30		18	30	
t_{PHZ}	Output Control	Any	C_L = 5 pF, See Note 3		19	30		20	30	ns
t_{PLZ}					15	25		16	25	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: Load circuit and waveforms are shown on page 3-11.

recommended operating conditions

	SN54S257, SN54S258			SN74S257, SN74S258			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S257, SN74S257			SN54S258, SN74S258			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1mA	SN74S'	2.7			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	S input	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
		Any other					50			50	
I_{IL}	Low-level input current	S input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
		Any other					−2			−2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	All outputs high	V_{CC} = MAX, See Note 2			44	68		36	56	mA
		All outputs low				60	93		52	81	
		All outputs off				64	99		56	87	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 280 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S257, SN74S257			SN54S258, SN74S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	Any	C_L = 15 pF, See Note 4		5	7.5		4	6	ns
t_{PHL}					4.5	6.5		4	6	
t_{PLH}	Select	Any			8.5	15		8	12	ns
t_{PHL}					8.5	15		7.5	12	
t_{PZH}	Output Control	Any			13	19.5		13	19.5	ns
t_{PZL}					14	21		14	21	
t_{PHZ}	Output Control	Any	C_L = 5 pF, See Note 4		5.5	8.5		5.5	8.5	ns
t_{PLZ}					9	14		9	14	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 4: Load circuit and waveforms are shown on pages 3-10.

TYPES SN54259, SN54LS259B, SN74259, SN74LS259B (TIM9906)
8-BIT ADDRESSABLE LATCHES

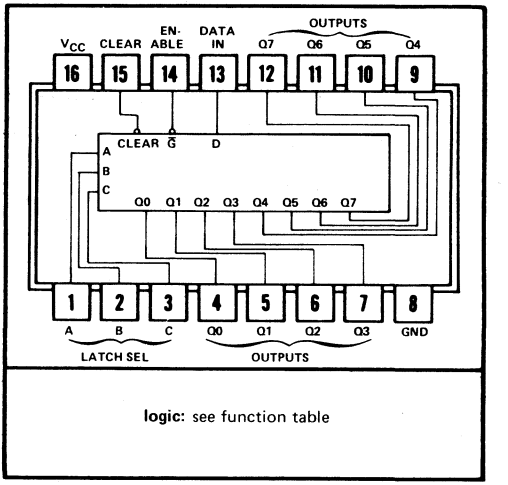
REVISED OCTOBER 1983

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage
- Asynchronous Parallel Clear
- Active High Decoder
- Enable/Disable Input Simplifies Expansion
- Direct Replacement for Fairchild 9334
- Expandable for N-Bit Applications
- Four Distinct Functional Modes
- Typical Propagation Delay Times:

	'259	'LS259B
Enable-to-Output	12	5
Data-to-Output	12	19
Address-to-Output	16	14
Clear-to-Output	16	12

- Fan-Out
  - I_{OL} (Sink Current)
    - '259 . . . . . 16 mA
    - SN54LS259B . . . . . 4 mA
    - SN74LS259B . . . . . 8 mA
  - I_{OH} (Source Current)
    - '259 . . . . . −0.8 mA
    - 'LS259B . . . . . −0.4 mA
- Typical I_{CC}
  - '259 . . . . . 60 mA
  - 'LS259B . . . . . 22 mA

SN54259, SN54LS259B . . . J OR W PACKAGE
SN74259, SN74LS259B . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

FUNCTION TABLE

INPUTS CLEAR	INPUTS $\overline{G}$	OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

LATCH SELECTION TABLE

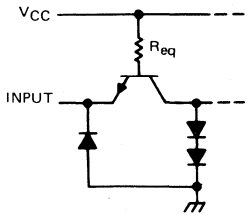
SELECT INPUTS C	B	A	LATCH ADDRESSED
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level
D = the level at the data input
Q_{i0} = the level of Q_i ($i = 0, 1, \ldots 7$, as appropriate) before the indicated steady-state input conditions were established.

schematic of inputs and outputs

'259

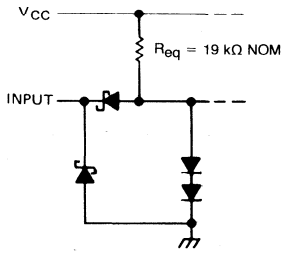
EQUIVALENT OF EACH INPUT



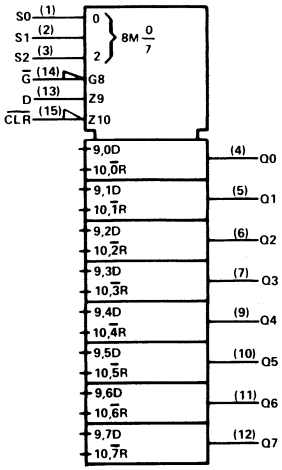
Latch select, data in, or clear: R_{eq} = 4 kΩ NOM
Enable: R_{eq} = 2.2 kΩ NOM

'LS259B

EQUIVALENT OF EACH INPUT EXCEPT $\overline{G}$ INPUT

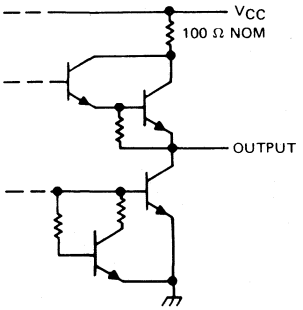


logic symbol



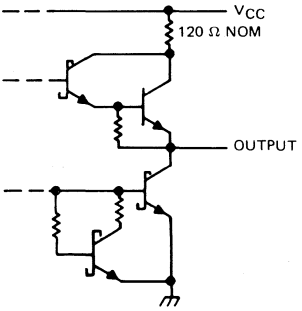
'259

TYPICAL OF ALL OUTPUTS



'LS259B

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: SN54259, SN74259	5.5 V
SN54LS259B, SN74LS259B	7 V
Operating free-air temperature range: SN54259, SN54LS259B	−55 °C to 125 °C
SN74259, SN74LS259B	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54259			SN74259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Width of clear or enable pulse, t_w		15			15			ns
Setup time, t_{su}	Data	15↑			15↑			ns
	Address	5↑			5↑			
Hold time, t_h	Data	0↑			0↑			ns
	Address	20↑			20↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54259			SN74259			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = 12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V			80			80	μA
		Other inputs					40			40	
I_{IL}	Low-level input current	Enable	V_{CC} = MAX,	V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs					−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−18		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		60	90		60	90	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Clear	Any Q	C_L = 15 pF, R_L = 400 Ω, See Note 3		16	25	ns
t_{PLH}	Data	Any Q			14	24	ns
t_{PHL}					11	20	
t_{PLH}	Address	Any Q			15	28	ns
t_{PHL}					17	28	
t_{PLH}	Enable	Any Q			12	20	ns
t_{PHL}					11	20	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit is shown on page 3-10.

recommended operating conditions

		SN54LS259B			SN74LS259B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of clear or enable pulse, t_w		15			15			ns
Setup time, t_{su}	Data before $\overline{G}$ ↑	20			20			ns
	Address before $\overline{G}$ ↑	17			17			
	Address before $\overline{G}$ ↓	0			0			
Hold time, t_h	Data after $\overline{G}$ ↑	0			0			ns
	Address after $\overline{G}$↑	0			0			
Pulse width, t_w	$\overline{G}$ pulse width, low	17			17			ns
	Clear pulse width, low	10			10			
Operating free-air temperature, T_A		−55		125	0		70	°C

†The arrow indicates that the rising edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS259B			SN74LS259B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High level input voltage			2			2			V
V_{IL}	Low level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −0.4 mA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			22	36		22	36	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Clear	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Note 3		12	18	ns
t_{PLH}	Data	Any Q			19	30	ns
t_{PHL}					13	20	
t_{PLH}	Address	Any Q			17	27	ns
t_{PHL}					14	20	
t_{PLH}	Enable	Any Q			5	24	ns
t_{PHL}					9	15	

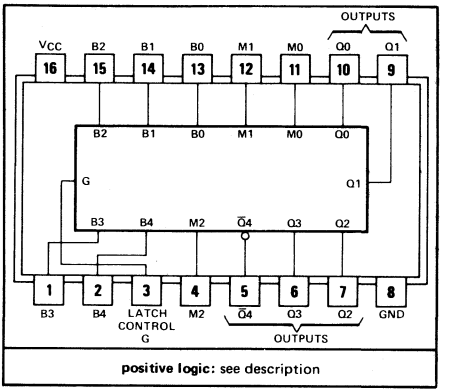
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit is shown on page 3-11.

TYPES SN54LS261, SN74LS261
2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

BULLETIN NO. DL-S 7612123, MARCH 1974—REVISED OCTOBER 1976

- Fast Multiplication . . . 5-Bit Product in 26 ns Typ
- Power Dissipation . . . 110 mW Typical
- Latch Outputs for Synchronous Operation
- Expandable for m-Bit-by-n-Bit Applications
- Fully Compatible with Most TTL and Other Saturated Low-Level Logic Families
- Diode-Clamped Inputs Simplify System Design

SN54LS261 . . . J OR W PACKAGE
SN74LS261 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most-significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

The SN54LS261 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS261 for operation from 0°C to 70°C.

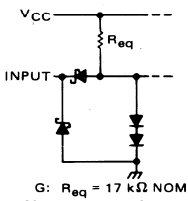
FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL G	MULTIPLIER M2	M1	M0	$\overline{Q4}$	Q3	Q2	Q1	Q0
L	X	X	X	$\overline{Q4}_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B4}$	B4	B3	B2	B1
H	L	H	L	$\overline{B4}$	B4	B3	B2	B1
H	L	H	H	$\overline{B4}$	B3	B2	B1	B0
H	H	L	L	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	H	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	L	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
$\overline{Q4}_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low transition of G.
B4 . . . B0 = The logic level of the indicated multiplicand (B) input.

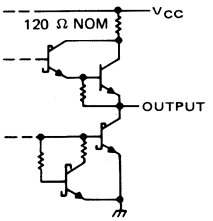
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

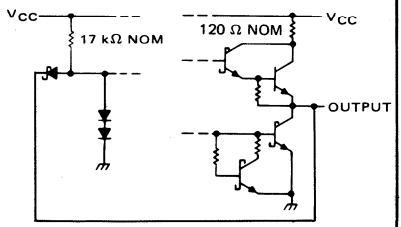


G: R_{eq} = 17 kΩ NOM
B or M_2: R_{eq} = 20 kΩ NOM
MO or MI: R_{eq} = 10 kΩ NOM

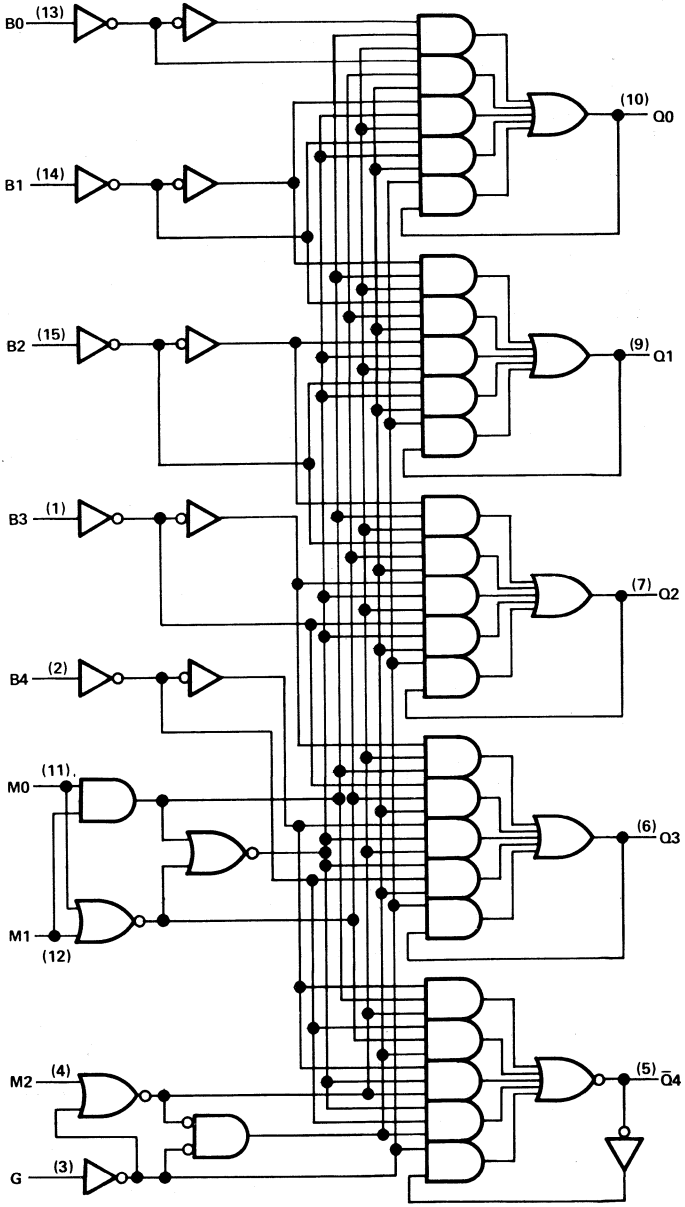
TYPICAL OF Q0, Q1, Q2, Q3 OUTPUTS



TYPICAL OF $\overline{Q4}$ OUTPUT



functional block diagram



TYPES SN54LS261, SN74LS261
2-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

REVISED DECEMBER 1980

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS261 . . . . . −55°C to 125°C
SN74LS261 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS261			SN74LS261			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of enable pulse, t_w		25			25			ns
Setup time, t_{su}	Any M input	17↓			17↓			ns
	Any B input	15↓			15↓			
Hold time, t_h	Any M input	0↓			0↓			ns
	Any B input	0↓			0↓			
Operating free-air temperature, T_A		−55		125	0		70	°C

↓The arrow indicates that the falling edge of the enable pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS261			SN74LS261			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	MO or MI			0.2			0.2	mA
				All others			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	MO or MI			40			40	μA
				All others			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	MO or MI			−0.8			−0.8	mA
				All others			−0.4			−0.4	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open.	All inputs at 0 V,			20	38		20	40	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the output short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

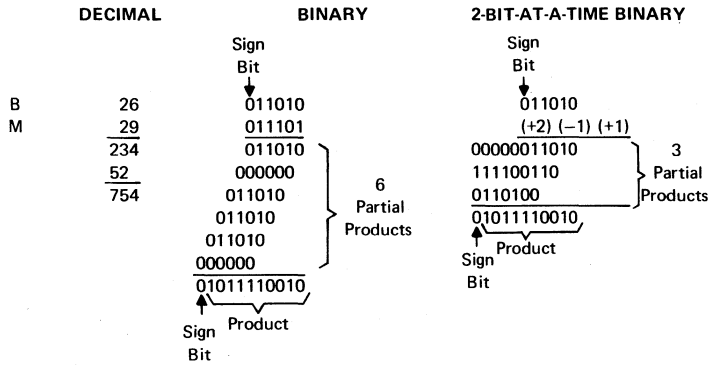
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable G	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	35	ns
t_{PHL}					20	30	ns
t_{PLH}	Any M input	Any Q			25	40	ns
t_{PHL}					22	35	ns
t_{PLH}	Any B input	Any Q			27	42	ns
t_{PHL}					24	37	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA

Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:

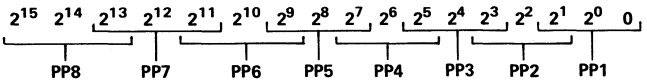


Two points should be noted in the two-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer.

A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.



TYPICAL APPLICATION DATA

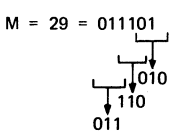
2. Generate partial product (PPi) as shown in the following table:

MULTIPLIER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplicand by zero
0	0	1	+1 B	Copy multiplicand
0	1	0	+1 B	Copy multiplicand
0	1	1	+2 B	Shift multiplicand left one bit
1	0	0	−2 B	Shift two's complement of multiplicand left one bit
1	0	1	−1 B	Replace multiplicand by two's complement
1	1	0	−1 B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

3. Weight the partial products by indexing each two places left relative to the next-less-significant product.

4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

EXAMPLE OF ALGORITHM



Operator Symbol	B = 26 = 011010
+1 B	00000011010
−1B	111100110
+2 B	0110100

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 'LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.

2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

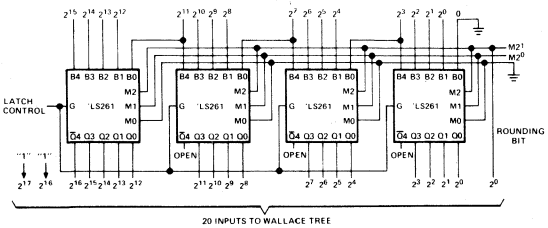


FIGURE A–FIRST PARTIAL PRODUCT, PP1

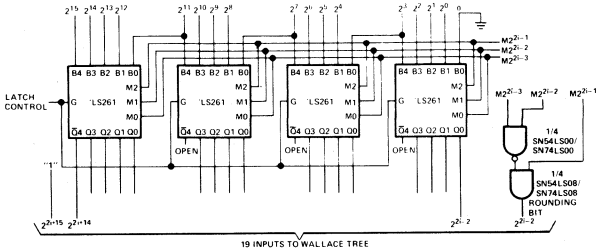


FIGURE B–OTHER PARTIAL PRODUCTS, PPi

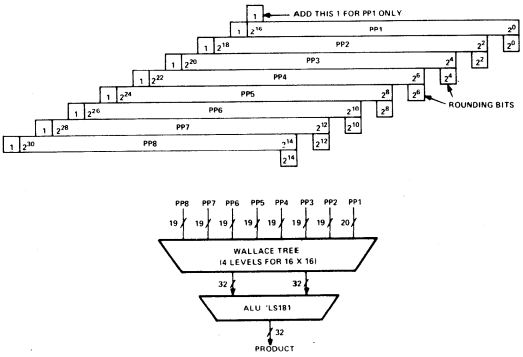


FIGURE C–MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 'LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 'LS261s m x n ÷ 16 'LS00s, and m x n ÷ 16 'LS08s. The size of the Wallace tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

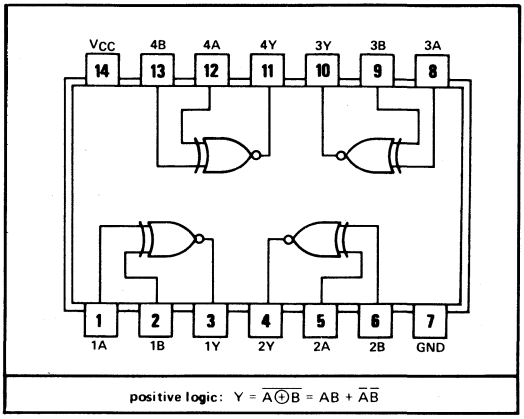
32	SN54LS261/SN74LS261
2	SN54LS00/SN74LS00
2	SN54LS08/SN74LS08
56	SN54H183/SN74H183
7	SN54LS181/SN74LS181
2	SN54LS182/SN74LS182

TYPES SN54LS266, SN74LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES
WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7611843, DECEMBER 1972—REVISED OCTOBER 1976

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

SN54LS266 . . . J OR W PACKAGE
SN74LS266 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

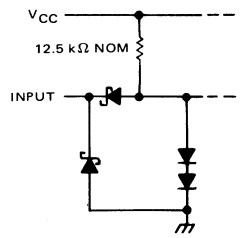
H = high level, L = low level

description

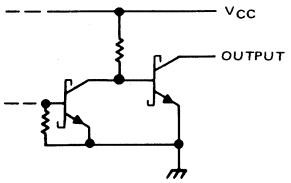
The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS266 . . . . . −55°C to 125°C
SN74LS266 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS266			SN74LS266			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS266			SN74LS266			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		8	13		8	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 3		18	30	ns
t_{PHL}					18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

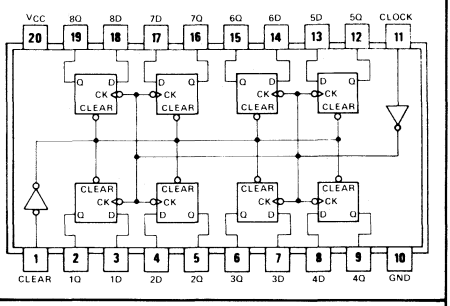
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54273, SN54LS273, SN74273, SN74LS273
OCTAL D-TYPE FLIP-FLOP WITH CLEAR

BULLETIN NO. DL-S 7612091, OCTOBER 1976

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54273, SN54LS273 . . . J PACKAGE
SN74273, SN74LS273 . . . J OR N PACKAGE



positive logic: see function table

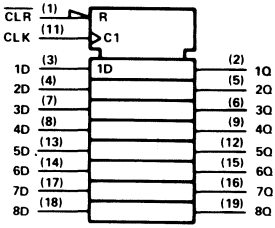
description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

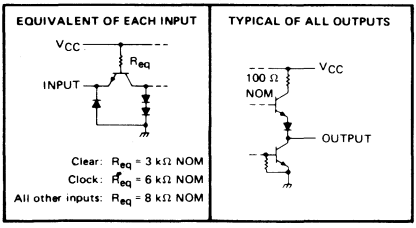
These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

logic symbol

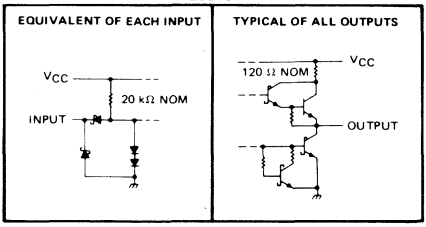


schematics of inputs and output

'273

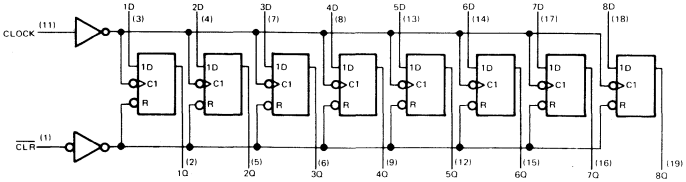


'LS273



functional block diagram

logic diagram (positive logic)



FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

See explanation of function tables on page 3-8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54273 . . . . . −55°C to 125°C
SN74273 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54273			SN74273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		16.5			16.5			ns
Set-up time, t_{su}	Data input	20†			20†			ns
	Clear inactive state	25†			25†			
Data hold time, t_h		5†			5†			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2			V
V_{IL} Low-level input voltage					0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH} High-level input current	Clear	V_{CC} = MAX, V_I = 2.4 V			80	μA
	Clock or D				40	
I_{IL} Low-level input current	Clear	V_{CC} = MAX, V_I = 0.4 V			−3.2	mA
	Clock or D				−1.6	
I_{OS} Short-circuit output current§		V_{CC} = MAX	−18		−57	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2		62	94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS273 . . . . . −55°C to 125°C
SN74LS273 . . . . . 0°C to 70°C
Storage temperature range . . . . . 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

		SN54LS273			SN74LS273			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Set-up time, t_{su}	Data input	20↑			20↑			ns
	Clear inactive state	25↑			25↑			
Data hold time, t_h		5↑			5↑			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS273			SN74LS273			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = −0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			17	27		17	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 4	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

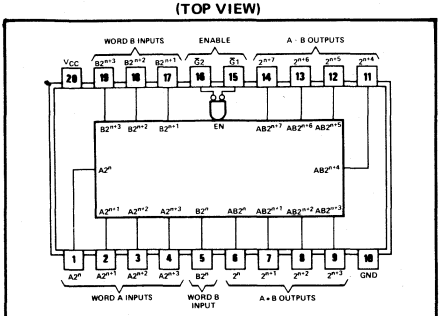
TYPES SN54LS275, SN54S274, SN54S275, SN74LS275, SN74S274, SN74S275
4-BIT-BY-4-BIT BINARY MULTIPLIER WITH 3-STATE OUTPUTS
7-BIT-SLICE WALLACE TREES WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612121, OCTOBER 1976

- 'S274 Provides 8-Bit Product in Typically 45 ns
- 'S274 Can Provide Sub-Multiple Products for n-Bit-by-n-Bit Binary Numbers
- 'LS275 and 'S275 Accept 7 Bit-Slice Inputs and 2 Carry Inputs for Reduction to 4 Lines in Typically 45 ns
- These High-Complexity Functions Can Reduce Package Count by Nearly 50% in Most Parallel Multiplier Designs
- When SN74S274 is Combined With SN74H183 (or SN74LS183) and Schottky Look-Ahead Adders, Multiplication Times are Typically:

  16-Bit Product in 75 ns (79 ns)
  32-Bit Product in 116 ns (132 ns)

SN54S274 . . . J PACKAGE
SN74S274 . . . J OR N PACKAGE
(TOP VIEW)



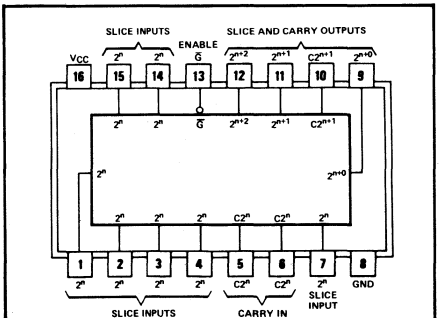
positive logic: When either (or both) $\overline{G}$ input(s) is (are) high, all eight outputs are off.

description

These high-complexity Schottky-clamped TTL circuits are designed specifically to reduce the delay time required to perform high-speed parallel binary multiplication and significantly reduce package count. The 'S274 is a basic 4-bit-by-4-bit parallel multiplier in a single package, and as such, no additional components are required to obtain an 8-bit product. For word lengths longer than 4 bits, a number of 'S274 multipliers can be combined to generate sub-multiple partial products. These partial products can then be combined in Wallace trees to obtain the final product. See Typical Application Data.

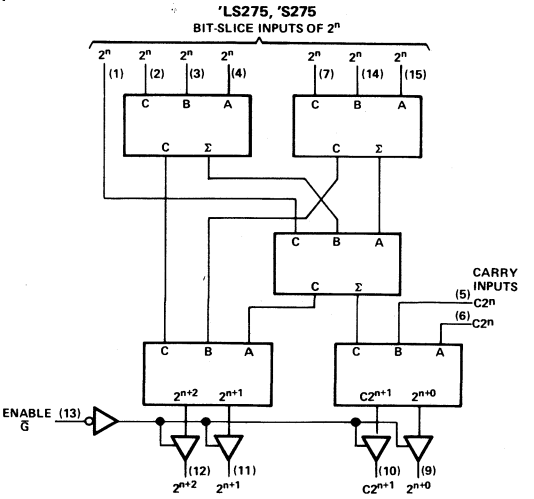
The 'LS275 and 'S275 expandable bit-slice Wallace trees have been designed to accept up to seven bit-slice inputs and two carry inputs from previous slices for reduction to four lines.

SN54LS275, SN54S275 . . . J PACKAGE
SN74LS275, SN74S275 . . . J OR N PACKAGE
(TOP VIEW)



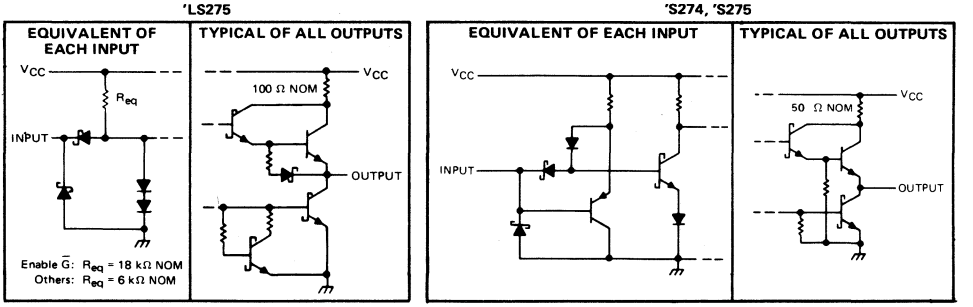
positive logic: When $\overline{G}$ is high, all four outputs are off.

functional block diagram



NOTE: When one of of the $C_2{}^n$ carry inputs is not used, it must be grounded. If neither $C_2{}^n$ carry input is used, both $C_2{}^n$ inputs are grounded and the $C_2{}^{n+1}$ output is normally left open.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS275	7 V
'S274, 'S275	5.5 V
Off-state output voltage: 'LS275	7 V
'S274, 'S275	5.5 V
Operating free-air temperature range: SN54LS, SN54S Circuits	−55°C to 125°C
SN74LS, SN74S Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS275			SN74LS275			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS275			SN74LS275			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.2		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL}max	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−20			−20	μA
I_I	Input current at maximum input voltage	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		All others					0.3			0.3	
I_{IH}	High-level input current	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		All others					60			60	
I_{IL}	Low-level input current	Enable $\overline{G}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−1.2			−1.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX			25	40		25	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable $\overline{G}$	Any	C_L = 45 pF, R_L = 667 Ω, See Note 2		35	62	ns
t_{PHL}					42	66	
t_{PZH}			C_L = 45 pF, R_L = 667 Ω, See Note 2		8	23	ns
t_{PZL}					13	23	
t_{PHZ}			C_L = 5 pF, R_L = 667 Ω, See Note 2		10	15	ns
t_{PLZ}					10	15	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54S274 SN54S275			SN74S274 SN74S275			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S274 SN54S275			SN74S274 SN74S275			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX			105	155		105	155	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S274 SN54S275			SN74S274 SN74S275			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PHL}	Any A or B ('S274), or Any Slice or Carry ('S275)	Any	C_L = 30 pF, R_L = 400 Ω, See Note 3		50	95		50	70	ns
t_{PLH}					50	95		50	70	
t_{PZH}	Any Enable	Any	C_L = 5 pF, R_L = 400 Ω, See Note 3		15	45		15	30	ns
t_{PZL}					15	45		15	30	
t_{PHZ}					10	40		10	25	ns
t_{PLZ}					10	40		10	25	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPICAL APPLICATION DATA

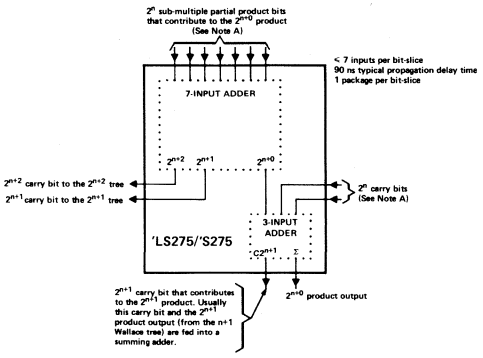


FIGURE 1—BASIC BIT-SLICE WALLACE TREE

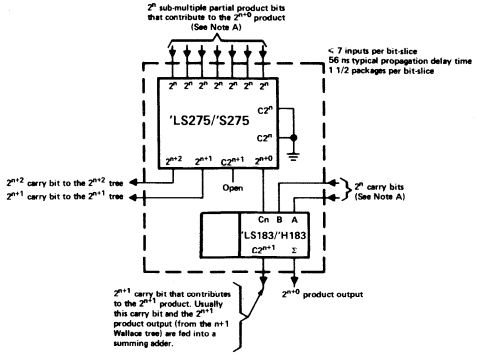


FIGURE 2—HIGH-SPEED BIT-SLICE WALLACE TREE

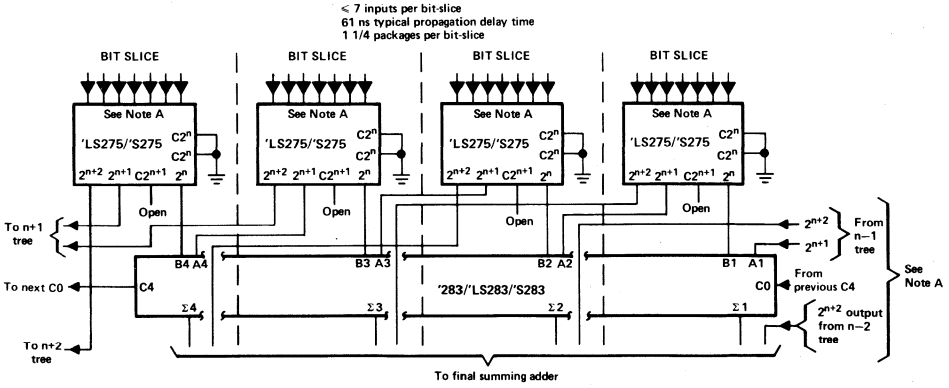
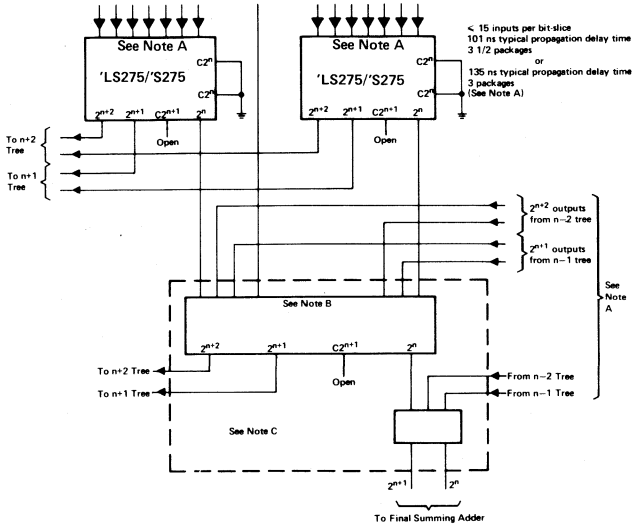


FIGURE 3—MODERATE-SPEED BIT-SLICE WALLACE TREE

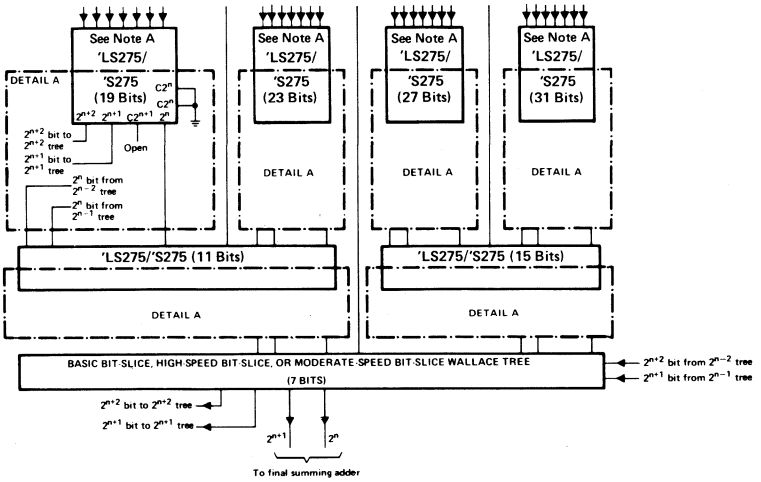
NOTE A: All unused inputs must be grounded.

TYPICAL APPLICATION DATA



NOTES: A. Ground unused inputs.
B. These outputs from preceeding trees may go to any of the inputs of the 'LS275/'S275.
C. The circuit within the dotted lines may be either the basic bit-slice Wallace tree or the high-speed Wallace tree. In the latter case both carry inputs of the 'LS275/'S275 must be grounded.

FIGURE 4—15-BIT-SLICE WALLACE TREE FOR 32-BIT X 32-BIT MULTIPLIER



NOTES: A. Ground unused inputs.
B. The number of bits in parentheses is the maximum number of bits this tree can combine if the remaining 'LS275/'S275 (all having a higher number in the parentheses) were not connected.

FIGURE 5—7-TO-31-BIT-SLICE WALLACE TREE FOR UP TO 64-BIT X 64-BIT MULTIPLIERS

TYPICAL APPLICATION DATA

$$2^{\text{upper half of n}} \times 2^{\text{lower half of n}}$$

$$2^{\text{upper half of n}} \times 2^{\text{upper half of n}} \quad 2^{\text{lower half of n}} \times 2^{\text{lower half of n}}$$

$$2^{\text{lower half of n}} \times 2^{\text{upper half of n}}$$

NOTE A: The left-hand half of each rectangle is the portion of word one used to obtain the product shown within the rectangle. Similarly, the right-hand half of each rectangle is the portion of word two used.

FIGURE 6–UNIVERSAL METHOD OF ADDING $\frac{n}{2}$-BIT PRODUCTS TO OBTAIN AN n-BIT PRODUCT

$$(2^{16} \text{ to } 2^{31}) \times (2^{0} \text{ to } 2^{15})$$

$$(2^{16} \text{ to } 2^{31}) \times (2^{16} \text{ to } 2^{31}) \quad (2^{0} \text{ to } 2^{15}) \times (2^{0} \text{ to } 2^{15})$$

$$(2^{0} \text{ to } 2^{15}) \times (2^{16} \text{ to } 2^{31})$$

FIGURE 7–METHOD OF ADDING 32-BIT PRODUCTS TO OBTAIN A 64-BIT PRODUCT

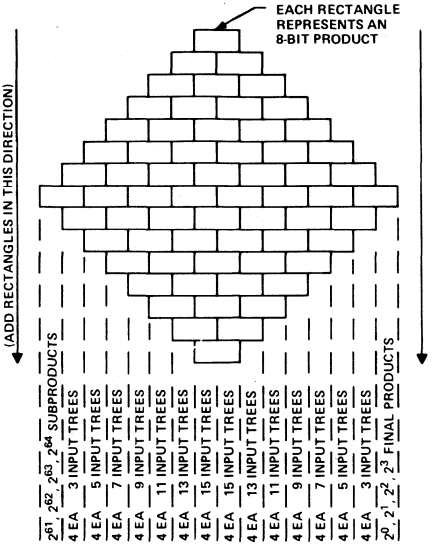
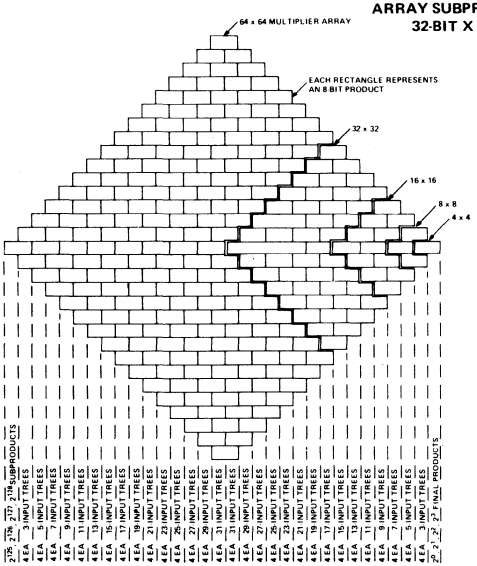


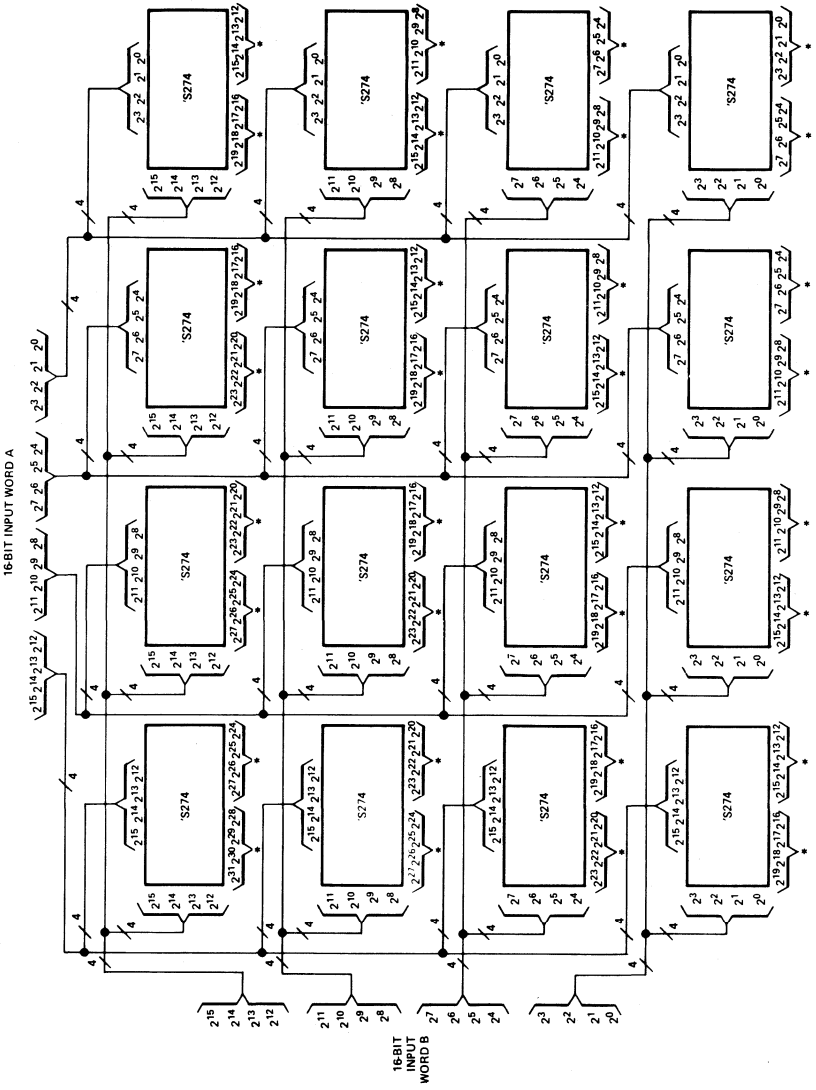
FIGURE 8–FINAL PRODUCTS AND ARRAY SUBPRODUCT ADDITIONS FOR 32-BIT X 32-BIT MULTIPLIER



NOTE A: See Note B of Figure 6 for designing trees with any number of inputs up to 31.

FIGURE 9–ARRAY ARRANGEMENT FOR VARIOUS MULTIPLIERS INCLUDING ARRAY SUBPRODUCT ADDITIONS FOR 64-BIT X 64-BIT MULTIPLIER

TYPICAL APPLICATION DATA



*This 4-bit binary number is a partial product. See Figure 11, Sheets 2 and 3 for diagram of summation process.

FIGURE 10–16-BIT X 16-BIT MULTIPLIER (SHEET 1 OF 3–OUTPUT CONNECTIONS)

TYPICAL APPLICATION DATA

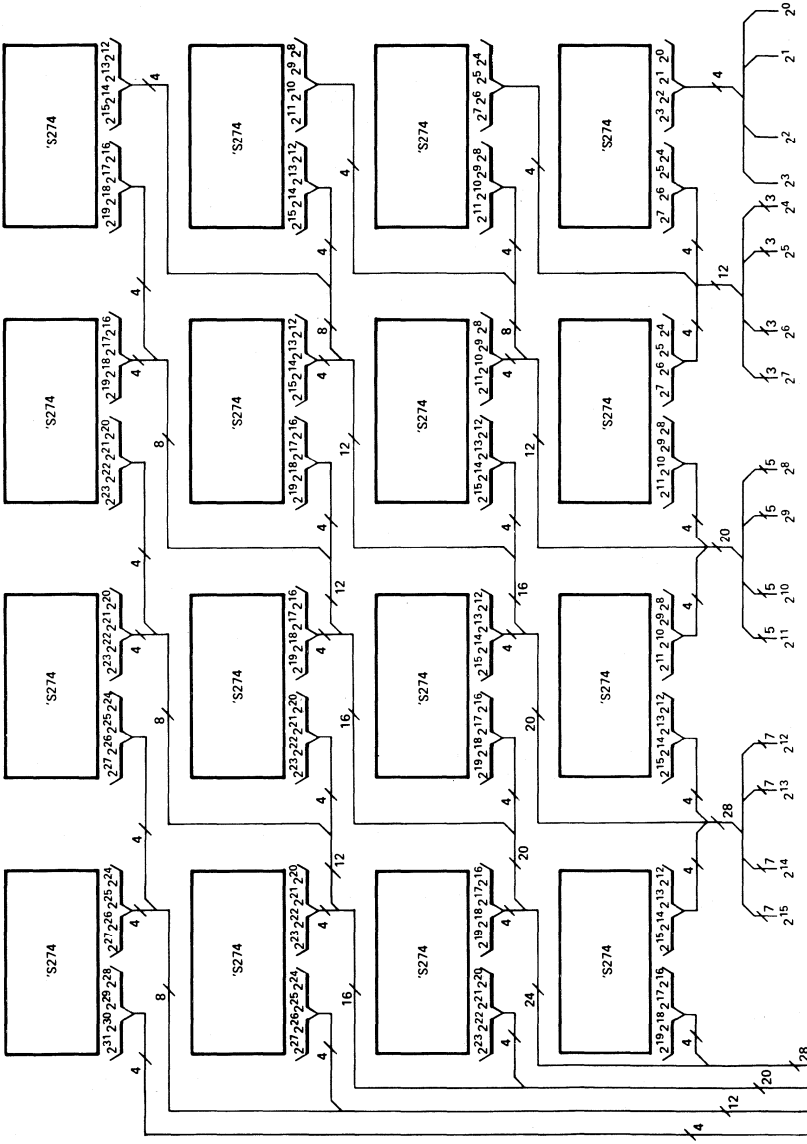
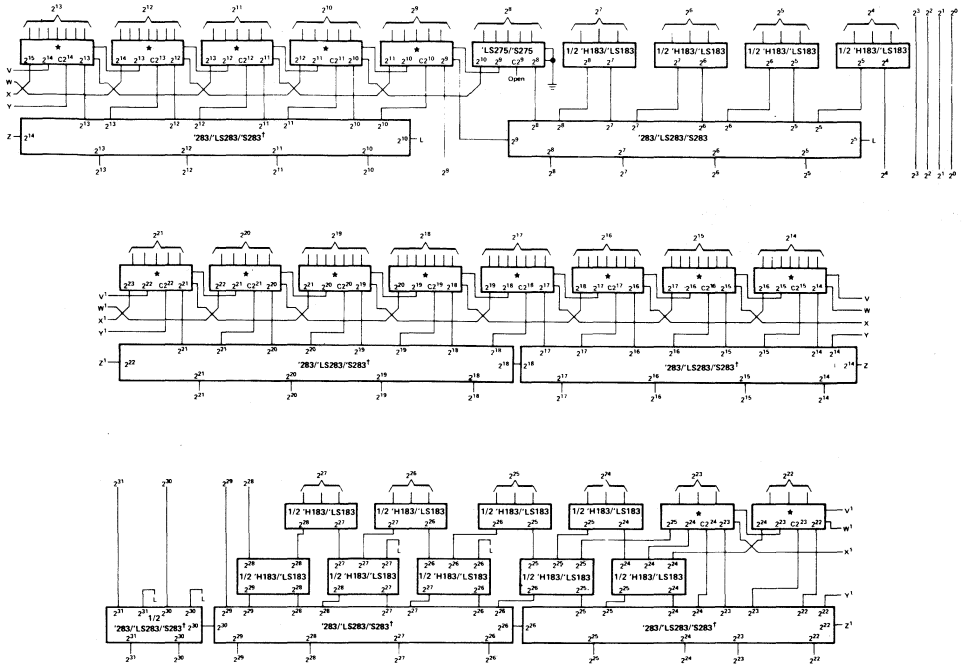


FIGURE 10–16-BIT X 16-BIT MULTIPLIER (SHEET 2 OF 3–OUTPUT CONNECTIONS)

TYPICAL APPLICATION DATA



*Each starred block may be either a basic bit-slice Wallace tree('LS275 or 'S275 only) or a high-speed bit-slice Wallace tree ('LS275 plus 1/2 'LS183 or 'S275 plus 1/2 'H183). In either case the function of the terminal is the same as the similarly located terminal of the basic bit-slice (Figure 1) or high-speed bit-slice Wallace tree (Figure 2). Also for either tree, when only five inputs of the seven-input adder of the 'LS275/'S275 are used, the remaining two inputs must be grounded. When the high-speed adder is used, the $C2^n$ inputs of the 'LS275/'S275 must be grounded.

†For improved performance SN74LS181/SN74S181 ALUs with SN74S182 look-ahead generators can be substituted for the SN74283/SN74LS283/SN74S283 adders. Typically, the multiplication time will be reduced by 18 to 32 nanoseconds.

FIGURE 10–16-BIT X 16-BIT MULTIPLIER
(SHEET 3 OF 3–SUMMING PARTIAL PRODUCTS)

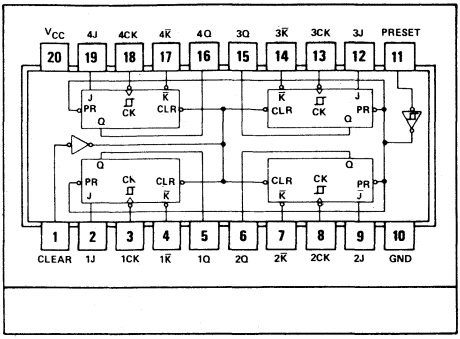
TYPES SN54276, SN74276
QUADRUPLE J-K FLIP-FLOPS

BULLETIN NO. DL-S 7612460, OCTOBER 1976

features

- Four J-$\overline{K}$ Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Separate Negative-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Typical Clock Input Frequency . . . 50 MHz
- Fully Buffered Outputs

SN54276 . . . J PACKAGE
SN74276 . . . J OR N PACKAGE
(TOP VIEW)

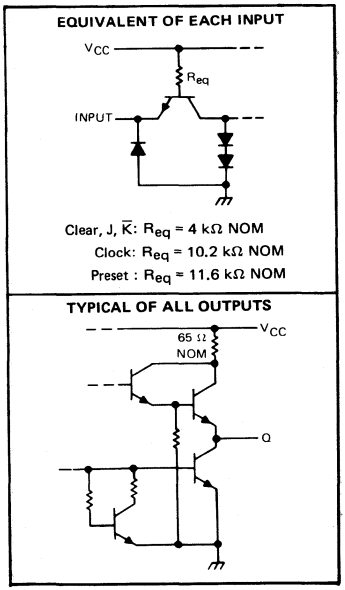


description

These quadruple TTL J-$\overline{K}$ flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by up to 50%. They feature hysteresis at each clock input, fully buffered outputs, and direct clear capability, and are presettable through a buffer that also features an input hysteresis loop. The negative-edge-triggering clocks are directly compatible with earlier Series 54/74 single and dual pulse-triggered flip-flops. These circuits can be used to emulate D- or T-type flip-flops by hard-wiring the inputs, or to implement asychronous sequential functions.

The SN54276 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74726 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INPUTS			OUTPUT
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H†
H	H	↓	L	H	Q_0
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q_0

†This configuration is nonstable; that is, it may not persist when preset and clear return to their inactive (high) level.

See explanation of function tables on page 3-8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54276 . . . . . −55°C to 125°C
SN74276 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54276			SN74276			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency		0		35	0		35	MHz
Pulse width, t_w	Clock high	13.5			13.5			ns
	Clock low	15			15			
	Preset or clear low	12			12			
Setup time, t_{su}	$\overline{J}$, $\overline{K}$ inputs	3↓			3↓			ns
	Clear and preset inactive state	10↓			10↓			
Input hold time, t_h		10↓			10↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−85	mA
I_{CC}	Supply current	V_{CC} = MAX			60	81	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 2	35	50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset			15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	ns

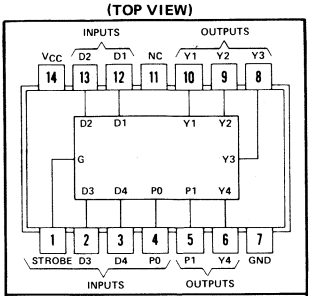
NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54278, SN74278
4-BIT CASCADABLE PRIORITY REGISTERS

BULLETIN NO. DL-S 7211729, MAY 1972—REVISED DECEMBER 1972

- Latched Data Inputs Serve as Buffer Register and Can also:
  - Synchronize Data Acquisition
  - "Debounce" Mechanical Switch Input
- Cascading Input P0 and Output P1 Provides "Busy"Signal Inhibiting All Lower-Order Bits
- Full TTL Compatibility
- Use for:
  - Priority Interrupt
  - Synchronous Priority Line Selection

SN54278 . . . J OR W PACKAGE
SN74278 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

description

The SN54278 and SN74278 each consist of four data latches, full priority output gating, and a cascading gate. The highest-order data applied at a D latch input is transferred to the appropriate Y output while the strobe input is high, and when the strobe goes low all data is latched. The cascading input P0 is fully overriding and on the highest-order package this input must be held at a low logic level. The P1 output is intended for connection to the P0 input of the next lower-order package and will provide a "busy" (high-level) signal to inhibit all subsequent lower-order packages.

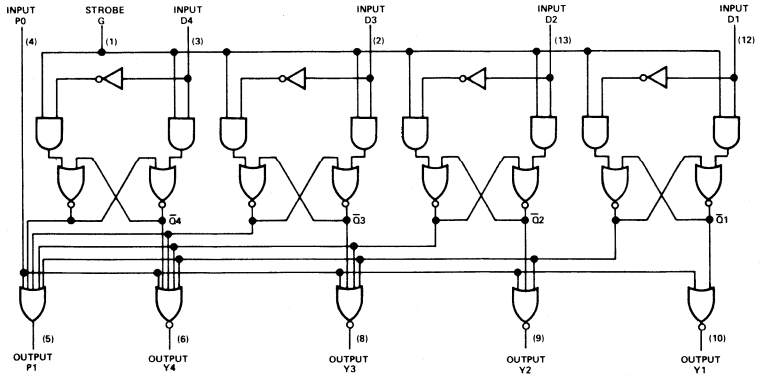
After the overriding P0 input, the order of priority is D1, D2, D3, and D4, respectively, within the package.

FUNCTION TABLE

INPUTS						INTERNAL LATCH NODES				OUTPUTS				
P0	G	D1	D2	D3	D4	$\bar{Q}1$	$\bar{Q}2$	$\bar{Q}3$	$\bar{Q}4$	Y1	Y2	Y3	Y4	P1
L	H	H	X	X	X	L	X	X	X	H	L	L	L	H
L	H	L	H	X	X	H	L	X	X	L	H	L	L	H
L	H	L	L	H	X	H	H	L	X	L	L	H	L	H
L	H	L	L	L	H	H	H	H	L	L	L	L	H	H
L	H	L	L	L	L	H	H	H	H	L	L	L	L	L
L	L	X	X	X	X	Latched when G goes low				Same function of $\bar{Q}$ nodes as on 1st 5 lines				
H	L	X	X	X	X					L	L	L	L	H
H	H	Internal $\bar{Q}$ levels are same function of D inputs as on first 5 lines								L	L	L	L	H

H = high level, L = low level, X = irrelevant

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54278 Circuits . . . . . −55°C to 125°C
SN74278 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the strobe input and any of the four data inputs.

recommended operating conditions

	SN54278			SN74278			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Data setup time, t_{su} (see Figure 1)	20			20			ns
Data hold time, t_h (see Figure 1)	5			5			ns
Strobe pulse width, t_w (see Figure 1)	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		P0 input					200	
		G input					320	
I_{IL}	Low-level input current	Any D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		P0 input					−8	
		G input					−12.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54278	−18		−55	mA
				SN74278	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			55	80	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the P0 input grounded, all other inputs at 4.5 V, and outputs open.

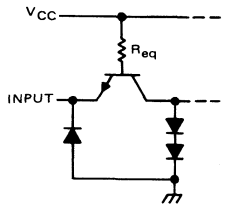
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORMS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	A and C (with strobe high)	C_L = 15 pF, R_L = 400 Ω, See Figure 1			30	ns
t_{PHL}							39	
t_{PLH}	Data	Y	A and D (with strobe high)				38	ns
t_{PHL}							31	
t_{PLH}	Data	P1	A and E (with strobe high)				46	ns
t_{PHL}							39	
t_{PLH}	Strobe	Any Y	B and C or B and D				30	ns
t_{PHL}							31	
t_{PLH}	Strobe	P1	B and E				38	ns
t_{PHL}							42	
t_{PLH}	P0	P1	F and G				23	ns
t_{PHL}							30	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

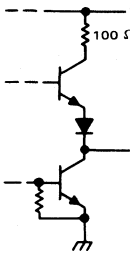
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

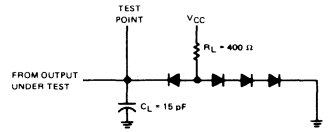


Any D: R_{eq} = 2.5 kΩ NOM
P0: R_{eq} = 1 kΩ NOM
G: R_{eq} = 0.6 kΩ NOM

TYPICAL OF ALL OUTPUTS

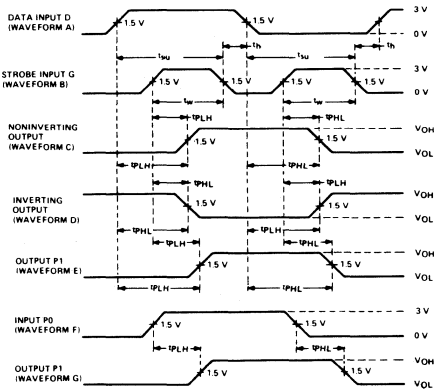


PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTE: Input pulses are supplied by a generator having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.

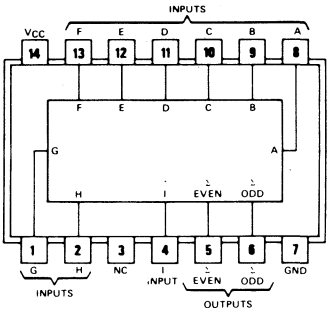
FIGURE 1–SWITCHING TIMES

TYPES SN54LS280, SN54S280, SN74LS280, SN74S280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7611829, DECEMBER 1972—REVISED OCTOBER 1976

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns for 'S280 and 33 ns for 'LS280
- Typical Power Dissipation:
  'LS280 . . . 80 mW
  'S280 . . . 335 mW

SN54LS280, SN54S280 . . . J OR W PACKAGE
SN74LS280, SN74S280 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

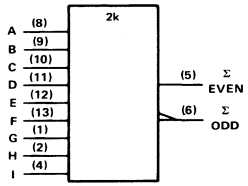
NC—No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

logic symbol



description

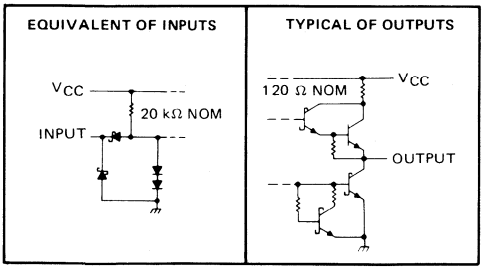
These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity application. The word-length capability is easily expanded by cascading as shown under typical application data.

Series 54LS/74LS and Series 54S/74S parity generators/checkers offer the designer a trade-off between reduced power consumption and high performance. These devices can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'LS280 and 'S280 are implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'LS280 and 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'LS280's and 'S280's are mixed with existing '180's.

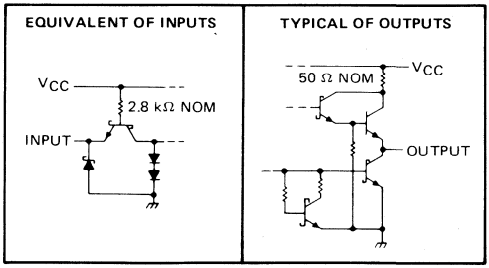
These devices are fully compatible with most other TTL and DTL circuits. All 'LS280 and 'S280 inputs are buffered to lower the drive requirements to one Series 54LS/74LS or Series 54S/74S standard load, respectively.

schematics of inputs and outputs

'LS280



'S280



REVISED DECEMBER 1980

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS280 . . . . . −55°C to 125°C
SN74LS280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS280			SN74LS280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−0.4			.4	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS280			SN74LS280			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		0.25	0.4		0.25	0.4	V
							0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		16	27		16	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 2 kΩ, Inputs not under test at 0 V, See Note 3		33	50	ns
t_{PHL}					29	45	
t_{PLH}	Data	Σ Odd			23	35	ns
t_{PHL}					31	50	

¶t_{PLH} = propagation delay time, low-to-high-level output; t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range; SN54S280 . . . . . −55°C to 125°C
SN74S280 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S280			SN74S280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54S280		67	99	mA
			SN74S280		67	105	
		V_{CC} = MAX, T_A = 125°C, See Note 2	SN54S280N			94	mA

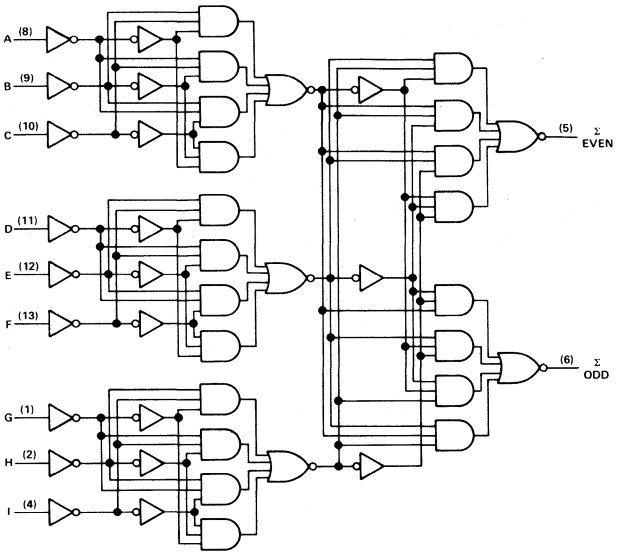
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 280 Ω, See Note 4		14	21	ns
t_{PHL}					11.5	18	
t_{PLH}	Data	Σ Odd			14	21	ns
t_{PHL}					11.5	18	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

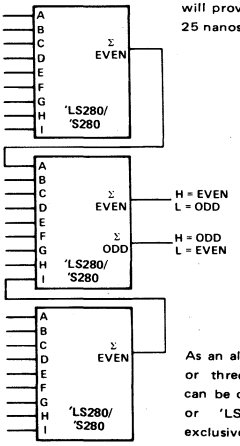
functional block diagram



TYPICAL APPLICATION DATA

25-LINE PARITY/GENERATOR CHECKER

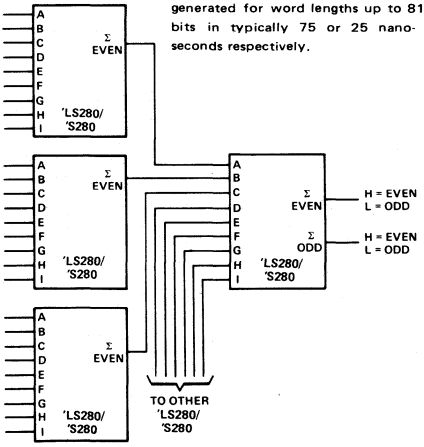
Three 'LS280's or 'S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 75 or 25 nanoseconds respectively.



As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86 or 'LS86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER

Longer word lengths can be implemented by cascading 'LS280's or 'S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 75 or 25 nanoseconds respectively.

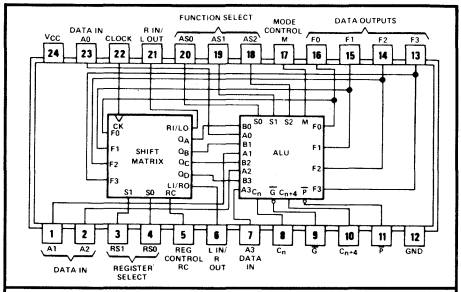


TYPES SN54S281, SN74S281
4-BIT PARALLEL BINARY ACCUMULATORS

BULLETIN NO. DL-S 7612065, FEBRUARY 1974 – REVISED OCTOBER 1976

- Full 4-Bit Binary Accumulator in a Single Package
- 15 Arithmetic/Logic-Type Operations:
  - Add
  - Subtract (B–A or A–B)
  - Complement
  - Increment
  - Transfer
  - Plus 10 Other Functions
- Full Shifting Capabilities:
  - Logic Shift (Left or Right)
  - Arithmetic Shift (Left or Right) for Sign Bit Protection
  - Hold
  - Parallel Load
- Expandable to Handle n-Bit Words with Full Carry Look-Ahead
- Logic Mode Operation Provides Seven Boolean Functions of the Two Variables

SN54S281 . . . J OR W PACKAGE
SN74S281 . . . J, N OR NT PACKAGE
(TOP VIEW)



logic: see description and function tables

description

These Schottky-clamped four-bit accumulators integrate high-performance versions of an arithmetic logic unit/function generator and a shift/storage matrix on a single monolithic circuit bar. The arithmetic logic unit (ALU) portion, similar to the SN54S181/SN74S181 circuit, incorporates the capability to perform 16 arithmetic/logic-type operations as detailed in Table 1. The accumulator includes an exchange of subtract operands by which either A–B or B–A can be accomplished directly. The ALU is controlled by three function-select inputs (AS0, AS1, AS2) and a mode-control input (M). When the mode-control input is high, the ALU is placed in a logic mode that performs any of seven logic functions on two binary variables as detailed in Table 2. Full carry look-ahead is provided for fast, simultaneous carry generation for the full four binary bits. The carry input (C_n) and propagate and generate outputs ($\overline{P}$, $\overline{G}$) are implemented for direct use with the SN54S182/SN74S182 look-ahead carry generators. This permits systems to be implemented with the added advantage of full look-ahead across any word length to minimize the accumulator delay times. Once data is loaded into the accumulator, the typical add time with full look-ahead is 29 nanoseconds for 16-bit words.

The shift/storage matrix is analogous in its capabilities to the SN54S194/SN74S194 universal bidirectional shift register with the added advantages of multiplexed input/output (I/O) cascading lines that comprehend arithmetic shift functions having a sign bit, such as 2's complements. The matrix can be used to perform either logic or arithmetic shifts in either direction (left or right), parallel load, or hold. Control of the register is accomplished with three inputs: register control (RC) and register selection (RS0, RS1). The cascading input/output lines incorporate three-state outputs multiplexed with an input. The least-significant cascading bit is combined with the A0, F0 circuitry to provide the shift-right input and the shift-left output (RI/LO), and the most significant bit is coupled with the A3, F3 circuitry to provide the shift-left input and the shift-right output (LI/RO).

Series 54S circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74S circuits are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

TABLE 1–ARITHMETIC FUNCTIONS
Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
			C_n = H	C_n = L
AS2	AS1	AS0	(with carry)	(no carry)
L	L	L	F_0 = L, $F_1 = F_2 = F_3$ = H	F_n = H
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	$F_n = B_n$
H	L	H	F = $\overline{B}$ PLUS 1	$F_n = \overline{B}_n$
H	H	L	F = A PLUS 1	$F_n = A_n$
H	H	H	F = $\overline{A}$ PLUS 1	$F_n = \overline{A}_n$

TABLE 2–LOGIC FUNCTIONS
Mode Control (M) = High
Carry Input (C_n) = X (Irrelevant)

ALU SELECTION			ACTIVE-HIGH DATA FUNCTION
AS2	AS1	AS0	
L	L	L	$F_n = L$
L	X	H	$F_n = \overline{A_n \oplus B_n}$
L	H	L	$F_n = A_n \oplus B_n$
H	L	L	$F_n = \overline{A_n B_n}$
H	L	H	$F_n = A_n + B_n$
H	H	L	$F_n = \overline{A_n B_n}$
H	H	H	$F_n = A_n + B_n$

TABLE 3 – SHIFT-MODE FUNCTIONS
C_n = M = AS0 = AS1 = L, and AS2 = H ($F_n = B_n$)

FUNCTION	INPUTS BEFORE ↑									CLOCK INPUT	OUTPUTS AFTER ↑					
	REGISTER SELECTION		REGISTER CONTROL INPUT	INPUT/ OUTPUT RI/LO	SHIFT-MATRIX INPUTS				INPUT/ OUTPUT LI/RO		INPUT/ OUTPUT RI/LO	SHIFT-MATRIX OUTPUTS (ALU B INPUTS)				INPUT/ OUTPUT LI/RO
	RS0	RS1			F0	F1	F2	F3				Q_A	Q_B	Q_C	Q_D	
LOAD	L	L	X	Z	f0	f1	f2	f3	Z	↑	Z	f0	f1	f2	f3	Z
LSL	L	H	L	Q_A	Q_A	Q_B	Q_C	Q_D	li	↑	Q_{Bn}	Q_{Bn}	Q_{Cn}	Q_{Dn}	li	li
LSA	L	H	H	Q_A	Q_A	Q_B	Q_C	Q_D	li	↑	Q_{Bn}	Q_{Bn}	Q_{Cn}	li	Q_{D0}	li
RSL	H	L	L	ri	Q_A	Q_B	Q_C	Q_D	Q_D	↑	ri	ri	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
RSA	H	L	H	ri	Q_A	Q_B	Q_C	Q_D	Q_C	↑	ri	ri	Q_{An}	Q_{Bn}	Q_{D0}	Q_{Bn}
HOLD	H	H	X	X	Q_A	Q_B	Q_C	Q_D	X	↑	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Z
	X	X	X	X	Q_A	Q_B	Q_C	Q_D	X	L	RI/LO	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	LI/RO

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high impedance (output off)
↑ = transition from low to high level
f0, f1, f2, f3, ri, li = the level of steady-state conditions at F0, F1, F2, F3, RI/LO, or I/RO respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent transition of the clock
See explanation of function tables on page 3-8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S281 (see Note 2) . . . . . −55°C to 125°C
SN74S281 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 20°C/W.

recommended operating conditions

		SN54S281			SN74S281			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except LI/RO and RI/LO			−1			−1	mA
	LI/RO and RI/LO			−2			−2	
Low-level output current, I_{OL}	Any output except LI/RO and RI/LO			20			20	mA
	LI/RO and RI/LO			10			10	
Clock frequency, f_{clock} (for shifting)		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$		8			8			ns
Data setup time with respect to clock, t_{su}		0↑			0↑			ns
Data hold time with respect to clock, t_h		18↑			18↑			ns
Operating free-air temperature, T_A (see Note 2)		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

NOTE 2: An SN54S281 in the W package operating at free-air temperatures above 110°C requires a heat sink that provides thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 20°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S281			SN74S281			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	Any input except LI/RO and RI/LO	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	Any output except LI/RO and RI/LO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.5	3.4		2.7	3.4		V
		LI/RO, RI/LO			2.4	3.4		2.4	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	RS0, RS1	V_{CC} = MAX, V_I = 2.7 V, See Note 3				50			50	μA
		M, Clock					150			150	
		LI/RO, RI/LO					200			200	
		AS2					300			300	
		All others					250			250	
I_{IL}	Low-level input current	RS0, RS1, LI/RO	V_{CC} = MAX, V_I = 0.5 V, See Note 3				−2			−2	mA
		RI/LO					−3			−3	
		M, Clock					−4			−4	
		AS0, AS1					−6			−6	
		All others					−8			−8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−110	−40		−110	mA
I_{CC}	Supply current		V_{CC} = MAX, T_A = 125°C	W package only			190				mA
			V_{CC} = MAX	All packages		144	230		144	230	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

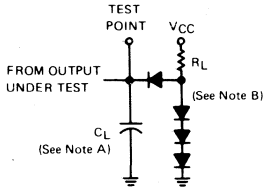
NOTE 3. When testing input current at the RI/LO or LI/RO terminals, the output under test must be in the high-impedance (off) state.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

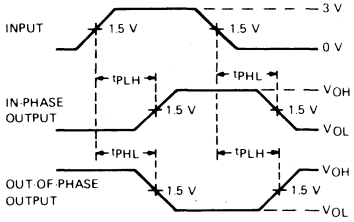
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}	C_L = 15 pF, I/O outputs: R_L = 560 Ω, Other outputs: R_L = 280 Ω, See Figure 1		10	20	ns
t_{PHL}					10	20	
t_{PLH}	Any A	C_{n+4}			18	30	ns
t_{PHL}					18	30	
t_{PLH}	C_n	Any F			10	20	ns
t_{PHL}					10	20	
t_{PLH}	Any A	$\overline{G}$			14	24	ns
t_{PHL}					14	24	
t_{PLH}	Any A	$\overline{P}$			12	20	ns
t_{PHL}					12	20	
t_{PLH}	A_i	F_i			20	35	ns
t_{PHL}					20	35	
t_{PLH}	A_0	RI/LO			30	45	ns
t_{PHL}					30	45	
t_{PLH}	A_3	LI/RO			30	45	ns
t_{PHL}					30	45	
t_{PLH}	F_0	RI/LO			7	11	ns
t_{PHL}					7	11	
t_{PLH}	F_3	LI/RO			7	11	ns
t_{PHL}					7	11	
t_{PLH}	Any AS	Any F or C_{n+4}			28	45	ns
t_{PHL}					28	45	
t_{PLH}	Any AS	$\overline{P}$ or $\overline{G}$			20	33	ns
t_{PHL}					20	33	
t_{PLH}	Clock	Any F			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Clock	RI/LO or LI/RO			35	55	ns
t_{PHL}					35	55	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

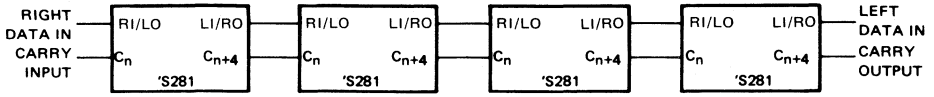


VOLTAGE WAVEFORMS

NOTES: A. Input pulse is supplied by a generator having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L inlcudes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

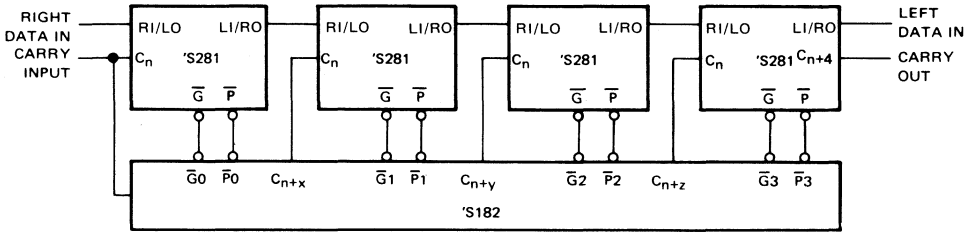
FIGURE 1

TYPICAL APPLICATION DATA



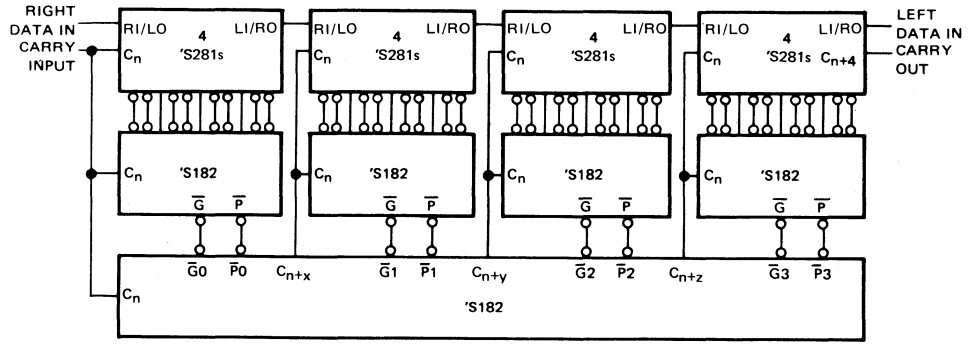
ENTER AND STORE TIME: 38 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 44 ns typical

FIGURE A–16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS IN RIPPLE-CARRY MODE



ENTER AND STORE TIME: 37 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 29 ns typical

FIGURE B–16-BIT BINARY ACCUMULATOR USING FOUR SN54S281/SN74S281 CIRCUITS AND ONE SN54S182/SN74S182 IN FULL LOOK-AHEAD CARRY MODE



ENTER AND STORE TIME: 42 ns typical
EACH SUCCESSIVE ADDITION TO STORED DATA: 34 ns typical

FIGURE C–64-BIT BINARY ACCUMULATOR USING 16 SN54S281/SN74S281 CIRCUITS AND FIVE SN54S182/SN74S182 CIRCUITS FOR FULL CARRY LOOK-AHEAD

A inputs and F outputs of 'S281 are not shown.

TYPES SN54283, SN54LS283, SN54S283, SN74283, SN74LS283, SN74S283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

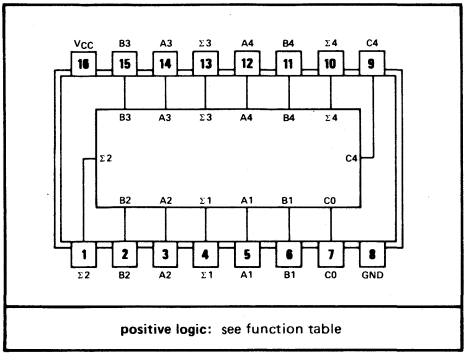
BULLETIN NO. DL-S 7611832, OCTOBER 1976

- Full-Carry Look-Ahead Across the Four Bits
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

TYPICAL ADD TIMES

TYPE	TWO 8-BIT WORDS	TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER ADDER
'283	23ns	43ns	310 mW
'LS283	25ns	45ns	95 mW
'S283	15ns	30ns	510 mW

SN54283, SN54LS283 . . . J OR W PACKAGE
SN54S283 . . . J PACKAGE
SN74283, SN74LS283, SN74S283 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

The '283 and 'LS283 adders are electrically and functionally identical to the '83A and 'LS283, respectively; only the arrangement of the terminals has been changed. The 'S283 high performance versions are also functionally identical.

These improved full adders perform the addition of two 4-bit binary words. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look-ahead across all four bits generating the carry term in ten nanoseconds, typically, for the '283 and 'LS283, and 7.5 nanoseconds for the 'S283. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form. End around carry can be accomplished without the need for logic or level inversion.

Series 54, Series 54LS, and Series 54S circuits are characterized for operation over the full temperature range of −55°C to 125°C. Series 74, Series 74LS, and Series 74S circuits are characterized for 0°C to 70°C operation.

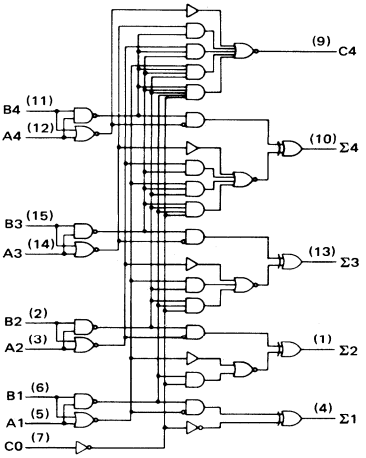
FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L			OUTPUT: WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A2	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

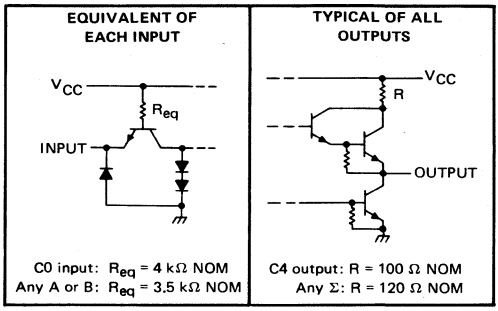
H = high level, L = low level

NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

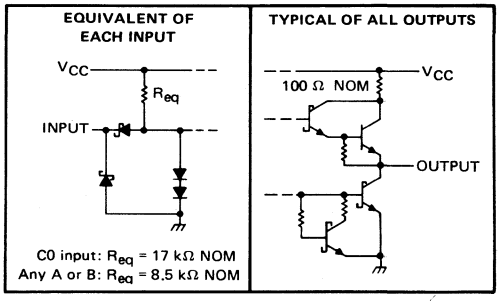
functional block diagram and schematics of inputs and outputs



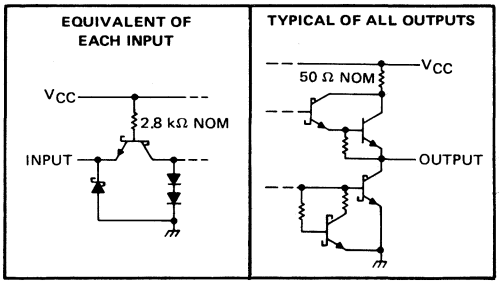
'283



'LS283



'S283



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7V
Input voltage: '283, 'S283	5.5V
'LS283	7V
Interemitter voltage (see Note 2)	5.5V
Operating free-air temperature range; SN54283, SN54LS283, SN54S283	−55°C to 125°C
SN74283, SN74LS283, SN74S283	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.

2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '283 and 'S283 only between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

recommended operating conditions

		SN54283			SN74283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−800			−800	μA
	Output C4			−400			−400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54283			SN74283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−20		−55	−18		−55	mA
		Output C4			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
				All inputs at 4.5 V		66	99		66	110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 780 Ω, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54LS283			SN74LS283			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS283			SN74LS283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Any A or B	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
		C0					0.1			0.1	
I_{IH}	High-level input current	Any A or B	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		C0					20			20	
I_{IL}	Low-level input current	Any A or B	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		C0					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All inputs grounded		22	39		22	39	mA
				All B low, other inputs at 4.5 V		19	34		19	34	
				All inputs at 4.5 V		19	34		19	34	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 2 kΩ, See Note 4		16	24	ns
t_{PHL}					15	24	
t_{PLH}	A_i or B_i	Σ_i			15	24	ns
t_{PHL}					15	24	
t_{PLH}	C0	C4			11	17	ns
t_{PHL}					11	22	
t_{PLH}	A_i or B_i	C4			11	17	ns
t_{PHL}					12	17	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

		SN54S283			SN74S283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−1			−1	mA
	Output C4			−500			−500	μA
Low-level output current, I_{OL}	Any output except C4			20			20	mA
	Output C4			10			10	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S283	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		V
		SN74S283	V_{IL} = 0.8 V,	I_{OH} = MAX	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−2	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−40		−100	mA
		Output C4			−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		80		mA
				All inputs at 4.5 V		95	160	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 280 Ω, See Note 3		11	18	ns
t_{PHL}					12	18	
t_{PLH}	A_i or B_i	Σ_i			12	18	ns
t_{PHL}					11.5	18	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 560 Ω, See Note 3		6	11	ns
t_{PHL}					7.5	11	
t_{PLH}	A_i or B_i	C4			7.5	12	ns
t_{PHL}					8.5	12	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54284, SN54285, SN74284, SN74285
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

BULLETIN NO. DL-S 7211741, MAY 1972—REVISED DECEMBER 1972

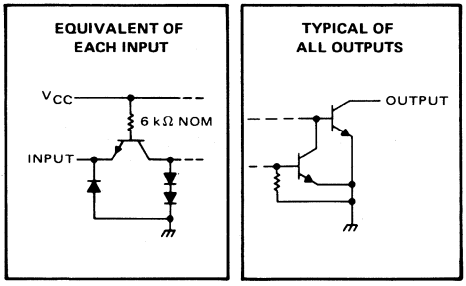
- Fast Multiplication of Two Binary Numbers 8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications: 16-Bit Product in 70 ns Typical 32-Bit Product in 103 ns Typical
- Fully Compatible with Most DTL and TTL Circuits
- Diode-Clamped Inputs Simplify System Design

description

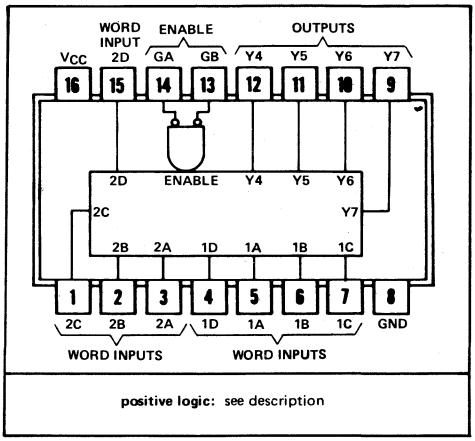
These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N × M bit multipliers.

schematics of inputs and outputs

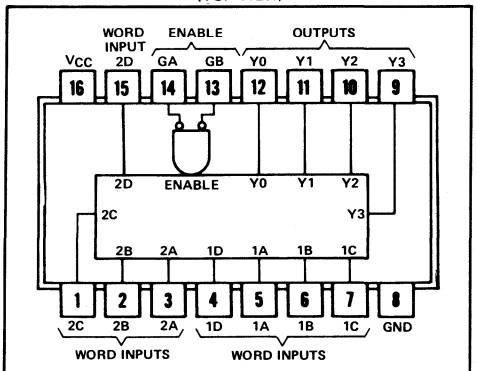


SN54284 . . . J OR W PACKAGE
SN74284 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

SN54285 . . . J OR W PACKAGE
SN74285 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

The SN54284 and SN54285 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

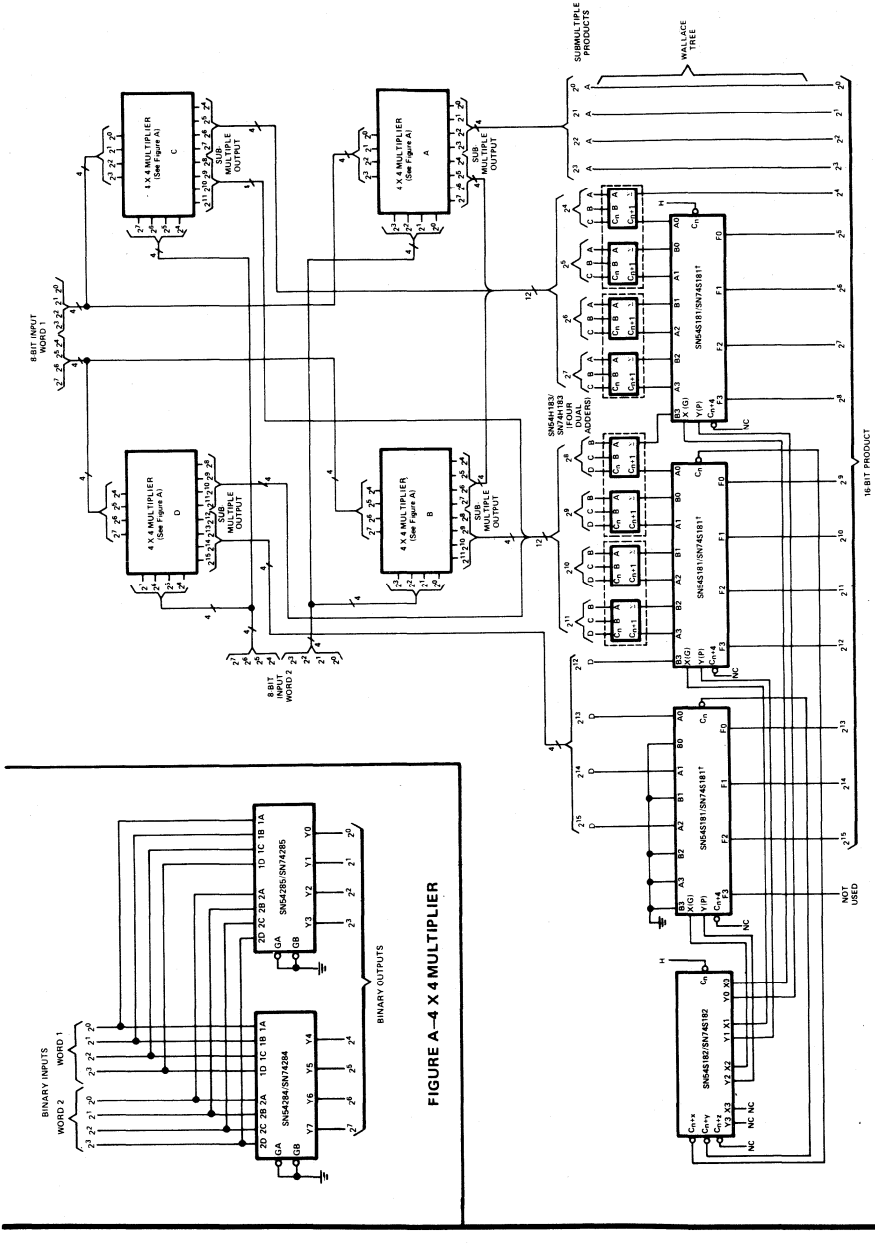


FIGURE A–4 X 4 MULTIPLIER

FIGURE B–8 X 8 MULTIPLIER

†Other terminals of the three SN54S181/SN74S181 ALU's are connected as follows: S3 = H, S2 = L, S1 = L, S0 = H, M = L. Output A = B is not used for this application.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54284 SN54285			SN74284 SN74285			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CC}	Supply current	V_{CC} = MAX, T_A = 125°C, See Note 2	SN54284, SN54285 N package only			99	mA
		V_{CC} = MAX, See Note 2	SN54284, SN54285		92	110	
			SN74284, SN74285		92	130	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF to GND, R_{L1} = 300 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from word inputs			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from word inputs			40	60	

NOTE 3: Load circuit is as described above; waveforms are shown on page 3-10.

TYPES SN54290, SN54293, SN54LS290, SN54LS293
SN74290, SN74293, SN74LS290, SN74LS293
DECADE AND 4-BIT BINARY COUNTERS

BULLETIN NO. DL-S 7611833, MARCH 1974—REVISED OCTOBER 1976

'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

- GND and V_{CC} on Corner Pins (Pins 7 and 14 Respectively)

description

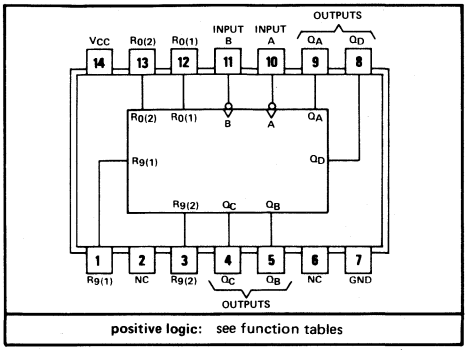
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

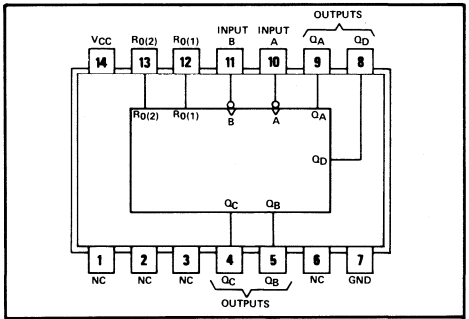
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

SN54290, SN54LS290 . . . J OR W PACKAGE
SN74290, SN74LS290 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

SN54293, SN54LS293 . . . J OR W PACKAGE
SN74293, SN74LS293 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function tables

NC—No internal connection

'290, 'LS290
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'290, 'LS290
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'290, 'LS290
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'293, 'LS293
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

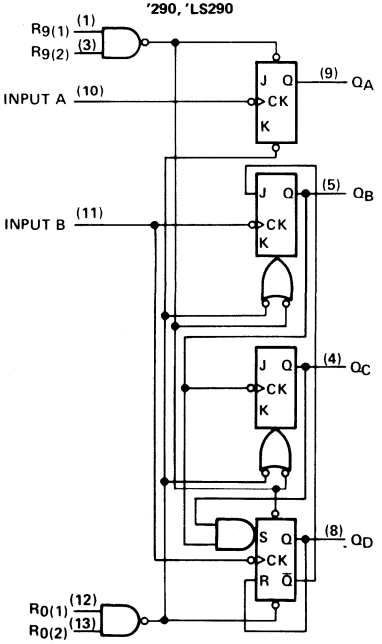
'293, 'LS293
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

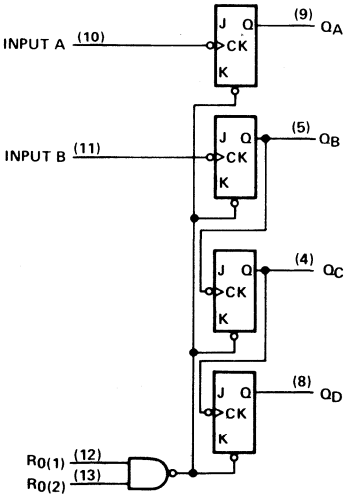
NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagrams

'290, 'LS290

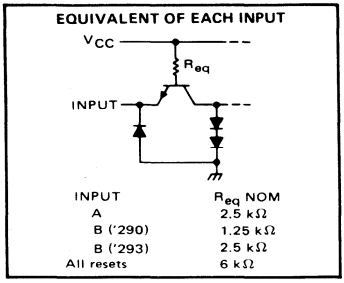


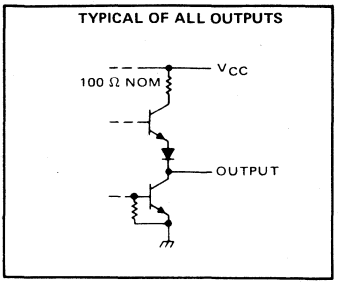
'293, 'LS293



The J and K inputs shown without connection are for reference only and are functionally at a high level.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '290 circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN54'			SN74'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'290			'293			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		A input					80			80	
		B input					120			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		A input					−3.2			−3.2	
		B input					−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			29	42		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

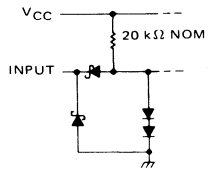
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 4	32	42		32	42		MHz
	B	Q_B		16			16			
t_{PLH}	A	Q_A			10	16		10	16	ns
t_{PHL}					12	18		12	18	
t_{PLH}	A	Q_D			32	48		46	70	ns
t_{PHL}					34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16	ns
t_{PHL}					14	21		14	21	
t_{PLH}	B	Q_C			21	32		21	32	ns
t_{PHL}					23	35		23	35	
t_{PLH}	B	Q_D			21	32		34	51	ns
t_{PHL}					23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30				ns
t_{PHL}		Q_B, Q_C			26	40				

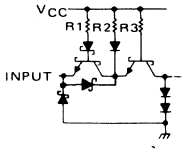
◇f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are the same as those shown for the '90A and '93A, page 3-10.

schematics of inputs and outputs

EQUIVALENT OF EACH RESET INPUT

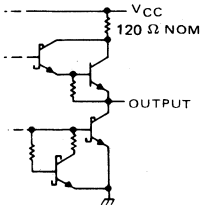


EQUIVALENT OF A AND B INPUTS



INPUT	NOMINAL VALUES R1	R2	R3
A	10 kΩ	10 kΩ	10 kΩ
B ('LS290)	6.7 kΩ	6.7 kΩ	5 kΩ
B ('LS293)	15 kΩ	15 kΩ	10 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 5) . . . . . 7 V
Input voltage: R inputs . . . . . 7 V
A and B inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293 . . . . . −55°C to 125°C
SN74LS290, SN74LS293 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		A input	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
		B of 'LS290						0.4			0.4	
		B of 'LS293						0.2			0.2	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		A input						40			40	
		B of 'LS290						80			80	
		B of 'LS293						40			40	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		A input						−2.4			−2.4	
		B of 'LS290						−3.2			−3.2	
		B of 'LS293						−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3	'LS290		9	15		9	15	mA
					'LS293		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS290 MIN	'LS290 TYP	'LS290 MAX	'LS293 MIN	'LS293 TYP	'LS293 MAX	UNIT
f_{max}	A	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Note 6	32	42		32	42		MHz
	B	Q_B		16			16			
t_{PLH}	A	Q_A			10	16		10	16	ns
t_{PHL}					12	18		12	18	
t_{PLH}	A	Q_D			32	48		46	70	ns
t_{PHL}					34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16	ns
t_{PHL}					14	21		14	21	
t_{PLH}	B	Q_C			21	32		21	32	ns
t_{PHL}					23	35		23	35	
t_{PLH}	B	Q_D			21	32		34	51	ns
t_{PHL}					23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30				ns
t_{PHL}		Q_B, Q_C			26	40				

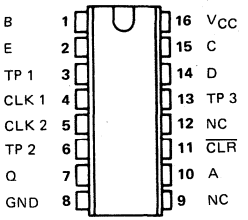
◇f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 6: Load circuit and voltage waveforms are the same as those shown for the 'LS90 and 'LS93, pages 7-70

TYPES SN54LS292, SN54LS294, SN74LS292, SN74LS294
PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

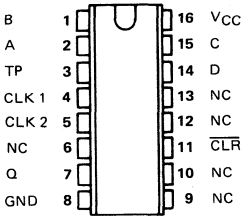
D2628, JANUARY 1981

- Count Divider Chain
- Digitally Programmable from 2^2 to 2^n ($n = 31$ for 'LS292, $n = 15$ for 'LS294)
- Useable Frequency Range from DC to 30 MHz
- Easily Expandable
- Applications
  - Frequency Division
  - Digital Timing

SN54LS292 . . J OR W PACKAGE
SN74LS292 . . J OR N PACKAGE
(TOP VIEW)



SN54LS294 . . J OR W PACKAGE
SN74LS294 . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

description

These programmable frequency dividers/digital timers contain 31 flip-flops ('LS292) or 15 flip-flops ('LS294) plus 30 gates on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'LS292 and TP on the 'LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the function table below.)

'LS292, 'LS294 FUNCTION TABLE

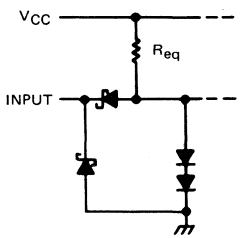
CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

A brief look at the digital timing capabilities of the 'LS292 will show that with a 1-MHz input frequency, programming for 2^{10} will give a period of 1.024 ms, and 2^{20} will give a period of 1.05 sec, 2^{26} will give a period of 1.12 min, and 2^{31} will give a period of 35.79 min.

These devices are easily cascadable giving limitless possibilities to timing delays that can be achieved.

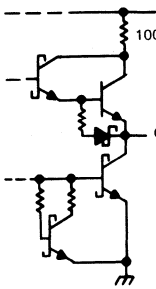
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

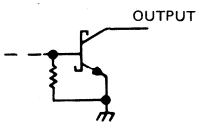


CLK: R_{eq} = 10 kΩ NOM
All others: R_{eq} = 20 kΩ NOM

TYPICAL OF Q OUTPUTS



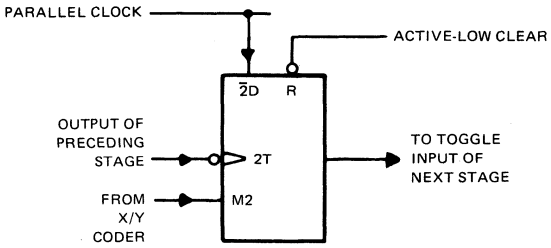
TYPICAL OF TP OUTPUTS



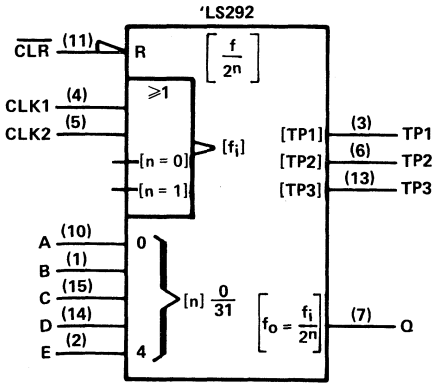
operation

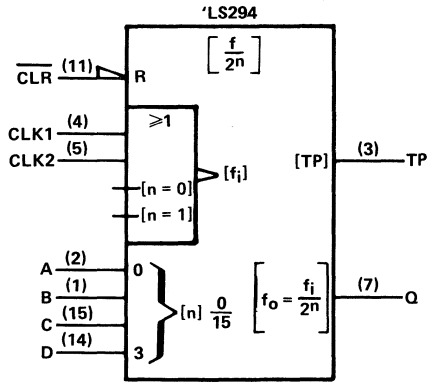
The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode-control inputs of several flip-flops. These flip flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of that flip-flop is enabled, and the signal from the parallel clock line ($f_{in} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



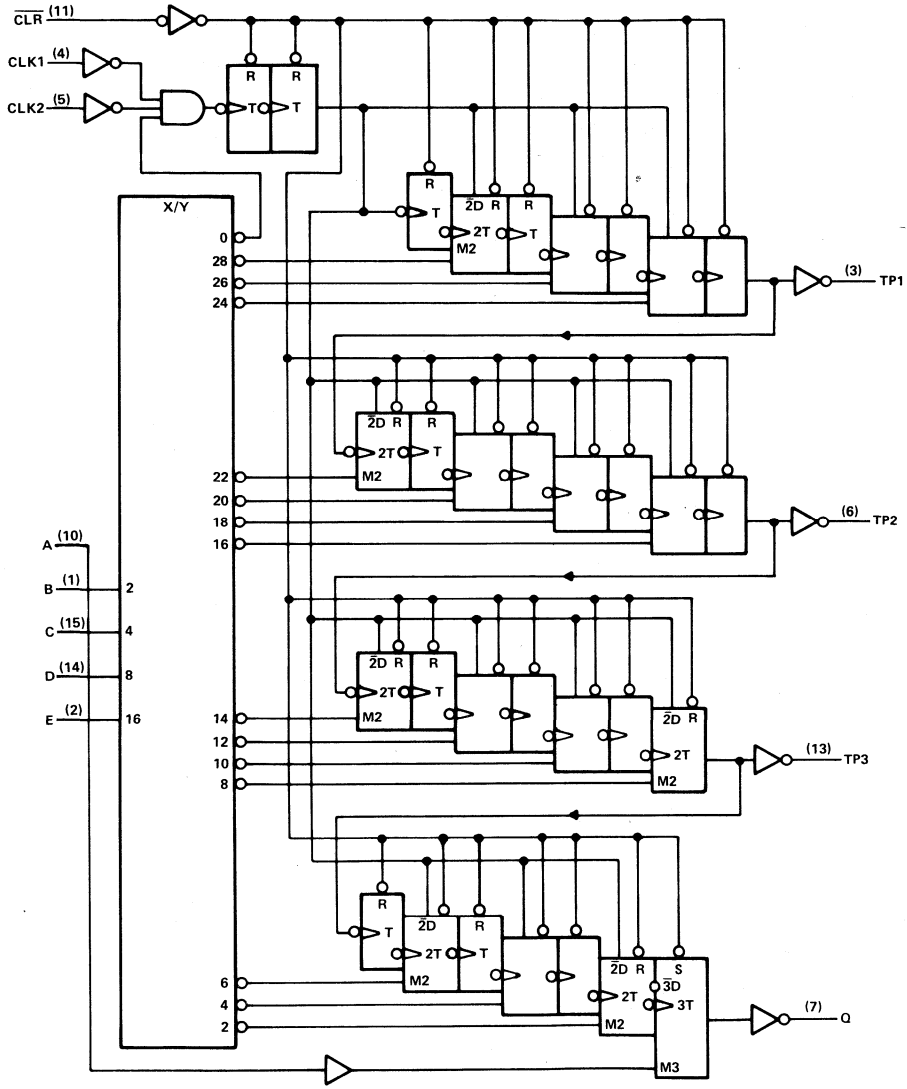
logic symbols





functional block diagram (positive logic)

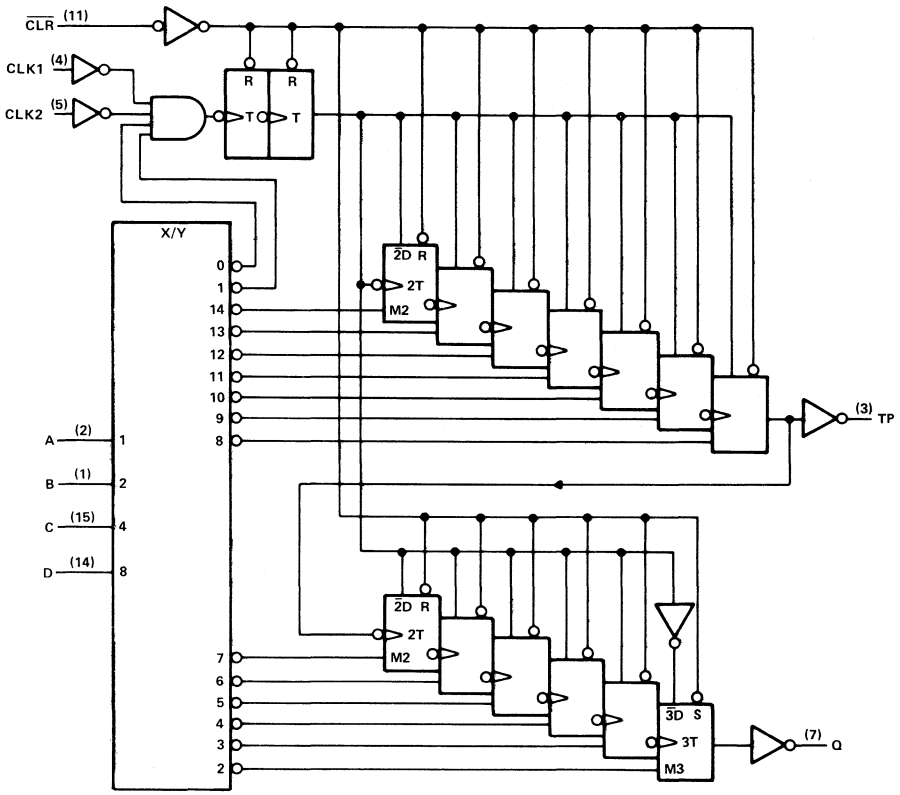
'LS292



7

functional block diagram (positive logic)

'LS294



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS292, SN54LS294 . . . . . −55°C to 125°C
SN74LS292, SN74LS294 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

REVISED OCTOBER 1983

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (Q only)			−1.2			−1.2	mA
Low-level output current, I_{OL} (Q only)			12			24	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock input pulse, t_w	16			16			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1.2 mA,	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		TP♦		I_{OL} = 1 mA					0.25	0.4	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	CLK1, CLK2	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
		All others					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	'LS292	V_{CC} = MAX, All inputs grounded,			40	75		40	75	mA
		'LS294	All outputs open			30	50		30	50	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The duration of the short-circuit should not exceed one second.
♦ The TP output or outputs are not intended to drive external loads but are solely provided for test points.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω, C_L = 45 pF, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS292			'LS294			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CLK 1 or 2			30	50		30	50		MHz
t_{PLH}	CLK1 or 2	Q	Modulo set at 2^2, A thru E = LLLHL ('LS292), A thru D = LLHL ('LS294)		55	90		55	90	ns
t_{PHL}	CLK 1 or 2	Q			80	120		80	120	ns
t_{PHL}	Clear	Q			85	130		85	130	ns

NOTE 2: Voltage waveforms are shown on page 3-11 in Figure 1.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

switching loads

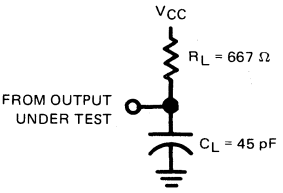


FIGURE 1

'LS292 FUNCTION TABLE

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

'LS294 FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

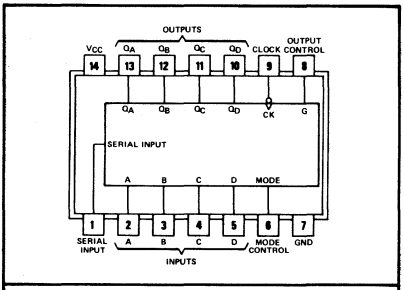
7

TYPES SN54LS295B, SN74LS295B
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7611780, OCTOBER 1976

- 'LS295B Offers Three Times the Sink-Current Capability of 'LS295A
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 80 mW Typical (Enabled)
- Applications:
  - N-Bit Serial-To-Parallel Converter
  - N-Bit Parallel-To-Serial Converter
  - N-Bit Storage Register

SN54LS295B . . . J OR W PACKAGE
SN74LS295B . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

The SN54LS295B is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS295B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
			A	B	C	D				
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

See explanation of function tables on page 3-8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS295B . . . . . −55°C to 125°C
SN74LS295B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS295B			SN74LS295B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$	16			16			ns
Setup time, high-level or low-level data, t_{su}	20			20			ns
Hold time, high-level or low-level data, t_h	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS295B			SN74LS295B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Condition A		20	29		20	29	mA
			Condition B		22	33		22	33	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time,and duration of the short-circuit should not exceed one second.

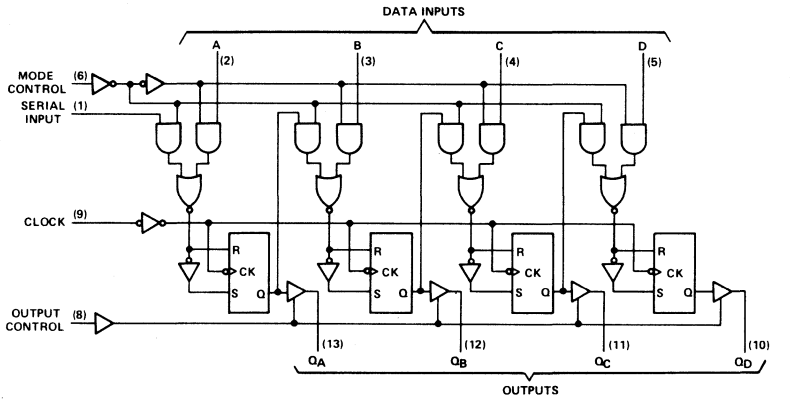
NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:
A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25 C, R_L = 667 Ω

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	C_L = 45 pF, See Note 3	30	45		MHz
t_{PLH} Propagation delay time, low-to-high-level output			14	20	ns
t_{PHL} Propagation delay time, high-to-low-level output			19	30	ns
t_{PZH} Output enable time to high level			18	26	ns
t_{PZL} Output enable time to low level			20	30	ns
t_{PHZ} Output disable time from high level	C_L = 5 pF, See Note 3		13	20	ns
t_{PLZ} Output disable time from low level			13	20	ns

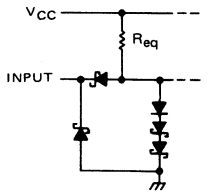
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

functional block diagram



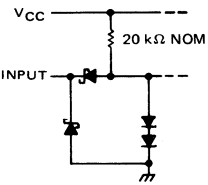
schematics of inputs and outputs

EQUIVALENT OF SERIAL AND DATA INPUTS

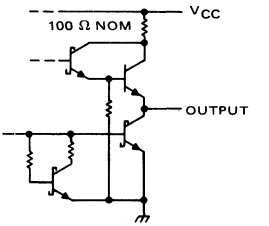


Serial: R_{eq} = 30 kΩ NOM
A, B, C, D: R_{eq} = 20 kΩ NOM

EQUIVALENT OF CLOCK, MODE CONTROL, AND OUTPUT CONTROL INPUTS



TYPICAL OF ALL OUTPUTS

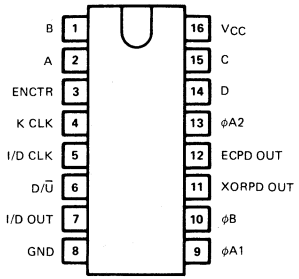


TYPES SN54LS297, SN74LS297
DIGITAL PHASE-LOCKED-LOOP FILTERS

D2629, JANUARY 1981

- **Digital Design Avoids Analog Compensation Errors**
- **Easily Cascadable for Higher Order Loops**
- **Useful Frequency from DC to:**
  50 MHz Typical (K Clock)
  35 MHz Typical (I/D Clock)

SN54LS297 . . . J OR W PACKAGE
SN74LS297 . . . J OR N PACKAGE



description

The SN54LS297 and SN74LS297 devices are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-N counter, to build first order phase-locked loops as described in Figure 1 in the operations section.

Both exclusive-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility.

Proper partitioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation or to cascade to higher order phase-locked loops.

The length of the up/down K counter is digitally programmable according to the K counter function table. With A, B, C, and D all low, the K counter is disabled. With A high and B, C, and D low, the K counter is only three stages long, which widens the bandwidth or capture range and shortens the lock time of the loop. When A, B, C, and D are all programmed high, the K counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwidth by manipulating the A through D inputs can maximize the overall performance of the digital phase-locked loop.

The 'LS297 can perform the classic first-order phase-locked loop function without using analog components. The accuracy of the digital phase-locked loop (DPLL) is not affected by V_{CC} and temperature variations, but depends solely on accuracies of the K clock, I/D clock, and loop propagation delays.

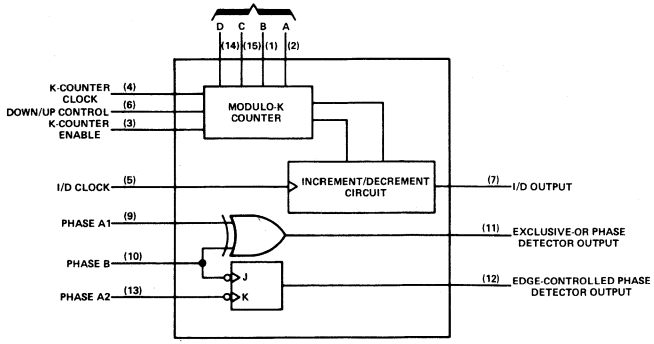
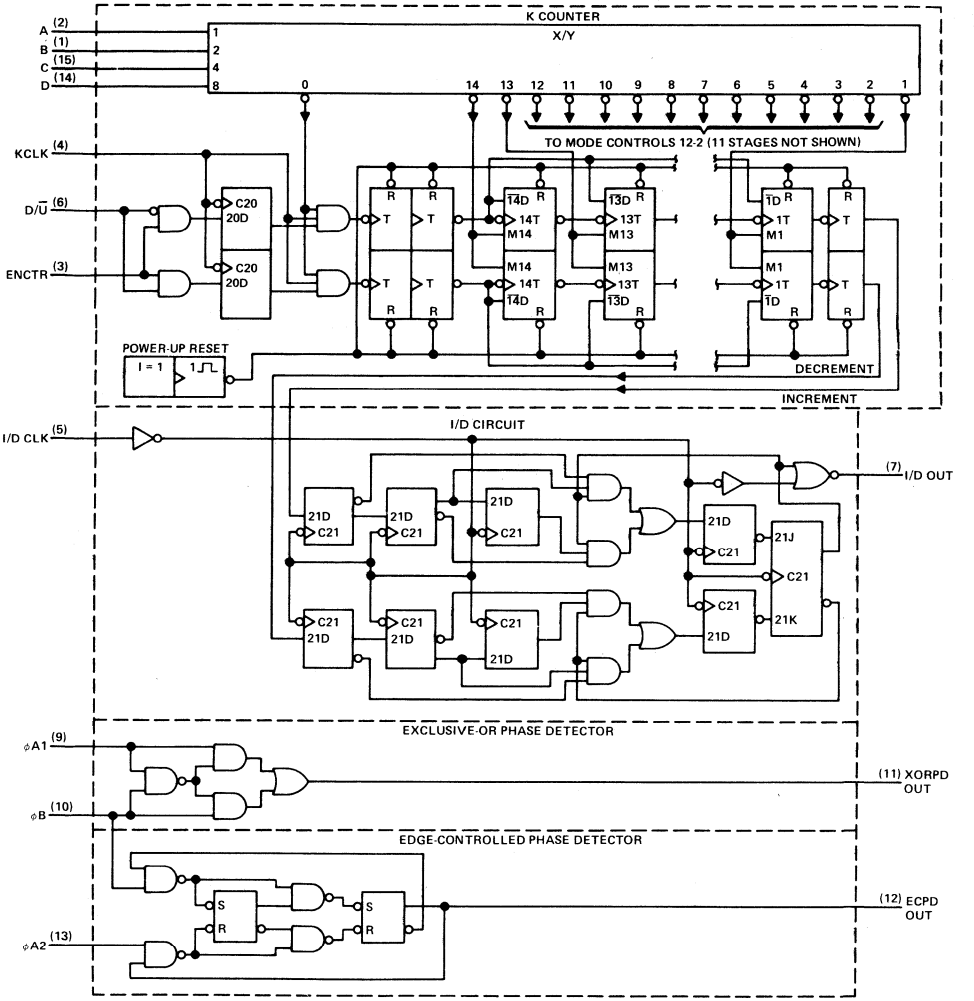


FIGURE 1–SIMPLIFIED BLOCK DIAGRAM

functional block diagram



K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2^3
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

FUNCTION TABLE
EXCLUSIVE-OR PHASE DETECTOR

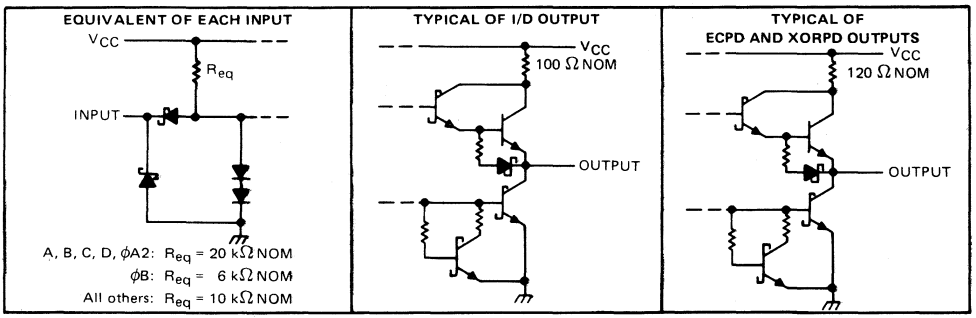
ϕA1	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

FUNCTION TABLE
EDGE-CONTROLLED PHASE DETECTOR

ϕA2	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

H = steady-state high level
L = steady-state low level
↓ = transition from high to low
↑ = transition from low to high

schematics of inputs and outputs



operation

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty cycle square wave. At the limits of linear operation, the phase detector output will be either high or low all of the time, depending on the direction of the phase error ($\phi_{in} - \phi_{out}$). Within these limits, the phase detector output varies linearly with the input phase error according to the gain k_d, which is expressed in terms of phase detector output per cycle of phase error. The phase detector output can be defined to vary between ±1 according to the relation:

$$\text{PD Output} = \frac{\%\ \text{high} - \%\ \text{low}}{100} \qquad (1)$$

The output of the phase detector will be $k_d\ \phi_e$, where the phase error $\phi_e = \phi_{in} - \phi_{out}$.

Exclusive-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function, but can be described generally as a circuit that changes states on one of the transitions of its inputs. k_d for an XORPD is 4 because its output remains high (PD output = 1) for a phase error of 1/4 cycle. Similarly, k_d for the ECPD is 2 since its output remains high for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for ϕ_e defined to be zero. For the basic DPLL system of Figure 2, $\phi_e = 0$ when the phase detector output is a square wave. The XORPD inputs are 1/4 cycle out of phase for zero phase error. For the ECPD, $\phi_e = 0$ when the inputs are 1/2 cycle out of phase.

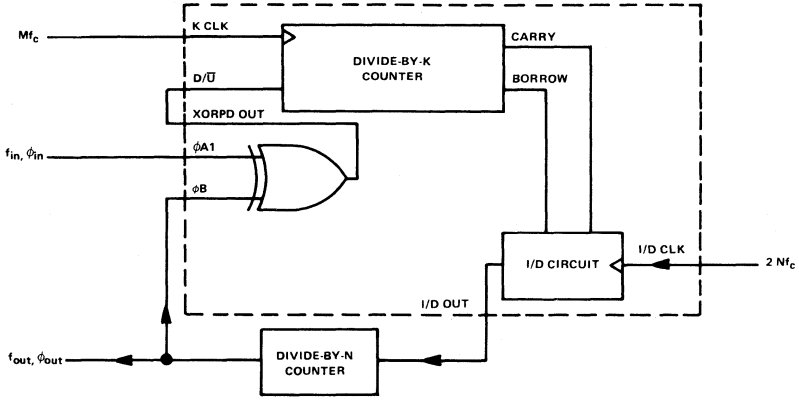


FIGURE 2–DPLL USING EXCLUSIVE-OR PHASE DETECTION

The phase detector output controls the up/down input to the K counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop center frequency f_c. When the K counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K counter will equal the input frequency multiplied by the division ratio. Thus the output from the K counter is $(k_d \phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit, which, in the absence of any carry or borrow pulse, has an output that is 1/2 of the input clock I/D CLK. The input clock is just a multiple, 2N, of the loop center frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D OUT. Thus the output of the I/D circuit will be $Nf_c + (k_d \phi_e Mf_c)/2K$.

The output of the N counter (or the output of the phase-locked loop) is thus:

$$f_o = f_c + (k_d \phi_e Mf_c)/2KN$$

If this result is compared to the equation for a first-order analog phase-locked loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus the simple first-order phase-locked loop with an adjustable K counter is the equivalent of an analog phase-locked loop with a programmable VCO gain.

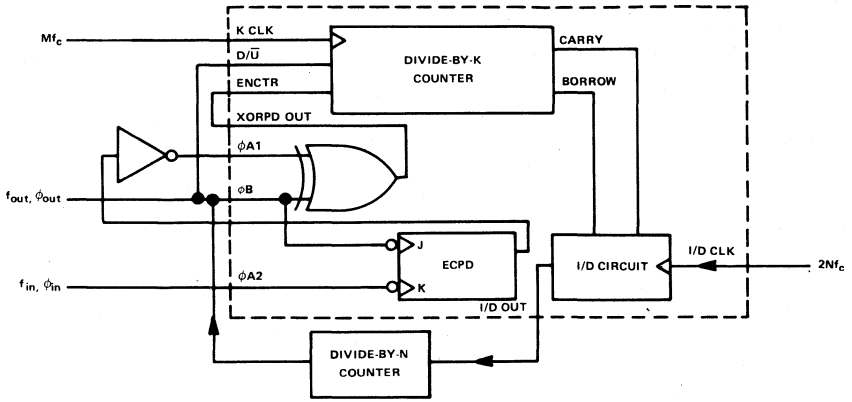


FIGURE 3–DPLL USING BOTH PHASE DETECTORS IN A RIPPLE-CANCELLATION SCHEME

7

absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS297 . . . . . −55°C to 125°C
SN74LS297 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS297			SN74LS297			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	I/D OUT			−1.2			−1.2	mA
	EXOR, ECPD			−400			−400	μA
Low-level output current, I_{OH}	I/D OUT			12			24	mA
	XOR, ECPD			4			8	mA
Clock frequency, f_{clock}	K Clock	0		30	0		30	MHz
	I/D Clock	0		15	0		15	MHz
Width of clock input pulse, t_w	K Clock	16			16			ns
	I/D Clock	33			33			ns
Setup time, t_{su}, to K Clock ↑	U/$\overline{D}$, ENCTR	30			30			ns
Hold time, t_h, from K Clock ↑	U/$\overline{D}$, ENCTR	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS297 MIN	SN54LS297 TYP‡	SN54LS297 MAX	SN74LS297 MIN	SN74LS297 TYP‡	SN74LS297 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	I/D OUT	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = MAX	2.4			2.4			V
		Others		I_{OH} = MAX	2.5			2.7			
V_{OL}	Low-level output voltage	I/D OUT	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Others		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	U/$\overline{D}$, EN, ϕA1	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
		ϕB					60			60	
		All others					20			20	
I_{IL}	Low-level input current	A,B,C,D,ϕA1	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		ϕB	V_I = 0.4 V				−1.2			−1.2	
		All others					−0.8			−0.8	
I_{OS}	Short-circuit output current §	I/D OUT	V_{CC} = MAX		−30		−130	−30		−130	mA
		Others			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, All inputs grounded, All outputs open			75	120		75	120	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are of V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)		TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	KCLK		I/D OUT	R_L = 667 Ω, C_L = 45 pF, See Note 2	30	50		MHz
	I/D CLK		I/D OUT		15	35		
t_{PLH}	I/D CLK ↑		I/D OUT			15	25	ns
t_{PHL}	I/D CLK ↑		I/D OUT			22	35	ns
t_{PLH}	ϕA1 or ϕB	Other input low	XOR OUT	R_L = 2 kΩ, C_L = 45 pF, See Note 2		10	15	ns
	ϕA1 or ϕB	Other input high	XOR OUT			17	25	
t_{PHL}	ϕA1 or ϕB	Other input low	XOR OUT			15	25	ns
	ϕA1 or ϕB	Other input high	XOR OUT			17	25	
t_{PLH}	ϕB ↓		ECPD OUT			20	30	ns
t_{PHL}	ϕA2↓		ECPD OUT			20	30	ns

¶t_{PLH} = propagation delay time, low-to-high level output
t_{PHL} = propagation delay time, high-to-low level output
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11

TYPES SN54298, SN54LS298, SN74298, SN74LS298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

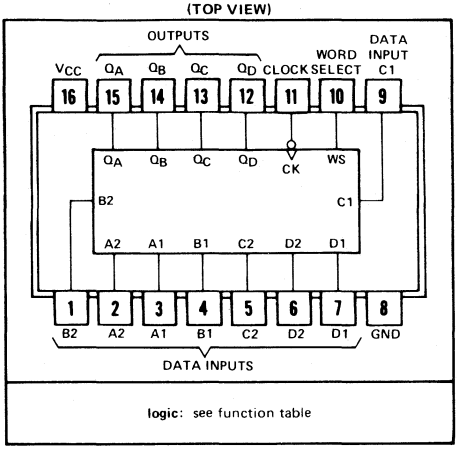
BULLETIN NO. DL-S 7611747, MARCH 1974–REVISED OCTOBER 1976

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

  Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

  Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

SN54298, SN54LS298 . . . J OR W PACKAGE
SN74298, SN74LS298 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 or SN54LS157/SN74LS157 and SN54175/SN74175 or SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applies to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

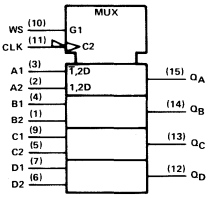
Typical power dissipation is 195 milliwatts for the '298 and 65 milliwatts for the 'LS298. SN54298 and SN54LS298 are characterized for operation over the full military temperature range of −55°C to 125°C; SN74298 and SN74LS298 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

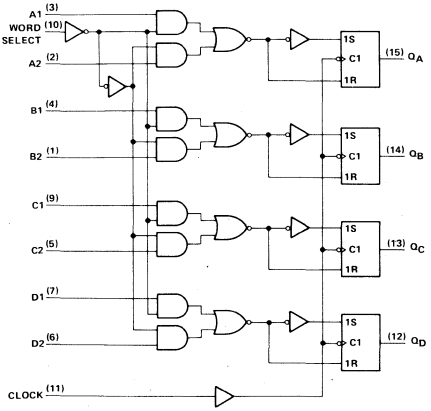
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

logic symbol

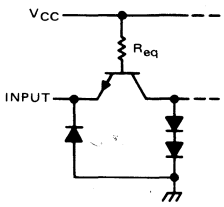


logic diagram (positive logic)



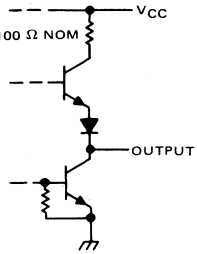
schematics of inputs and outputs

'298
EQUIVALENT OF EACH INPUT

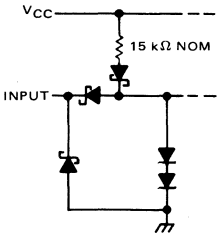


Clock: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 6 kΩ NOM

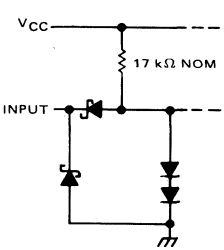
'298
TYPICAL OF ALL OUTPUTS



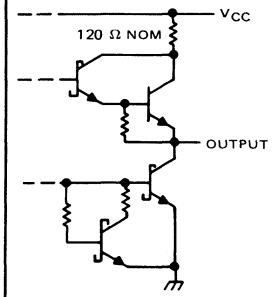
'LS298
EQUIVALENT OF DATA INPUTS



'LS298
EQUIVALENT OF OTHER INPUTS



'LS298
TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54298 . . . . . −55°C to 125°C
SN74298 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54298			SN74298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{su}	Data	15			15			ns
	Word select	25			25			
Hold time, t_h	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54298	−20		−57	mA
			SN74298	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 3		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	

NOTE 3: Load circuit and waveforms are shown on page 3-10.

REVISED OCTOBER 1976

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS298 . . . . . −55°C to 125°C
SN74LS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS298			SN74LS298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{su}	Data	15			15			ns
	Word select	25			25			
Hold time, t_h	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS298			SN74LS298			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			13	21		13	21	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

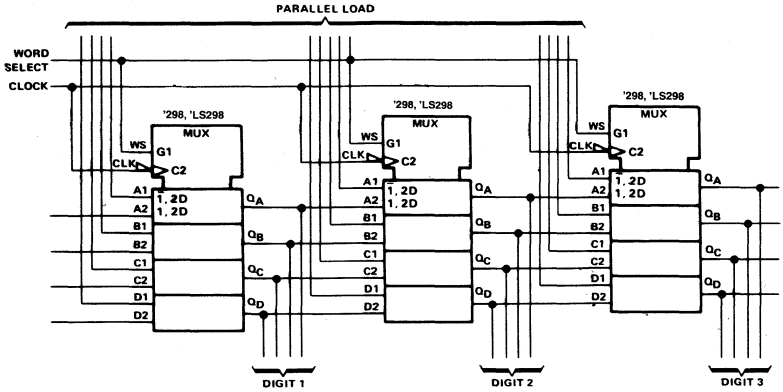
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 kΩ, See Note 4		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	

NOTE 4: Load circuit and waveforms are shown on page 3-11.

TYPICAL APPLICATION DATA

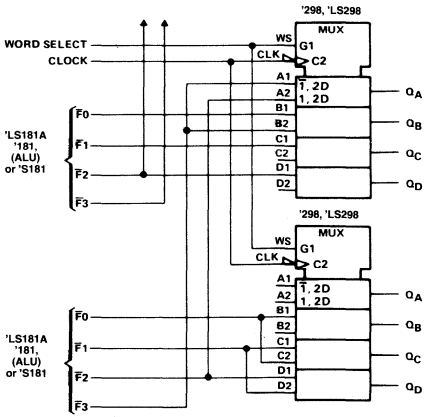
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 or 'LS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

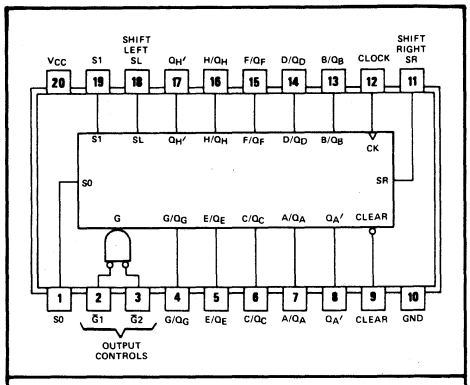
TYPES SN54LS299, SN54S299, SN74LS299, SN74S299
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

BULLETIN NO. DL-S 12115, MARCH 1974—REVISED DECEMBER 1980

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear
- Applications:
  Stacked or Push-Down Registers
  Buffer Storage, and
  Accumulator Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . J PACKAGE
SN74LS299, SN74S299 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These Schottky† TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals. See explanation of function tables on page 3-8.

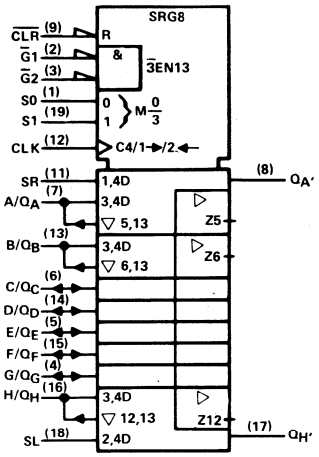
TEXAS INSTRUMENTS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

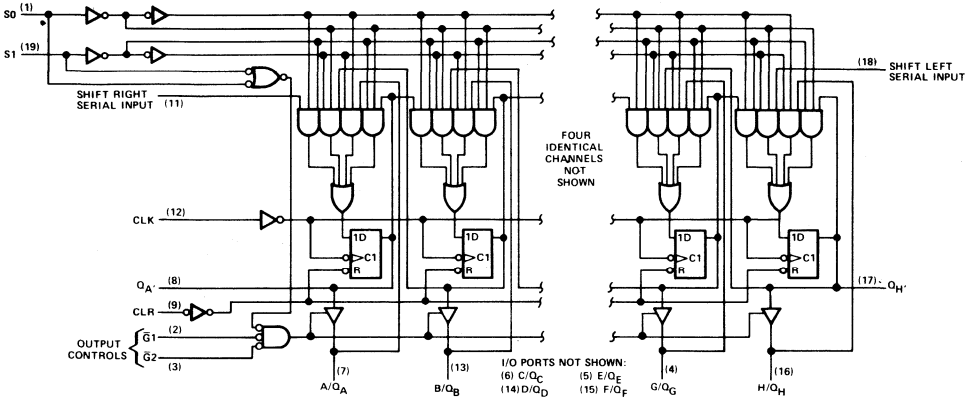
functional block diagram

logic symbols

'LS299, 'S299

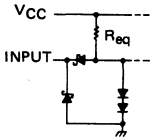


'LS299, 'S299



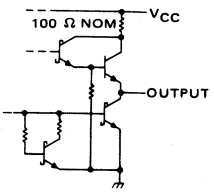
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

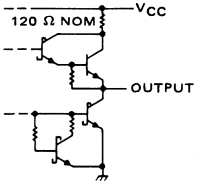


S0, S1: R_{eq} = 9 kΩ NOM
All other inputs: R_{eq} = 18 kΩ NOM

TYPICAL OF OUTPUTS
Q_A THRU Q_H



TYPICAL OF OUTPUTS
$Q_{A'}$ THRU $Q_{H'}$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS299 . . . . . −55°C to 125°C
SN74LS299 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	$Q_{A'}$ or $Q_{H'}$			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	$Q_{A'}$ or $Q_{H'}$			4			8	
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	30			30			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	20			20			ns
Setup time, t_{su}	Select	35↑			35↑			ns
	High-level data◇	20↑			20↑			
	Low-level data◇	20↑			20↑			
	Clear inactive-state	20↑			20↑			
Hold time, t_h	Select	10↑			10↑			ns
	Data◇	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS299			SN74LS299			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		$Q_{A'}$ or $Q_{H'}$	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.5	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		$Q_{A'}$ or $Q_{H'}$	V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	S0, S1	V_{CC} = MAX	V_I = 7 V			200			200	μA
		A thru H		V_I = 5.5 V			100			100	
		Any other		V_I = 7 V			100			100	
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Any other					20			20	
I_{IL}	Low-level input current	S0, S1	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Any other					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX		−30		−130	−30		−130	mA
		$Q_{A'}$ or $Q_{H'}$			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			33	53		33	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

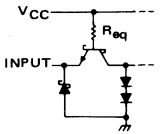
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	25	35		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	33	ns
t_{PHL}					26	39	
t_{PHL}	Clear	$Q_{A'}$ or $Q_{H'}$			27	40	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 2		17	25	ns
t_{PHL}					26	39	
t_{PHL}	Clear	Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			13	21	ns
t_{PZL}					19	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 2		10	15	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11.

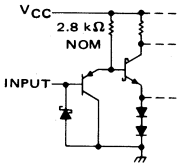
schematics of inputs and outputs

EQUIVALENT OF CLOCK AND CLEAR INPUTS

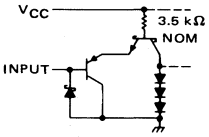


Clock: R_{eq} = 2.8 kΩ NOM
Clear: R_{eq} = 3.5 kΩ NOM

EQUIVALENT OF $\overline{G1}$ AND $\overline{G2}$ INPUTS

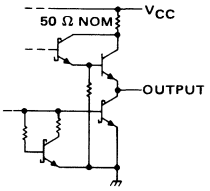


EQUIVALENT OF A THRU H†, S0, S1, SHIFT RIGHT, AND SHIFT LEFT INPUTS

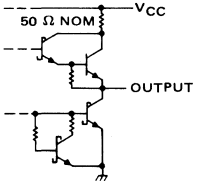


†When 3-state outputs are disabled.

TYPICAL OF OUTPUTS Q_A THRU Q_H



TYPICAL OF OUTPUTS $Q_{A'}$ AND $Q_{H'}$



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S299 (see Note 2) . . . . . −55°C to 125°C
SN74S299 . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTES 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−2			−6.5	mA
	$Q_{A'}$ or $Q_{H'}$			−0.5			−0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	$Q_{A'}$ or $Q_{H'}$			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15↑			15↑			ns
	High-level data◇	7↑			7↑			
	Low-level data◇	5↑			5↑			
	Clear inactive-state	10↑			10↑			
Hold time, t_h	Select	5↑			5↑			ns
	Data◇	5↑			5↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.2		V
		$Q_{A'}$ or $Q_{H'}$		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−250	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A thru H, S0, S1	V_{CC} = MAX, V_I = 2.7 V			100	μA
		Any other				50	
I_{IL}	Low-level input current	Clock or clear	V_{CC} = MAX, V_I = 0.5 V			−2	mA
		Any other				−250	μA
		S0, S1				−500	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX	−40		−100	mA
		$Q_{A'}$ or $Q_{H'}$		−20		−100	
I_{CC}	Supply current		V_{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	50	70		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 1 kΩ, See Note 2		12	20	ns
t_{PHL}					13	20	
t_{PHL}	Clear	$Q_{A'}$ or $Q_{H'}$			14	21	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 280 Ω, See Note 2		15	21	ns
t_{PHL}					15	21	
t_{PHL}	Clear	Q_A thru Q_H			16	24	ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			10	18	ns
t_{PZL}					12	18	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 280 Ω, See Note 3		7	12	ns
t_{PLZ}					7	12	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 3: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-10.

TYPES SN54LS320, SN54LS321, SN74LS320, SN74LS321
CRYSTAL-CONTROLLED OSCILLATORS

D2418, DECEMBER 1978 – REVISED JANUARY 1981

'LS320

- **Crystal-Controlled Oscillator Operation from 1 MHz to 20 MHz**
- **2-Phase Driver Outputs**

'LS321

- **Similar to 'LS320 But Includes f/2 and f/4 Count-Down Outputs**

description

The 'LS320 is a crystal-controlled oscillator/clock driver. It features complementary standard and high-current driver outputs. A synchronization flip-flop is included.

The driver outputs, F' and $\overline{F}$' have very-low impedance and can be used to drive highly capacitive TTL-level lines. If the driver outputs are not used, then the V_{CC}' terminal can be left open.

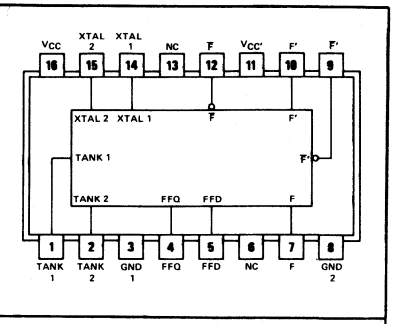
The 'LS321 is identical to the 'LS320 except it additionally features two count-down outputs, F/2 and F/4.

These circuits were designed for series reasonent crystal control of frequency, and capacitative control is not recommended. If a fundamental crystal is used an inductor of 5 to 100 μH with a Q_L of 30 to 40 is required to be connected between the tank 1 and tank 2 inputs. If a third overtone crystal is used, a tuned tank is necessary. The XTAL 1 and XTAL 2 inputs have an input capacitance of 6 to 8 pF.

Interaction of the driver outputs with the other outputs limits useful frequencies as shown in the frequency-limits table.

The SN54LS320 and SN54LS321 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS320 and SN74LS321 are characterized for operation from 0°C to 70°C.

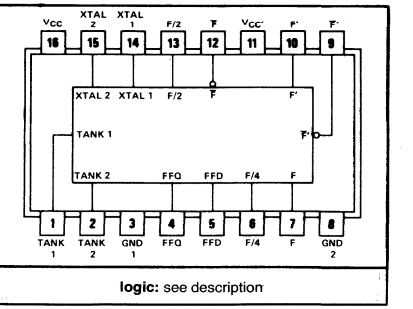
SN54LS320 . . . J OR W PACKAGE
SN74LS320 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description

NC—No internal connection

SN54LS321 . . . J OR W PACKAGE
SN74LS321 . . . J OR N PACKAGE
(TOP VIEW)

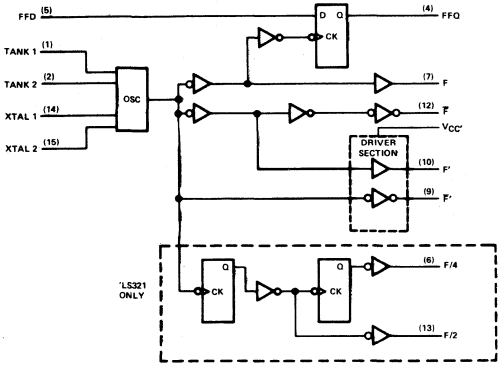


logic: see description

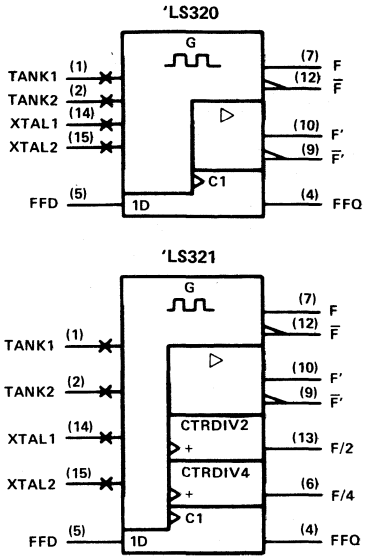
FREQUENCY LIMITS

OUTPUTS IN USE	V_{CC}	V_{CC}'	f_{max}
Driver outputs only	5 V	5 V	20 MHz
Other outputs only	5 V	Open	20 MHz
Driver and any other outputs	5 V	5 V	10 MHz

functional block diagram (positive logic)



logic symbols



7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Supply voltage, V_{CC}' . . . . . 7 V
Input voltage to FFD terminal . . . . . −0.5 V to 7 V
Operating free-air temperature range: SN54LS320, SN54LS321 . . . . . −55°C to 125°C
SN74LS320, SN74LS321 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminals.

recommended operating conditions

		SN54LS320 SN54LS321			SN74LS320 SN74LS321			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Supply voltage, V_{CC}'		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	F' or $\overline{F}$'			−12			−24	mA
	F, $\overline{F}$, F/2, F/4			−0.4			−0.4	
Low-level output current, I_{OL}	F' or $\overline{F}$'			12			24	mA
	F, $\overline{F}$, F/2, F/4			4			8	
Output frequency, f_{out}	F/2 ('LS321)	0.5		10	0.5		10	MHz
	F/4 ('LS321)	0.25		5	0.25		5	
	F or $\overline{F}$	1		20	1		20	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS320 SN54LS321			SN74LS320 SN74LS321			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	V_{CC}' = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	F′, $\overline{F}$′	V_{CC} = 4.5 V,	V_{CC}' = 4.5 V,	I_{OH} = −12 mA	2.5	3.3					V
			V_{CC} = 4.75 V,	V_{CC}' = 4.75 V,	I_{OH} = −24 mA				2.7	3.3		
		Others	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	F′, $\overline{F}$′	V_{CC} = MIN,	V_{CC}' = MIN	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
		Others	V_{CC} = MIN,	V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current from V_{CC}		V_{CC} = MAX,	FFD at GND	'LS320		42	70		42	70	mA
					'LS321		47	75		47	75	
I_{CC}'	Supply current from V_{CC}'		V_{CC} = MAX,	V_{CC}' = MAX,	FFD at GND		4	8		4	8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, V_{CC}' = 5 V, and T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Outputs F′ and $\overline{F}$′ do not have short-circuit protection and these limits do not apply.

switching characteristics, V_{CC} = 5 V, V_{CC}' = 5 V, T_A = 25°C

PARAMETER		OUTPUTS	TEST CONDITIONS¶		'LS320			'LS321			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum operating frequency	F/2	C_L = 100 pF					10	15		MHz
		F/4						5	7.5		
		All others			20	30		20	30		
t_r	Rise time, 1 V to 3 V	F′, $\overline{F}$′	C_L = 50 pF			6	12		6	12	ns
			C_L = 100 pF			7	14		7	14	
			C_L = 200 pF			7	14		7	14	
		Others	C_L = 50 pF			11	22		11	22	
			C_L = 100 pF			25	40		25	40	
			C_L = 200 pF			45	70		45	70	
t_f	Fall time, 3 V to 1 V	F′, $\overline{F}$′	C_L = 50 pF			5	10		5	10	ns
			C_L = 100 pF			5	10		5	10	
			C_L = 200 pF			6	12		6	12	
		Others	C_L = 50 pF			6	12		6	12	
			C_L = 100 pF			10	20		10	20	
			C_L = 200 pF			17	30		17	30	

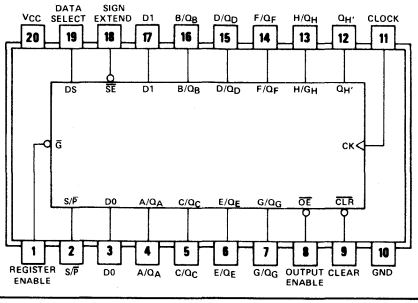
¶ Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS322A, SN74LS322A
8-BIT SHIFT REGISTERS WITH SIGN EXTEND

D2411, OCTOBER 1977 – REVISED JANUARY 1981

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- 3-State Outputs Drive Bus Lines Directly
- Sign Extend Function
- Direct Overriding Clear
- Equivalent to 25LS22

SN54LS322A . . . J PACKAGE
SN74LS322A . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These low-power Schottky eight-bit shift registers feature multiplexed input/output data ports to achieve full eight-bit data handling in a single 20-pin package. Serial data may be entered into the shift-right register through either the D0 or the D1 input as selected by the data select input. A serial output (Q_H') is also provided to facilitate expansion. Synchronous parallel loading is accomplished by taking both the register enable and the $S/\overline{P}$ inputs low. This places the three-state input/output ports in the data input mode. Data are entered on the low-to-high transition of the clock. The data extend function repeats the sign in the Q_A flip-flop during shifting. A direct overriding clear input clears the internal registers when taken low whether the outputs are enabled or off. The output enable does not interfere with synchronous operation of the register.

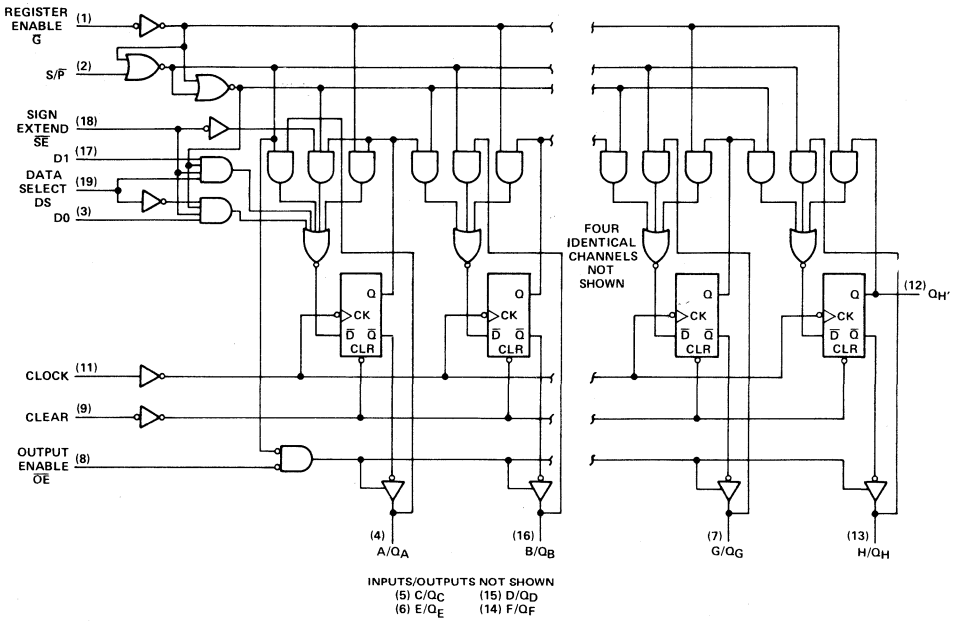
FUNCTION TABLE

OPERATION	INPUTS							INPUTS/OUTPUTS				OUTPUT
	CLEAR	REGISTER ENABLE	$S/\overline{P}$	SIGN EXTEND	DATA SELECT	OUTPUT ENABLE	CLOCK	A/Q_A	B/Q_B	$C/Q_C \ldots H/Q_H$		Q_H'
Clear	L	H	X	X	X	L	X	L	L	L	L	L
	L	X	H	X	X	L	X	L	L	L	L	L
Hold	H	H	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}	Q_{H0}
Shift Right	H	L	H	H	L	L	↑	D0	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
	H	L	H	H	H	L	↑	D1	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Sign Extend	H	L	H	L	X	L	↑	Q_{An}	Q_{An}	Q_{Bn}	Q_{Gn}	Q_{Gn}
Load	H	L	L	X	X	X	↑	a	b	c	h	h

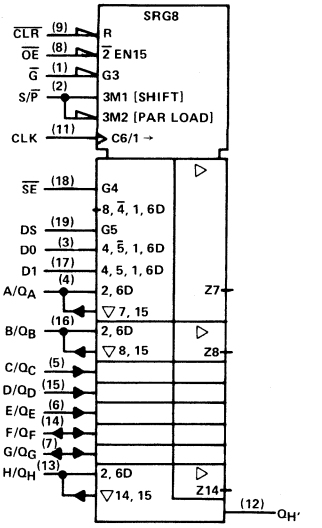
When the output enable is high, the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected. If both the register enable input and the $S/\overline{P}$ input are low while the clear input is low, the register is cleared while the eight input/output terminals are disabled to the high-impedance state.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$Q_{A0} \ldots Q_{H0}$ = the level of Q_A through Q_H, respectively, before the indicated steady-state conditions were established
$Q_{An} \ldots Q_{Hn}$ = the level of Q_A through Q_H, respectively, before the most recent ↑ transition of the clock
D0, D1 = the level of steady-state inputs at inputs D0 and D1 respectively
a . . . h = the level of steady-state inputs at inputs A through H respectively

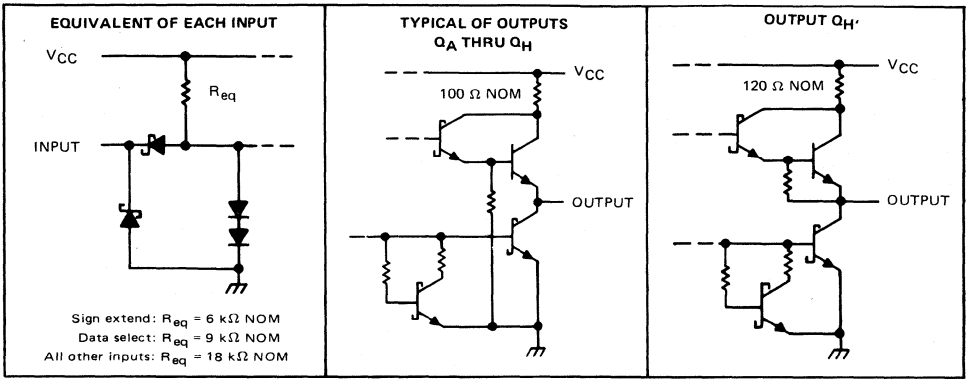
functional block diagram (positive logic)



logic symbol



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS322A . . . . . −55°C to 125°C
SN74LS322A . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS322A			SN74LS322A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			−1			−2.6	mA
	Q_H'			−0.4			−0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_H'			4			8	
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	30			30			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	20			20			ns
Setup time, t_{su}	Data select	10↑			10↑			ns
	High-level data◇	20↑			20↑			
	Low-level data◇	20↑			20↑			
	Clear inactive-state	20↑			20↑			
Hold time, t_h	Data select	10↑			10↑			ns
	Data◇	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

◇Data includes the two serial inputs and the eight input/output data lines.
↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS322A			SN74LS322A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IL} = V_{ILmax},	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.2		2.4	3.1		V
		Q_H'			2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Q_A thru Q_H	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{ILmax}	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Q_H'		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	Q_A thru Q_H	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A thru H	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Data select		V_I = 7 V			0,2			0.2	
		Sign extend		V_I = 7 V			0.3			0.3	
		Any other		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	A thru H, DS	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Sign extend					60			60	
		Any other					20			20	
I_{IL}	Low-level input current	Data select	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Sign extend					−1.2			−1.2	
		Any other					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Q_A thru Q_H	V_{CC} = MAX		−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX			35	60		35	60	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	25	30		MHz
t_{PLH}	Clock	Q_H'	C_L = 15 pF, R_L = 2 kΩ, See Note 2		22	33	ns
t_{PHL}					26	35	
t_{PHL}	Clear	Q_H'			27	35	ns
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 2		16	25	ns
t_{PHL}					22	33	
t_{PHL}	Clear	Q_A thru Q_H			22	35	ns
t_{PZH}	Output enable	Q_A thru Q_H			15	35	ns
t_{PZL}					15	35	
t_{PHZ}	Output enable	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 2		15	25	ns
t_{PLZ}					15	25	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

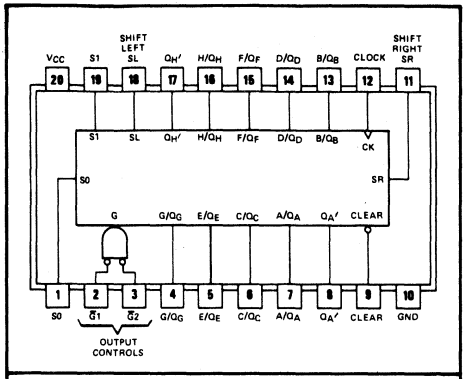
NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11

TYPES SN54LS323, SN74LS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

BULLETIN NO. DL-S 12462, OCTOBER 1976 – REVISED DECEMBER 1980

- **Multiplexed Inputs/Outputs Provide Improved Bit Density**
- **Four Modes of Operation:**
  Hold (Store) **Shift Left**
  Shift Right **Load Data**
- **Operates with Outputs Enabled or at High Z**
- **3-State Outputs Drive Bus Lines Directly**
- **Can Be Cascaded for N-Bit Word Lengths**
- **Typical Power Dissipation . . . 175 mW**
- **Guaranteed Shift (Clock) Frequency . . . 25 MHz**
- **Applications:**
  Stacked or Push-Down Registers,
  Buffer Storage, and
  Accumulator Registers
- **SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear**
- Equivalent to 25LS23

SN54LS323 . . . J PACKAGE
SN74LS323 . . . J OR N PACKAGE
(TOP VIEW)



logic: see description and function table

description

These Low-Power Schottky† eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low level at the clear input clears the register on the next low-to-high transition of the clock.

FUNCTION TABLE

MODE	INPUTS								INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals. See explanation of function tables on page 3-8.

schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

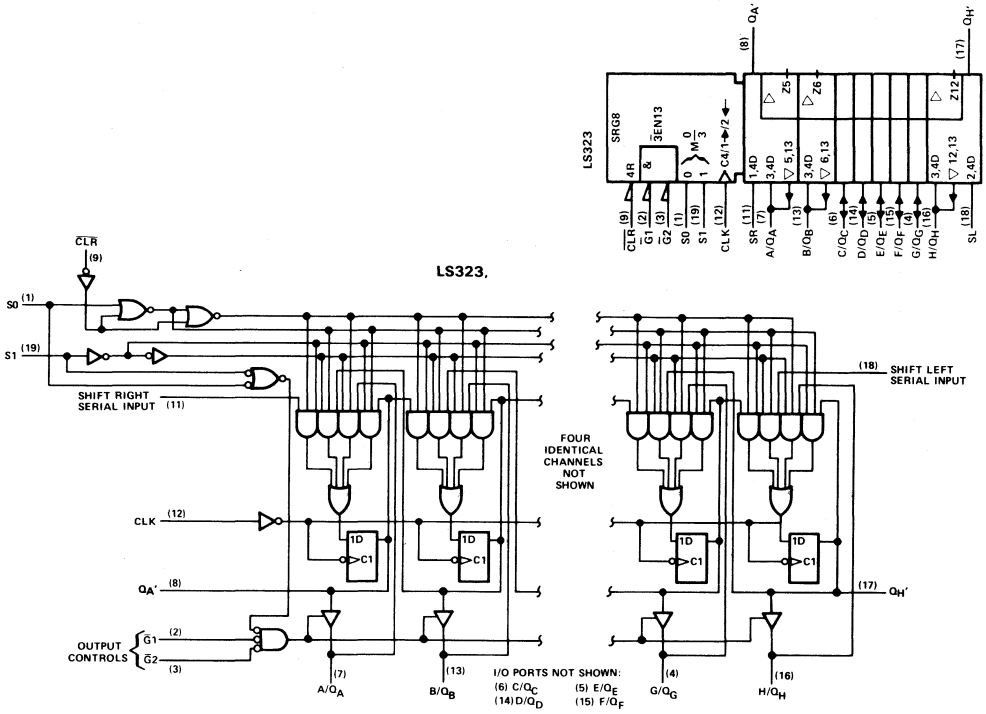
Same as SN54LS299 and SN74LS299, see page 7-462

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

TYPES SN54LS323, SN74LS323
8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

REVISED DECEMBER 1980

functional block diagram



switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 1	25	35		MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$	C_L = 15 pF, R_L = 2 kΩ, See Note 1		22	33	ns
t_{PHL}					26	39	
t_{PLH}	Clock	Q_A thru Q_H	C_L = 45 pF, R_L = 665 Ω, See Note 1		17	25	ns
t_{PHL}					25	39	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H			14	21	ns
t_{PZL}					20	30	
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H	C_L = 5 pF, R_L = 665 Ω, See Note 1		10	15	ns
t_{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

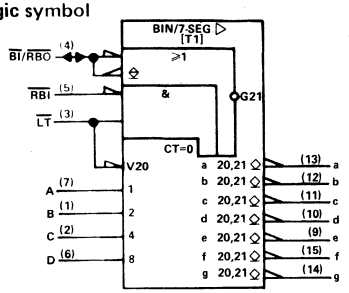
NOTE 1: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times. See load circuits and waveforms on page 3-11.

TYPES SN54LS347, SN74LS347
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

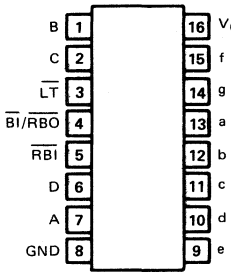
D2426, NOVEMBER 1977

- Low-Voltage Version of SN54LS47/SN74LS47
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

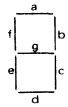
logic symbol



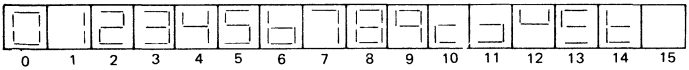
(TOP VIEW)



TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS347	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS347	low	open-collector	24 mA	7 V	35 mW	J, N



SEGMENT IDENTIFICATION



FONT TABLE T1 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp test input, all segment outputs are on.

† BI/RBO is wire AND logic serving as blanking input (BI) and/or ripple blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS347 . . . . . −55°C to 125°C
SN74LS347 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS347			SN74LS347			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS347			SN74LS347			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max,	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max,	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

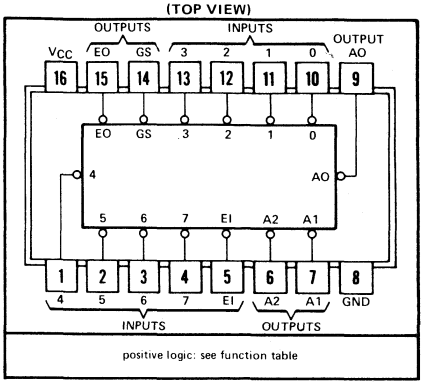
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11
t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

TYPES SN54LS348, SN74LS348 (TIM9908)
8-LINE-TO-3-LINE PRIORITY ENCODERS
WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612469, OCTOBER 1976

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  N-Bit Encoding
  Code Converters and Generators
- Typical Data Delay . . . 15 ns
- Typical Power Dissipation . . . 60 mW

SN54LS348 . . . J OR W PACKAGE
SN74LS348 . . . J OR N PACKAGE
(TOP VIEW)

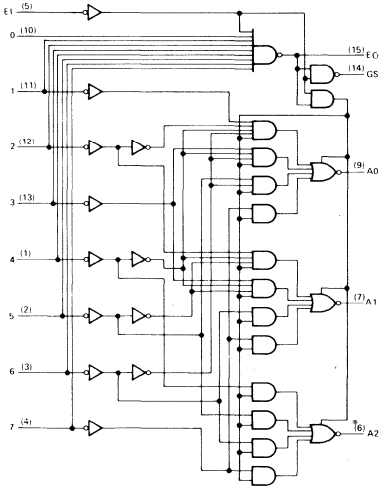


positive logic: see function table

description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

functional block diagram

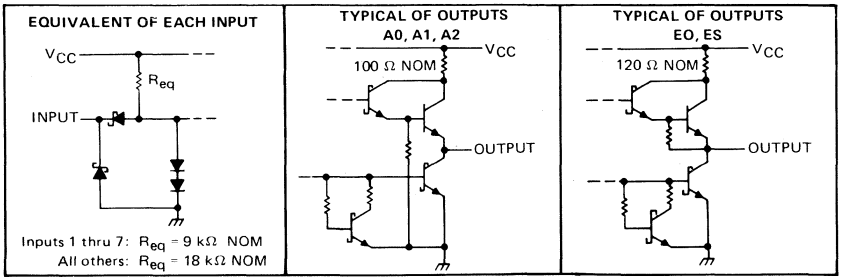


FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant
Z = high-impedance state

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS348 . . . . . −55°C to 125°C
SN74LS348 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS348			SN74LS348			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A0, A1, A2			−1			−2.6	mA
	EO, GS			−400			−400	μA
Low-level output current, I_{OL}	A0, A1, A2			12			24	mA
	EO, GS			4			8	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS348			SN74LS348			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	3.1					V
				I_{OH} = −2.6 mA				2.4	3.1		
		EO, GS		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	A0, A1, A2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		EO, GS		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZ}	Off-State (high-impedance state) output current	A0, A1, A2	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
				V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		All other inputs					0.1			0.1	
I_{IH}	High-level input current	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		All other inputs					20			20	
I_{IL}	Low-level input current	Inputs 1 thru 7	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		All other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§	Outputs A0, A1, A2	V_{CC} = MAX		−30		−130	−30		−130	mA
		Outputs EO, GS			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition 1		13	25		13	25	mA
				Condition 2		12	23		12	23	

NOTE 2: I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1 thru 7	A0, A1, or A2	In-phase output	C_L = 45 pF, R_L = 667 Ω, See Note 3		11	17	ns
t_{PHL}						20	30	
t_{PLH}	1 thru 7	A0, A1, or A2	Out-of-phase output			23	35	ns
t_{PHL}						23	35	
t_{PZH}	EI	A0, A1, or A2				25	39	ns
t_{PZL}						24	41	
t_{PLH}	0 thru 7	EO	Out-of-phase output	C_L = 15 pF R_L = 2 kΩ, See Note 3		11	18	ns
t_{PHL}						26	40	
t_{PLH}	0 thru 7	GS	In-phase output			38	55	ns
t_{PHL}						9	21	
t_{PLH}	EI	GS	In-phase output			11	17	ns
t_{PHL}						14	36	
t_{PLH}	EI	EO	In-phase output			17	26	ns
t_{PHL}						25	40	
t_{PHZ}	EI	A0, A1, or A2		C_L = 5 pF R_L = 667 Ω		18	27	ns
t_{PLZ}						23	35	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level
NOTE 3: Load circuits and waveforms are shown on page 3-11.

7

TYPICAL APPLICATION DATA

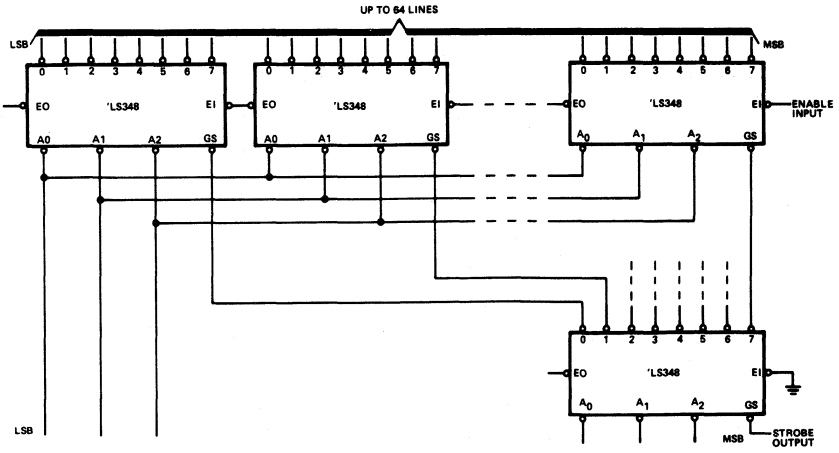


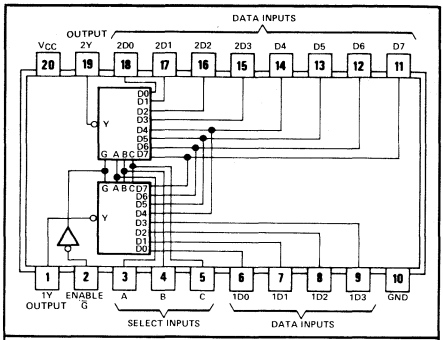
FIGURE 1–PRIORITY ENCODER WITH UP TO 64 INPUTS.

TYPE SN74351
DUAL DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612116, MARCH 1974 – REVISED OCTOBER 1976

- Dual 8-Line-to-1-Line Multiplexer That Can Replace Two SN54151, SN74151 Multiplexers in Some Applications
- Four Common Data Lines Permit Simultaneous Interdigitation with Parallel-to-Serial Conversion
- 4-Bit Organization Is Easily Adapted to Handle Binary or BCD
- Three-State Outputs Can Be Connected Directly to System Bus Lines
- Enable Input Controls Impedance Levels of the 12 Data Inputs and Two Outputs

N
DUAL-IN-LINE PACKAGE (TOP VIEW)

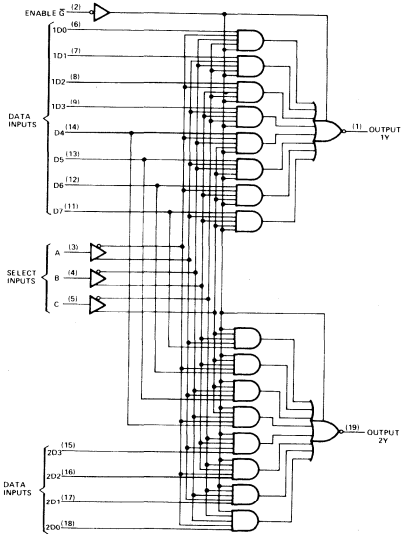


logic: see function table

description

The SN74351 comprises two 8-line-to-1-line data selectors/multiplexers with full decoding on one monolithic chip. Symmetrically switching, complementary decode generators minimize decoder skew during changes at the select inputs and ensure that potentially erroneous effects are minimized at the data outputs. Four data inputs are exclusive to each multiplexer and four are common to both. A common enable input is provided which, when high, causes both outputs to assume the high-impedance (off) state and simultaneously diverts the majority of the input current, which reduces the load significantly on the data input drivers. A low logic level at the enable input activates both outputs so that each will assume the complement of the level of the selected input.

functional block diagram

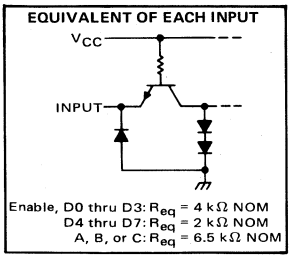


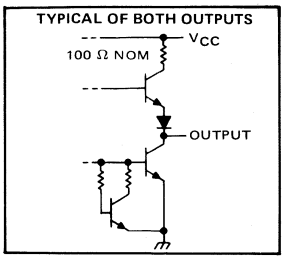
FUNCTION TABLE

INPUTS				OUTPUTS	
ENABLE	SELECT				
$\overline{G}$	C	B	A	1Y	2Y
H	X	X	X	Z	Z
L	L	L	L	$\overline{1D0}$	$\overline{2D0}$
L	L	L	H	$\overline{1D1}$	$\overline{2D1}$
L	L	H	L	$\overline{1D2}$	$\overline{2D2}$
L	L	H	H	$\overline{1D3}$	$\overline{2D3}$
L	H	L	L	$\overline{D4}$	$\overline{D4}$
L	H	L	H	$\overline{D5}$	$\overline{D5}$
L	H	H	L	$\overline{D6}$	$\overline{D6}$
L	H	H	H	$\overline{D7}$	$\overline{D7}$

H = high level, L = low level, X = irrelevant
Z = high impedance (off)
$\overline{1D0}$, $\overline{1D1}$, . . . $\overline{D7}$ = The complement of the level of the respective D input

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−0.8	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.8 mA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			40	μA
I_{OZL}	Off state output current, low level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V			−40	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Enable, any select, any D0 thru D3	V_{CC} = MAX, V_I = 2.4 V			40	μA
		D4 thru D7				80	
I_{IL}	Low-level input current	Enable, any select, any D0 thru D3	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		D4 thru D7				−3.2	
		Any D	V_{CC} = MAX, V_I = 0.5, $V_{I(enable)}$ = 2 V			−40	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		44	66	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the enable input grounded, other inputs and both outputs open.

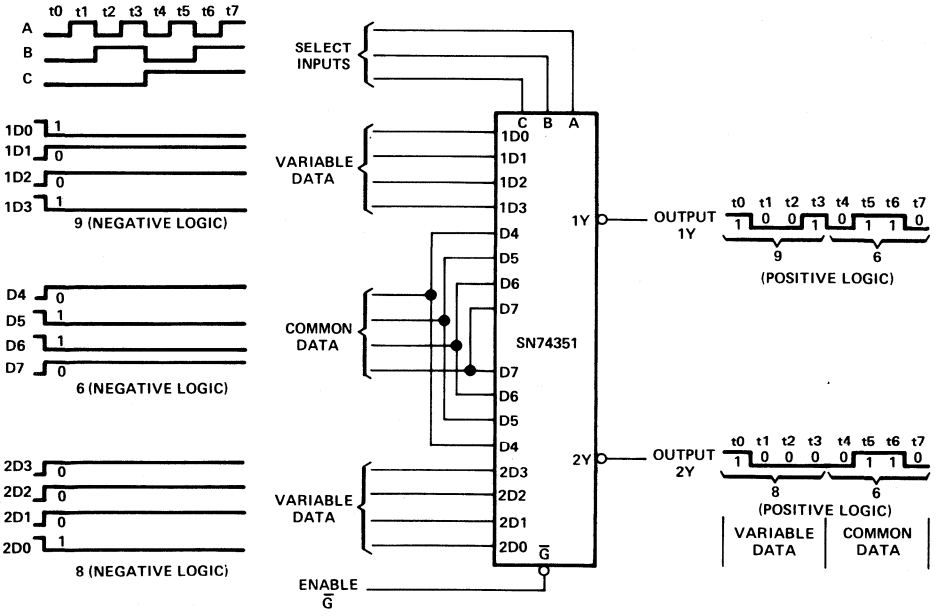
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C	Y	C_L = 50 pF, R_L = 400 Ω, See Note 3		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Any D	Y			10	22	ns
t_{PHL}					10	22	
t_{ZH}	$\overline{G}$	Y			18	33	ns
t_{ZL}					20	33	
t_{HZ}	$\overline{G}$	Y	C_L = 5 pF, R_L = 400 Ω, See Note 3		6	20	ns
t_{LZ}					10	20	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPICAL APPLICATION DATA

This application illustrates how common data can be interdigitated onto two serial data lines. It is useful for transmitting prefixes, suffixes, addresses, or similar functions.

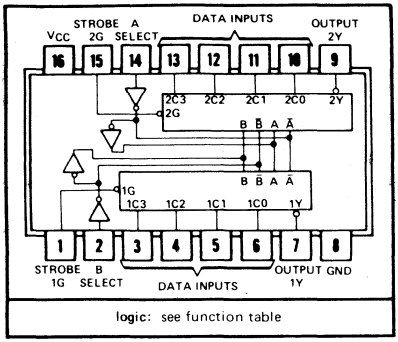


TYPES SN54LS352, SN74LS352
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7612463, OCTOBER 1976

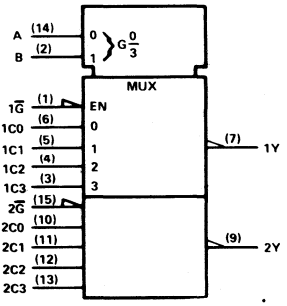
- Inverting Versions of SN54LS153, SN74LS153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
  Data Input to Output . . . 15 ns
  Strobe Input to Output . . . 19 ns
  Select Input to Output . . . 22 ns
- Fully Compatible with most TTL and DTL Circuits
- Low Power Dissipation . . . 31 mW Typical (Enabled)
- Inverted Data

SN54LS352 . . . J OR W PACKAGE
SN74LS352 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

logic symbol



description

Each of these Schottky-clamped data selectors/-multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

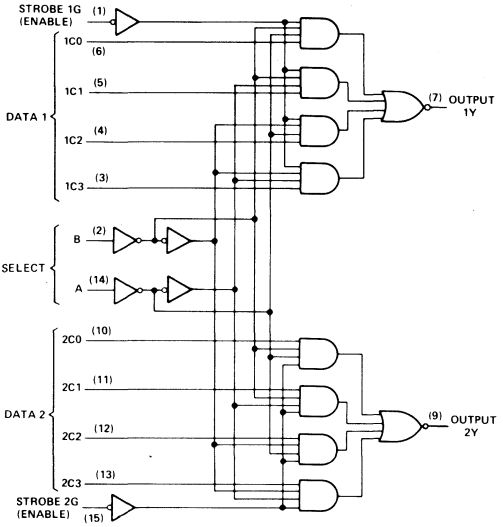
Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

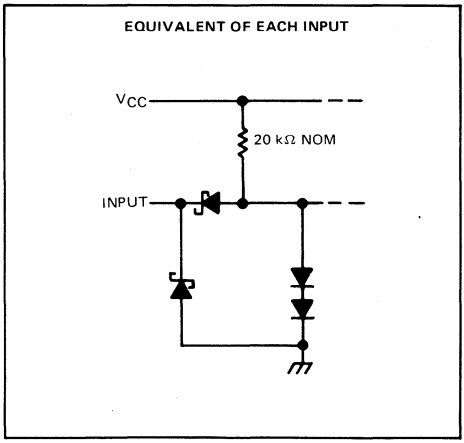
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS352 . . . . . −55°C to 125°C
SN74LS352 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

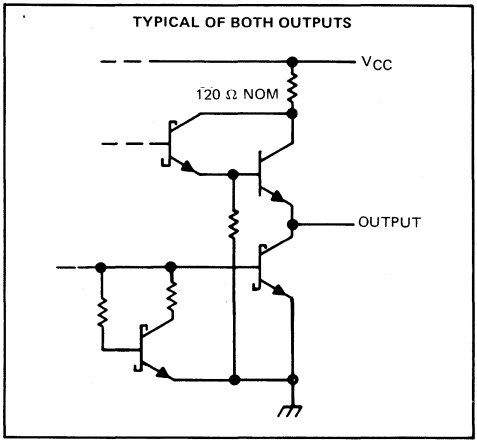
NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagram



schematics of inputs and outputs





recommended operating conditions

	SN54LS352			SN74LS352			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54LS352			SN74LS352			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		G input			−0.2			−0.2	
I_{OS} Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CCL} Supply current, output low	V_{CC} = MAX, See Note 2			6.2	10		6.2	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time,and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 3		13	20	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

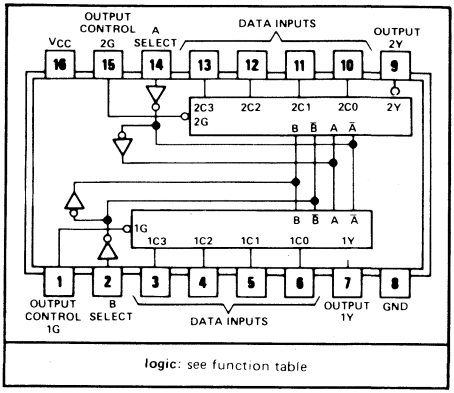
NOTE 3: Load circuits and voltage waveforms are shown on page 3-11.

TYPES SN54LS353, SN74LS353
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS
3-STATE OUTPUTS

BULLETIN NO. DL-S 7612464, OCTOBER 1976

- Inverting Versions of SN54LS253, SN74LS253
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
  Data Input to Output . . . 12 ns
  Control Input to Output . . . 16 ns
  Select Input to Output . . . 21 ns
- Fully Compatible with Most TTL and DTL Circuits
- Low Power Dissipation . . . 35 mW Typical (Enabled)
- Inverted Data

SN54LS353 . . . J OR W PACKAGE
SN74LS353 . . . J OR N PACKAGE
(TOP VIEW)



description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

logic

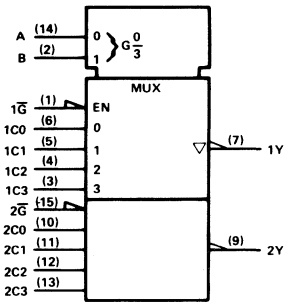
FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

logic symbol

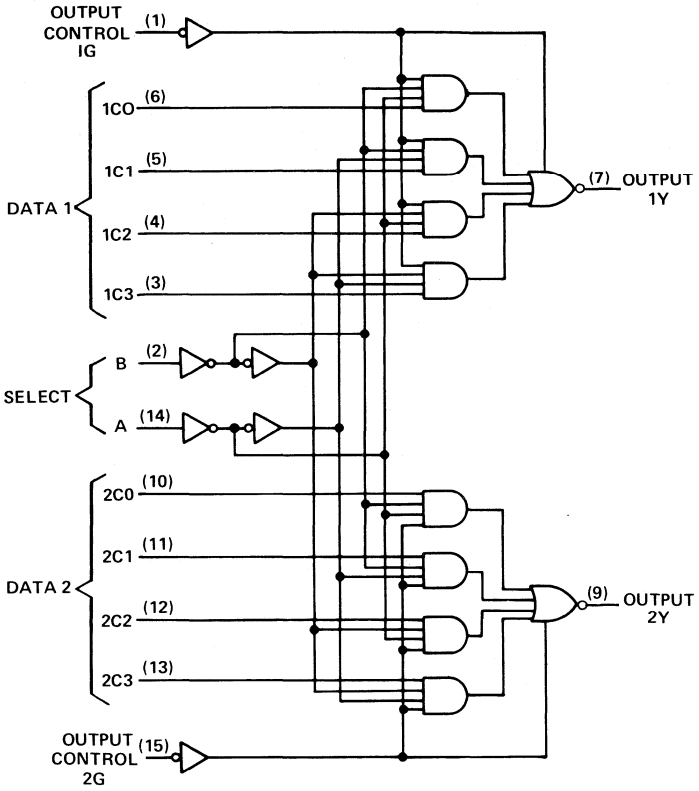


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

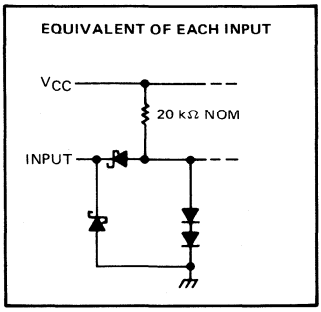
Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS353 . . . . . −55°C to 125°C
SN74LS353 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

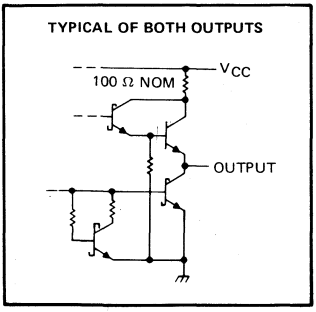
NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagram



schematics of inputs and outputs





TYPES SN54LS353, SN74LS353
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS
WITH 3-STATE OUTPUTS

REVISED OCTOBER 1983

recommended operating conditions

	SN54LS353			SN74LS353			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS353			SN74LS353			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_{OZ}	Off-State (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
			G input			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Condition A		7	12		7	12	mA
			Condition B		8.5	14		8.5	14	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with the outputs open under the following conditions:

A. All inputs grounded.

B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 3		11	25	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			20	45	ns
t_{PHL}					21	32	
t_{PZH}	Output Control	Y			11	23	ns
t_{PZL}					15	23	
t_{PHZ}	Output Control	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 3		27	41	ns
t_{PLZ}					12	27	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

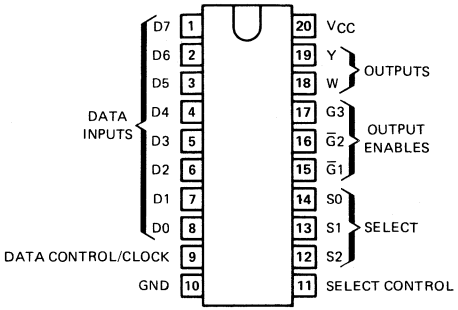
NOTE 3: Load circuit and waveforms are shown on page 3-11.

TYPES SN54LS354, SN54LS355, SN54LS356, SN54LS357, SN74LS354, SN74LS355, SN74LS356, SN74LS357
8-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS/REGISTERS

D2544, JULY 1979

- Transparent Latches on Data Select Inputs
- Choice of Data Registers:
  Transparent ('LS354, 'LS355)
  Edge-Triggered ('LS356, 'LS357)
- Choice of Outputs:
  Three-State ('LS354, 'LS356)
  Open-Collector ('LS355, 'LS357)
- Complementary Outputs
- Easily Expandable
- High-Density 20-Pin Package

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data-select address is stored in transparent latches that are enabled by a low level on pin 11, $\overline{SC}$. On the 'LS354 and 'LS355 a similar enable for data is obtained by a low level on pin 9, $\overline{DC}$. The edge-triggered data registers of the 'LS356 and 'LS357 are clocked by a low-to-high transition on pin 9, CLK. Complementary outputs are available in either three-state versions ('LS354 and 'LS356) or open-collector versions ('LS355 and 'LS357).

The SN54LS354 through SN54LS357 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS354 through SN74LS357 are characterized for operation from 0°C to 70°C.

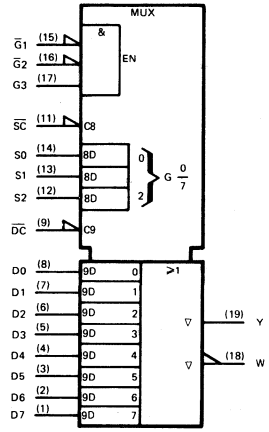
FUNCTION TABLE

INPUTS								OUTPUTS	
SELECT†			DATA CONTROL ('LS354, 'LS355)	CLOCK ('LS356, 'LS357)	OUTPUT ENABLES				
S2	S1	S0			$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

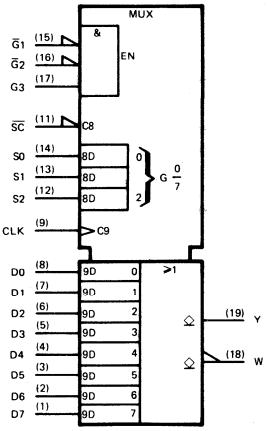
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level
D0 . . . D7 = the level of steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'LS356 and 'LS357
$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock
† This column shows the input address setup with $\overline{SC}$ low.

logic symbols†

'LS354
('LS355 is open-collector version)

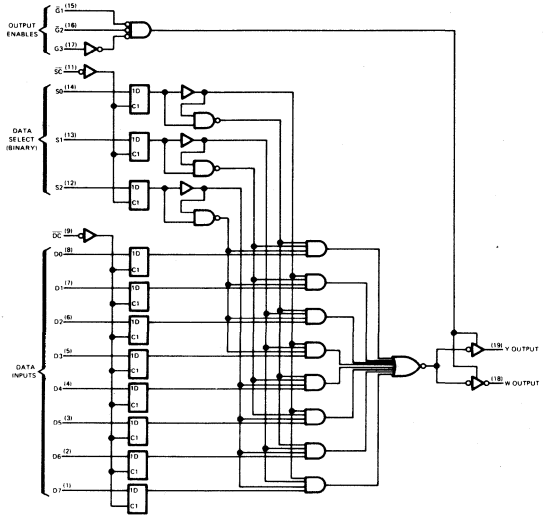


'LS357
('LS356 is 3-state version)

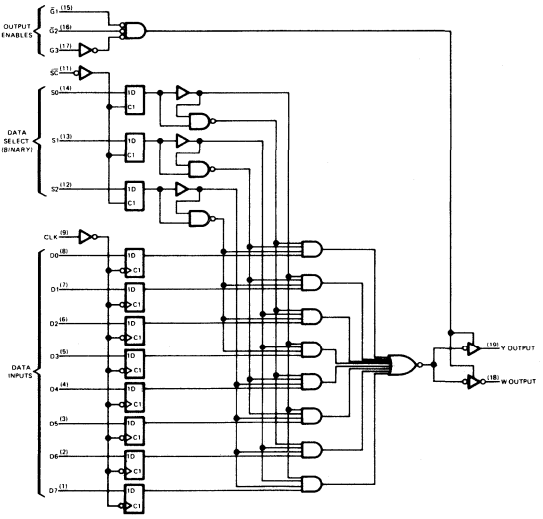


functional block diagrams (positive logic)

'LS354, 'LS355



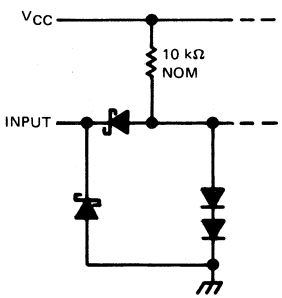
'LS356, 'LS357



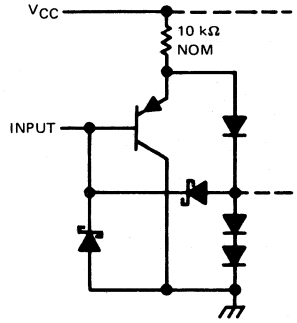
†These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

schematics of inputs and outputs

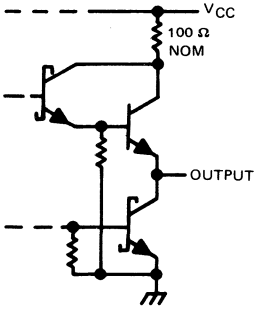
EQUIVALENT OF EACH DATA OR SELECT INPUT



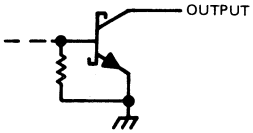
EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF BOTH OUTPUTS ON 'LS354 AND 'LS356



TYPICAL OF BOTH OUTPUTS ON 'LS355 AND 'LS357



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		7 V
Operating free-air temperature range:	SN54LS'	−55°C to 125°C
	SN74LS'	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS354, SN54LS356			SN74LS354, SN74LS356			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Setup times, high- or low-level data, t_{su} (with respect to ↑ at pin 9)	'LS354	15			15			ns
	'LS356	15			15			
Hold times, high- or low-level data, t_h (with respect to ↑ at pin 9)	'LS354	15			15			ns
	'LS356	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS354, SN54LS356			SN74LS354, SN74LS356			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = V_{IL} max,	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX		V_O = 2.7 V			20			20	μA
					V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	$\overline{DC}$ or CLK, $\overline{G}1$, $\overline{G}2$, G3	V_{CC} = MAX,	V_I = 0.4 V				−0.2			−0.2	mA
		All others						−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2			29	46		29	46	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS354			'LS356			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D0-D7	Y	C_L = 45 pF, See Note 3		24	36				ns
t_{PHL}					23	35				
t_{PLH}		W			18	27				ns
t_{PHL}					29	44				
t_{PLH}	$\overline{DC}$ or CLK	Y			28	42		18	27	ns
t_{PHL}					26	39		33	50	
t_{PLH}		W			22	33		24	36	ns
t_{PHL}					33	50		18	27	
t_{PLH}	S0, S1, S2	Y			29	44		30	45	ns
t_{PHL}					24	45		28	48	
t_{PLH}		W			28	42		36	54	ns
t_{PHL}					34	51		30	45	
t_{PLH}	$\overline{SC}$	Y			34	51		36	54	ns
t_{PHL}					31	47		40	60	
t_{PLH}		W			27	41		32	48	ns
t_{PHL}					40	60		36	54	
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Y			14	27		14	25	ns
t_{PZL}					18	27		17	25	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	24	ns
t_{PLZ}					15	23		16	24	
t_{PZH}		W	C_L = 45 pF, See Note 3		12	24		14	23	ns
t_{PZL}					16	24		16	23	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	23	ns
t_{PLZ}					15	23		16	23	
t_{PZH}	G3	Y	C_L = 45 pF, See Note 3		15	29		15	27	ns
t_{PZL}					19	29		18	27	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	25	ns
t_{PLZ}					15	23		16	25	
t_{PZH}		W	C_L = 45 pF, See Note 3		13	25		14	25	ns
t_{PZL}					17	25		16	25	
t_{PHZ}			C_L = 5 pF, See Note 3		15	23		16	25	ns
t_{PLZ}					15	23		16	25	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 3: Load circuit and waveforms are shown on page 3-11

7

recommended operating conditions

		SN54LS355 SN54LS357			SN74LS355 SN74LS357			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Setup times, high- or low-level data, t_{su} (with respect to ↑ at pin 9)	'LS355	15			15			ns
	'LS357	15			15			
Hold times, high- or low-level data, t_h (with respect to ↑ at pin 9)	'LS355	15			15			ns
	'LS357	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS355 SN54LS357			SN74LS355 SN74LS357			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	$\overline{DC}$ or CLK, $\overline{G1}$, $\overline{G2}$, G3	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
		All others					−0.4			−0.4	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		29	46		29	46	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS355			'LS357			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	D0-D7	Y	C_L = 45 pF, See Note 3		34	41				ns
t_{PHL}					26	39				
t_{PLH}		W			30	45				ns
t_{PHL}					33	50				
t_{PLH}	$\overline{DC}$ or CLK	Y			38	57		27	41	ns
t_{PHL}					31	47		34	51	
t_{PLH}		W			33	50		32	48	ns
t_{PHL}					39	59		23	35	
t_{PLH}	S0, S1, S2	Y			39	59		38	57	ns
t_{PHL}					36	49		40	60	
t_{PLH}		W			32	48		38	57	ns
t_{PHL}					39	58		35	53	
t_{PLH}	$\overline{SC}$	Y			45	68		44	66	ns
t_{PHL}					42	63		41	62	
t_{PLH}		W			44	66		41	62	ns
t_{PHL}					45	68		41	62	
t_{PLH}	$\overline{G1}$, $\overline{G2}$	Y			21	32		18	27	ns
t_{PHL}					22	33		18	27	
t_{PLH}		W			18	27		20	30	ns
t_{PHL}					19	29		21	32	
t_{PZH}	G3	Y			24	36		24	36	ns
t_{PHL}					25	40		24	36	
t_{PLH}		W			19	29		19	31	ns
t_{PHL}					19	31		19	31	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

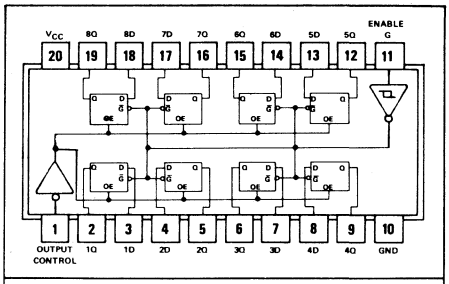
NOTE 3: Load circuit and waveforms are shown on page 3-11

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374 OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7612350, OCTOBER 1976

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

SN54LS373, SN54S373 . . . J PACKAGE
SN74LS373, SN74S373 . . . J OR N PACKAGE
(TOP VIEW)

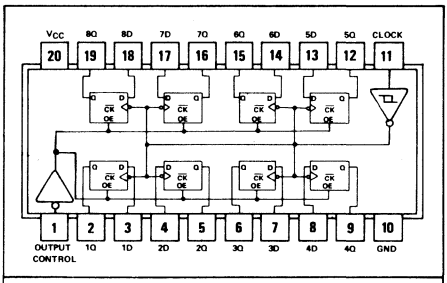


logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS374, SN54S374 . . . J PACKAGE
SN74LS374, SN74S374 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

See explanation of function tables on page 3-8.

description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

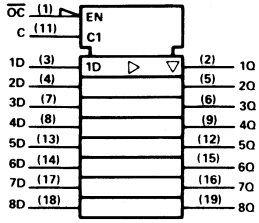
description (continued)

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

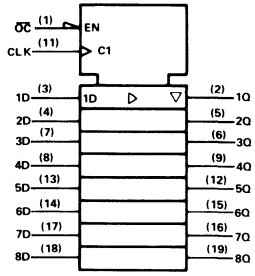
Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

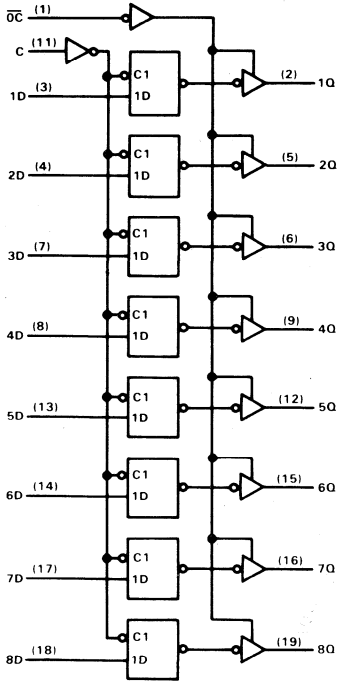
logic symbol



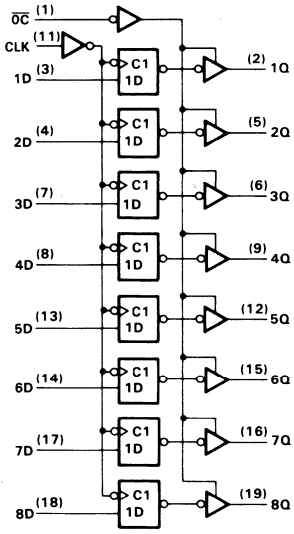
logic symbol



logic diagram (positive logic)



logic diagram (positive logic)



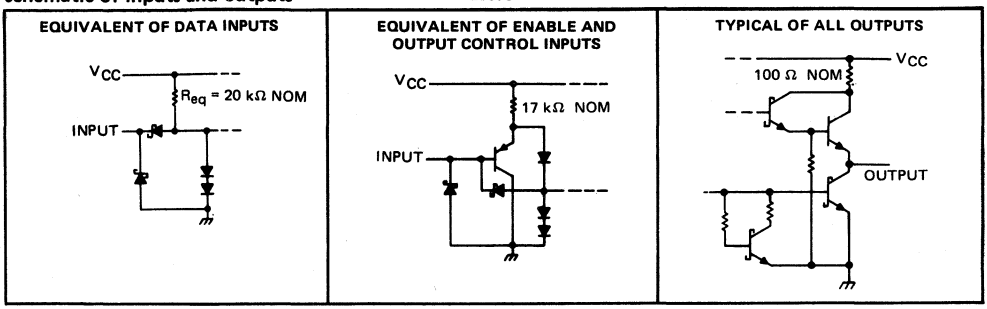
7

TYPES SN54LS373, SN54LS374, SN74LS373, SN74LS374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

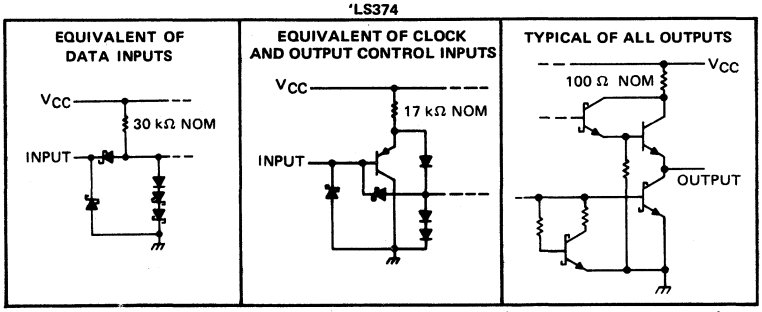
REVISED DECEMBER 1980

schematic of inputs and outputs

'LS373



'LS374



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−1			−2.6	mA
Width of clock/enable pulse, t_w	High	15			15			ns
	Low	15			15			
Data setup time, t_{su}	'LS373	5↓			5↓			ns
	'LS374	20↑			20↑			
Data hold time, t_h	'LS373	20↓			20↓			ns
	'LS374	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

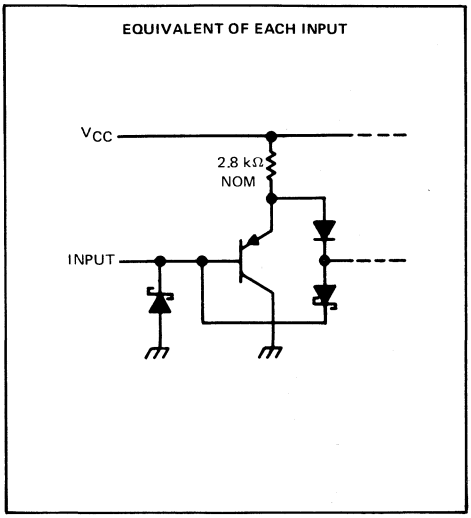
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3				35	50		MHz
t_{PLH}	Data	Any Q			12	18				ns
t_{PHL}					12	18				
t_{PLH}	Clock or enable	Any Q			20	30		15	28	ns
t_{PHL}					18	30		19	28	
t_{PZH}	Output Control	Any Q			15	28		20	28	ns
t_{PZL}					25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3		12	20		12	20	ns
t_{PLZ}					15	25		14	25	

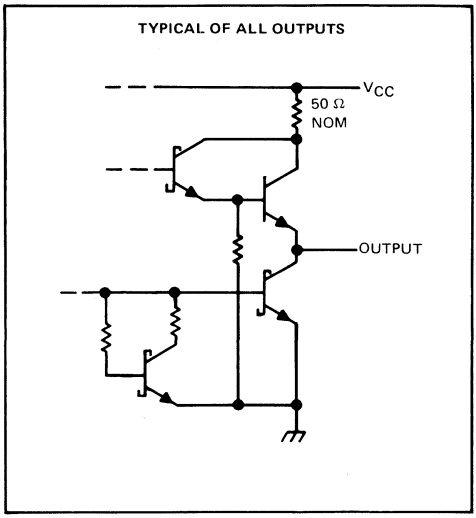
NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See load circuits and waveforms on page 3-11.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE: For pulse width less than 20 nsec, a minimum 5 nsec t_h is required. For pulse width greater than 20 nsec, a MIN 0 ns t_h is acceptable. All f_{max} applications are dependand upon the above conditions.

schematic of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' . . . . . −55°C to 125°C
SN74S' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.4		V
		SN74S'	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN,	V_{IH} = 2 V,			0.5	V
			V_{IL} = 0.8 V,	I_{OL} = 20 mA				
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_{IH} = 2 V,			50	μA
			V_O = 2.4 V					
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_{IH} = 2 V,			−50	μA
			V_O = 0.5 V					
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			50	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	'S373		105	160	mA
				'S374 all inputs grounded		90	140	
				C_K = O_C = 4 V, all D inputs grounded			180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

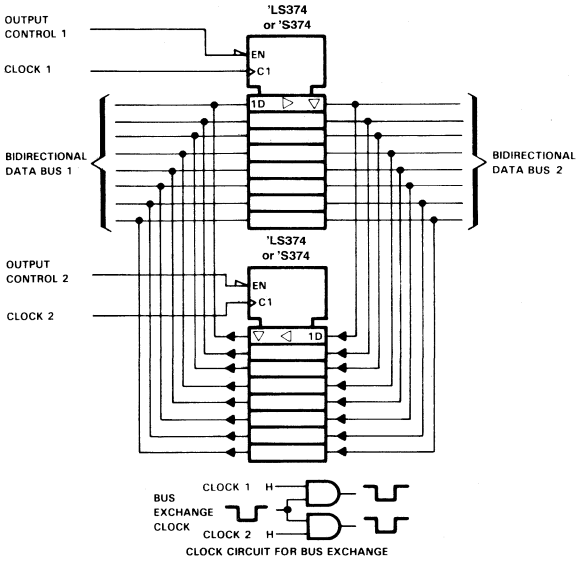
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Notes 2 and 4				75	100		MHz
t_{PLH}	Data	Any Q			7	12				ns
t_{PHL}					7	12				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	Output Control	Any Q			8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note 3		6	9		5	9	ns
t_{PLZ}					8	12		7	12	

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
4. See load circuits and waveforms on page 3-10.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

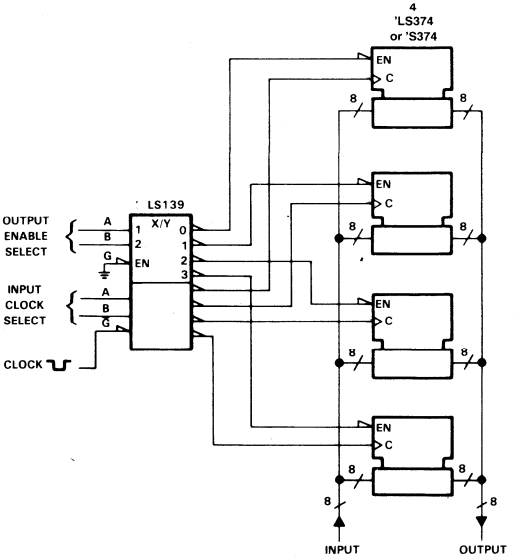
TYPICAL APPLICATION DATA

BIDIRECTIONAL BUS DRIVER



CLOCK CIRCUIT FOR BUS EXCHANGE

EXPANDABLE 4-WORD BY 8-BIT GENERAL REGISTER FILE



TYPES SN54LS375, SN74LS375
4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7612131, OCTOBER 1976

- Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

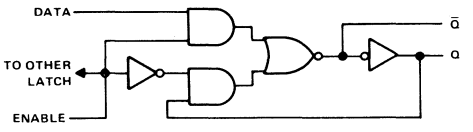
logic

FUNCTION TABLE
(EACH LATCH)

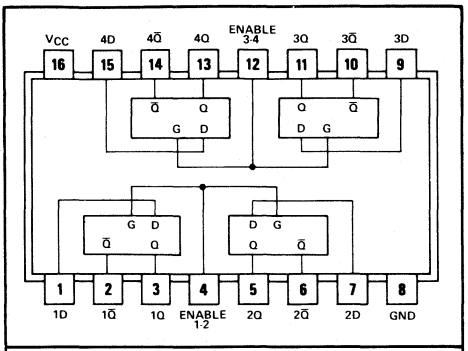
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G.

functional block diagram (each latch)



SN54LS375 . . . J OR W PACKAGE
SN74LS375 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

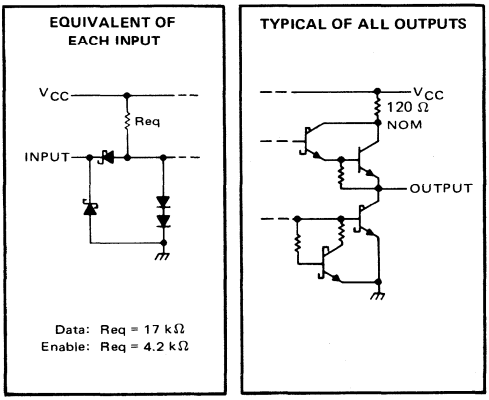
description

The SN54LS375 and SN74LS375 bistable latches are electrically and functionally identical to the SN54LS75 and SN74LS75, respectively. Only the arrangement of the terminals has been changed in the SN54LS375 and SN74LS375.

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The SN54LS375 is characterized for operation over the full military temperature range of −55°C to 125°C; SN74LS375 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS375 . . . . . −55°C to 125°C
SN74LS375 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions, electrical characteristics, and switching characteristics

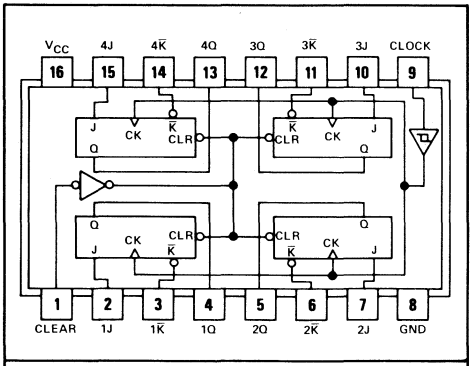
Same as SN54LS75 and SN74LS75, see page 7-33.

TYPES SN54376, SN74376
QUADRUPLE J-$\overline{K}$ FLIP-FLOPS

BULLETIN NO. DL-S 7612461, OCTOBER 1976

- Four J-$\overline{K}$ Flip-Flops in a Single Package . . . Can Reduce FF Package Count by 50%
- Common Positive-Edge-Triggered Clocks with Hysteresis . . . Typically 200 mV
- Fully Buffered Outputs
- Typical Clock Input Frequency . . . 45 MHz

SN54376 . . . J OR W PACKAGE
SN74376 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These quadruple TTL J-$\overline{K}$ flip-flops incorporate a number of third-generation IC features that can simplify system design and reduce flip-flop package count by as much as 50%. They feature hysteresis at the clock input, fully buffered outputs, and direct clear capability. The positive-edge-triggered SN54376 and SN74376 are directly compatible with most Series 54/74 MSI registers.

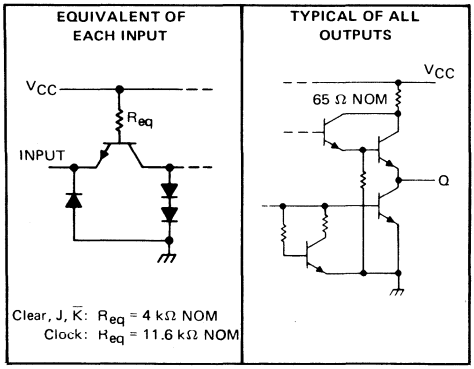
The SN54376 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74376 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH FLIP-FLOP)

COMMON INPUTS		INPUTS		OUTPUT
CLEAR	CLOCK	J	$\overline{K}$	Q
L	X	X	X	L
H	↑	L	H	Q_0
H	↑	H	H	H
H	↑	L	L	L
H	↑	H	L	TOGGLE
H	L	X	X	Q_0

See explanation of function tables on page 3-8.

schematics of inputs and outputs



Resistor values shown are nominal and in ohms

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54376 . . . . . −55°C to 125°C
SN74376 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54376			SN74376			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency		0		30	0		30	MHz
Pulse width, t_w	Clock high	22			22			ns
	Clock low	12			12			
	Preset or clear low	12			12			
Setup time, t_{su}	J, $\overline{K}$ inputs	0↑			0↑			ns
	Clear inactive state	10↑			10↑			
Input hold time, t_h		20↑			20↑			ns
Operating free-air temperature, T_A		55		125	0		70	°C

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−85	mA
I_{CC}	Supply current	V_{CC} = MAX			52	74	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 2	30	45		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			17	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			24	35	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

BULLETIN NO. DL-S 7612474, OCTOBER 1976

- 'LS377 and 'LS378 Contain Eight and Six Flip-Flops, Respectively, with Single-Rail Outputs
- 'LS379 Contains Four Flip-Flops with Double-Rail Outputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- 'LS378 is equivalent to 25LS07
- 'LS379 is equivalent to 25LS08

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The 'LS377, 'LS378, and 'LS379 devices are similar to 'LS273, 'LS174, and 'LS175, respectively, but feature a common enable instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the $\overline{G}$ input.

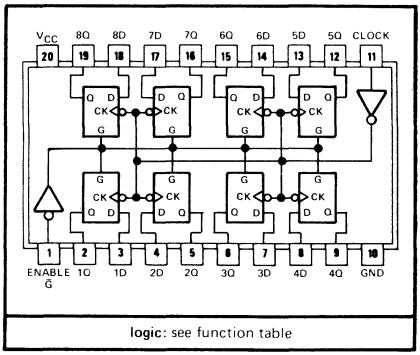
These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 MHz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 10 milliwatts per flip-flop.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{G}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

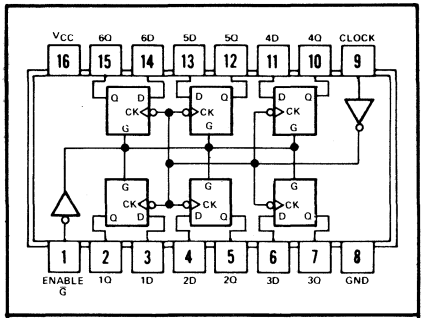
See explanation of function tables on page 3-8.

SN54LS377 . . . J PACKAGE
SN74LS377 . . . J OR N PACKAGE
(TOP VIEW)



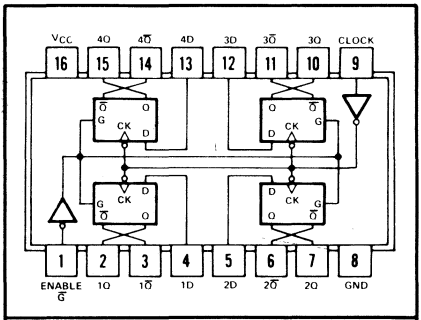
logic: see function table

SN54LS378 . . . J OR W PACKAGE
SN74LS378 . . . J OR N PACKAGE
(TOP VIEW)



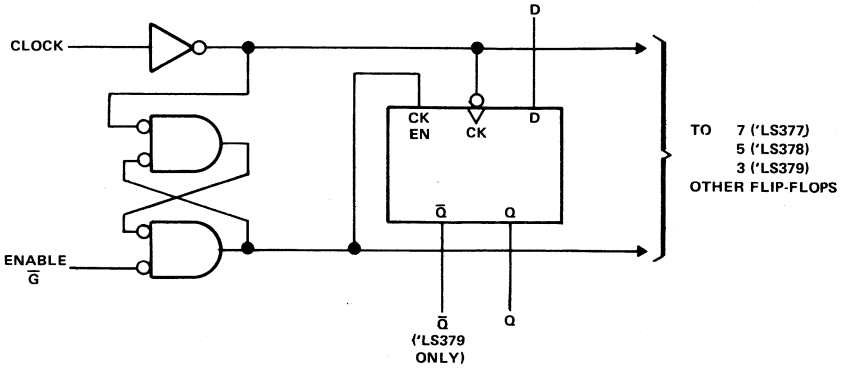
logic: see function table

SN54LS379 . . . J OR W PACKAGE
SN74LS379 . . . J OR N PACKAGE
(TOP VIEW)

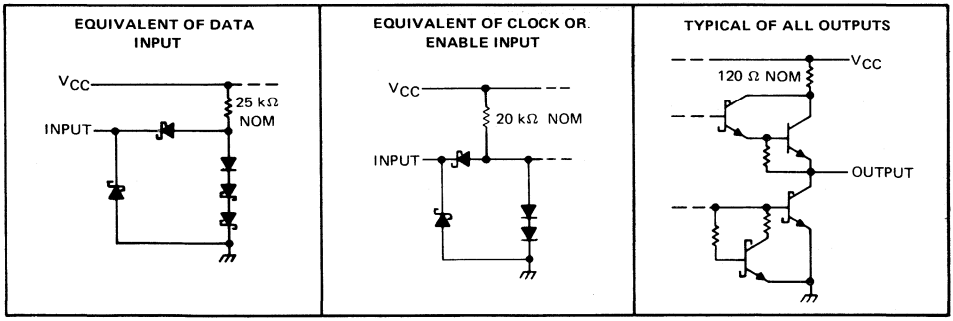


logic: see function table

functional block diagram



schematics of inputs and outputs



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OH}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20↑			20↑			ns
	Enable active-state	25↑			25↑			
	Enable inactive-state	10↑			10↑			
Hold time, t_h	Data and enable	5↑			5↑			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,		2.5	3.5		2.7	3.5		V
		V_{IL} = V_{IL} max,	I_{OH} = −400 μA								
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{IL} = V_{IL} max		I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	'LS377		17	28		17	28	mA
				'LS378		13	22		13	22	mA
				'LS379		9	15		9	15	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Note more than one input should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and ground applied to all data and enable inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF,	30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock	R_L = 2 kΩ		17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock	See Note 3		18	27	ns

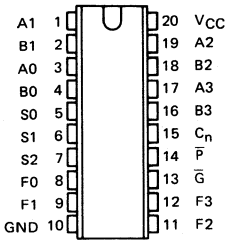
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS381A, SN54LS382, SN74LS381A, SN74LS382
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

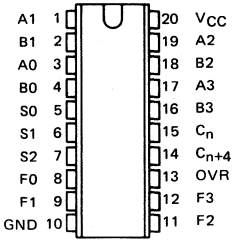
PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$ ('LS381 ONLY)	14	ACTIVE-LOW CARRY PROPAGATE OUTPUT
$\overline{G}$ ('LS381 ONLY)	13	ACTIVE-LOW CARRY GENERATE OUTPUT
C_{n+4} ('LS382 ONLY)	14	RIPPLE-CARRY OUTPUT
OVR ('LS382 ONLY)	13	OVERFLOW OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

SN54LS381A . . . J PACKAGE
SN74LS381A . . . J OR N PACKAGE
(TOP VIEW)



SN54LS382 . . J PACKAGE
SN74LS382 . . J OR N PACKAGE
(TOP VIEW)



FUNCTION TABLE

SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

- **Fully Parallel 4-Bit ALU's in 20-Pin Package for 0.300-Inch Row Spacing**
- **Ideally Suited for High-Density Economical Processors**
- **'381A Features $\overline{G}$ and $\overline{P}$ Outputs for Look-Ahead Carry Cascading**
- **'LS382 Features Ripple Carry ($C_n + 4$) and Overflow (OVR) Outputs**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  - **A Minus B**
  - **B Minus A**
  - **A Plus B**
  - **and Five Other Functions**
- **'LS382 is equivalent to 25LS2517**

description

The 'LS381A and 'LS382 are low-power Schottky TTL arithmetic logic units (ALUs)/function generators that perform eight binary arithmetic/logic operations on two-4-bit words as shown in the function table. The exclusive-OR, AND, or OR function of the two Boolean variables is provided without the use of external circuitry. Also, the outputs can be cleared (low) or preset (high) as desired. The 'LS381A provides two cascade outputs ($\overline{P}$ and $\overline{G}$) for expansion utilizing SN54S182/SN74S182 look-ahead carry generators. The 'LS382 provides a $C_n + 4$ output to ripple the carry to the C_n input of the next stage. The 'LS382 detects and indicates two's complement overflow condition via the OVR output. The overflow output is logically equivalent to $C_{n+3} + C_{n+4}$. When the 'LS382 is cascaded to handle word lengths longer than four bits in length, only the most significant overflow (OVR) output is used.

The SN54LS381A and SN54LS382 will be characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS381A and SN74LS382 will be characterized for operation from 0°C to 70°C.

function table

Certain differences exist in the $\overline{G}$, $\overline{P}$ ('LS381A) and OVR, C_{n+4} ('LS382) function table compared with similar parts from other vendors. No differences exist in the arithmetic modes (B minus A, A minus B, and A plus B), where these outputs perform valuable cascade functions.

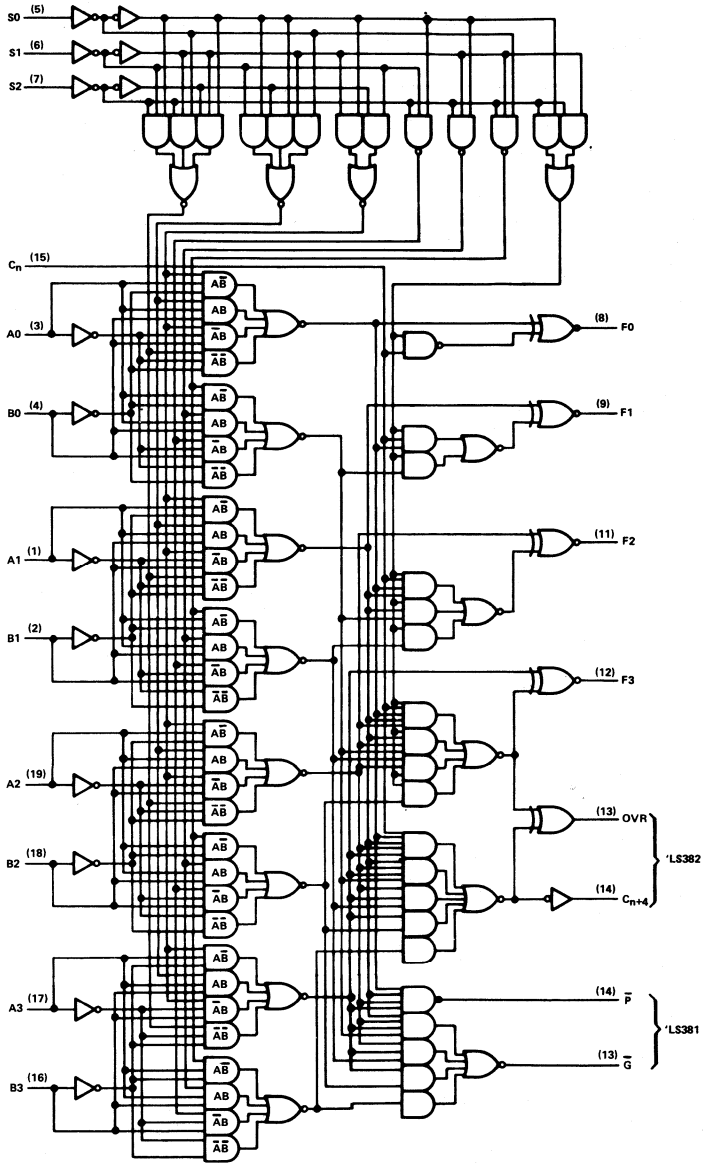
There are slight differences in the other modes (CLEAR, A + B, A + B, AB, and PRESET), where these outputs are strictly "don't care".

This function table is a condensed version and assumes for A_n that A0, A1, A2, and A3 inputs all agree and for B_n that B0, B1, B2, and B3 inputs all agree. This table is intended to point out the response of these $\overline{G}$, $\overline{P}$ ('LS381A) and OVR, C_{n+4} ('LS382) outputs in all modes of operation to facilitate incoming inspection.

FUNCTION TABLE

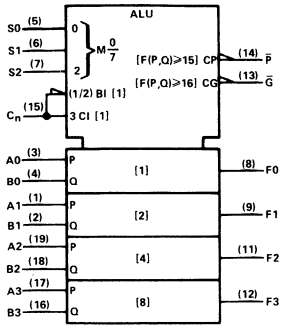
ARITHMETIC/LOGIC OPERATION	INPUTS						OUTPUTS				('LS381A)		('LS382)	
	S2	S1	S0	C_n	A_n	B_n	F3	F2	F1	F0	$\overline{G}$	$\overline{P}$	OVR	C_{n+4}
CLEAR	L	L	L	X	X	X	L	L	L	L	H	H	L	L
B MINUS A	L	L	H	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	H	H	H	L	L	H	L	H
				L	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	H	H	H	H	L	H	L	H
				H	H	L	L	L	L	H	H	H	L	L
				H	H	H	L	L	L	L	H	L	L	H
A MINUS B	L	H	L	L	L	L	H	H	H	H	H	L	L	L
				L	L	H	L	L	L	L	H	H	L	L
				L	H	L	H	H	H	H	L	H	L	H
				L	H	H	H	H	H	H	H	L	L	L
				H	L	L	L	L	L	L	H	L	L	H
				H	L	H	L	L	L	H	H	H	L	L
				H	H	L	H	H	H	H	L	H	L	H
				H	H	H	L	L	L	L	H	L	L	H
A PLUS B	L	H	H	L	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				L	H	L	H	H	H	H	H	L	L	L
				L	H	H	H	H	H	L	L	H	L	H
				H	L	L	L	L	L	H	H	H	L	L
				H	L	H	L	L	L	L	H	L	L	H
				H	H	L	L	L	L	L	H	L	L	H
				H	H	H	H	H	H	H	L	H	L	H
A ⊕ B	H	L	L	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				X	H	H	L	L	L	L	H	H	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H	L	L
				L	L	H	H	H	H	H	H	L	L	L
				H	L	H	H	H	H	H	H	L	H	H
				L	H	L	H	H	H	H	H	L	L	L
				H	H	L	H	H	H	H	H	L	H	H
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
AB	H	H	L	X	L	L	L	L	L	L	H	H	L	L
				X	L	H	L	L	L	L	H	H	L	L
				X	H	L	L	L	L	L	H	H	L	L
				L	H	H	H	H	H	H	H	L	L	L
				H	H	H	H	H	H	H	H	L	H	H
PRESET	H	H	H	L	X	X	H	H	H	H	H	L	L	L
				H	X	X	H	H	H	H	H	L	H	H

functional block diagram (positive logic)

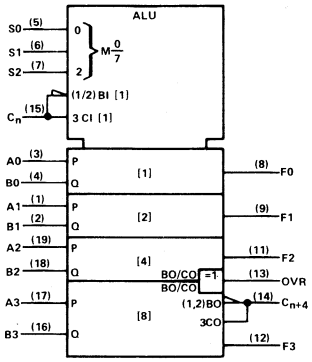


logic symbols

'LS381A

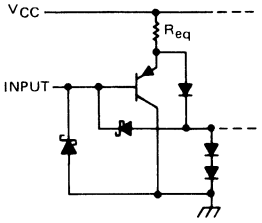


'LS382



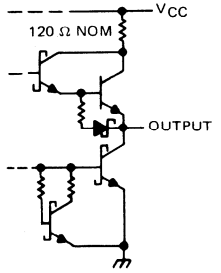
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Any S: R_{eq} = 10 kΩ
C_n ('LS381A): R_{eq} = 2.5 kΩ
All others: R_{eq} = 2 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS381A, SN54LS382 . . . . . −55°C to 125°C
SN74LS381A, SN74LS382 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}	$\overline{G}$ output of 'LS381A			16			16	mA
	All other outputs			4			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	$\overline{G}$ ('LS381A)	V_{CC} = MIN,	I_{OL} = 16 mA		0.47	0.7		0.47	0.7	V
		Other outputs	V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	Any S	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Any A or B					100			100	
		C_n ('LS381A)					80			80	
		C_n ('LS382)					100			100	
I_{IL}	Low-level input current	Any S	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
		Any A or B					−1			−1	
		C_n ('LS381A)					−0.8			−0.8	
		C_n ('LS382)					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs grounded, Outputs open			35	65		35	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS381A			'LS382			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	C_n	Any F	R_L = 2 kΩ, C_L = 15 pF		18	27		18	27	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Any A or B	$\overline{G}$			20	30				ns
t_{PHL}					21	33				
t_{PLH}	Any A or B	$\overline{P}$			21	33				ns
t_{PHL}					23	33				
t_{PLH}	A_i or B_i	F_i			20	30		20	30	ns
t_{PHL}					15	23		15	23	
t_{PLH}	S_i	F_i			35	53		35	53	ns
t_{PHL}					34	51		34	51	
t_{PLH}	S_i	$\overline{G}$ or $\overline{P}$			31	47				ns
t_{PHL}					32	48				
t_{PLH}	Any A or B	C_{n+4}						28	42	ns
t_{PHL}								26	39	
t_{PLH}	Any A or B	OVR						23	35	ns
t_{PHL}								27	41	
t_{PLH}	S_i	C_{n+4} or OVR						38	57	ns
t_{PHL}								36	54	
t_{PLH}	C_n	OVR						10	15	ns
t_{PHL}								13	23	
t_{PLH}	C_n	C_{n+4}						13	21	ns
t_{PHL}								11	20	

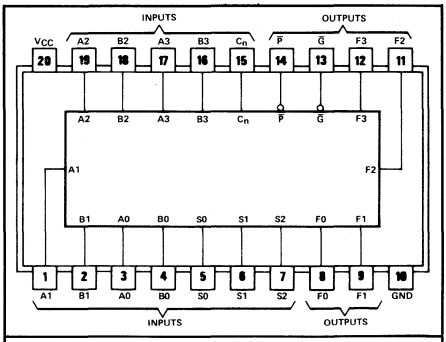
TYPES SN54S381, SN74S381
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

BULLETIN NO. DL-S 7612124, MARCH 1974 – REVISED OCTOBER 1976

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	17, 19, 1, 3	WORD A INPUTS
B3, B2, B1, B0	16, 18, 2, 4	WORD B INPUTS
S2, S1, S0	7, 6, 5	FUNCTION-SELECT INPUTS
C_n	15	CARRY INPUT FOR ADDITION, INVERTED CARRY INPUT FOR SUBTRACTION
F3, F2, F1, F0	12, 11, 9, 8	FUNCTION OUTPUTS
$\overline{P}$	14	INVERTED CARRY PROPAGATE OUTPUT
$\overline{G}$	13	INVERTED CARRY GENERATE OUTPUT
V_{CC}	20	SUPPLY VOLTAGE
GND	10	GROUND

SN54S381 . . . J PACKAGE
SN74S381 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

- **A Fully Parallel 4-Bit ALU in 20-Pin Package for 0.300-Inch Row Spacing**
- **Ideally Suited for High-Density Economical Processors**
- **Parallel Inputs and Outputs and Full Look-Ahead Provide System Flexibility**
- **Arithmetic and Logic Operations Selected Specifically to Simplify System Implementation:**
  A Minus B
  B Minus A
  A Plus B
  and Five Other Functions
- **Schottky-Clamped for High Performance**
  16-Bit Add Time . . . 26 ns Typ Using Look-Ahead
  32-Bit Add Time . . . 34 ns Typ Using Look-Ahead

FUNCTION TABLE

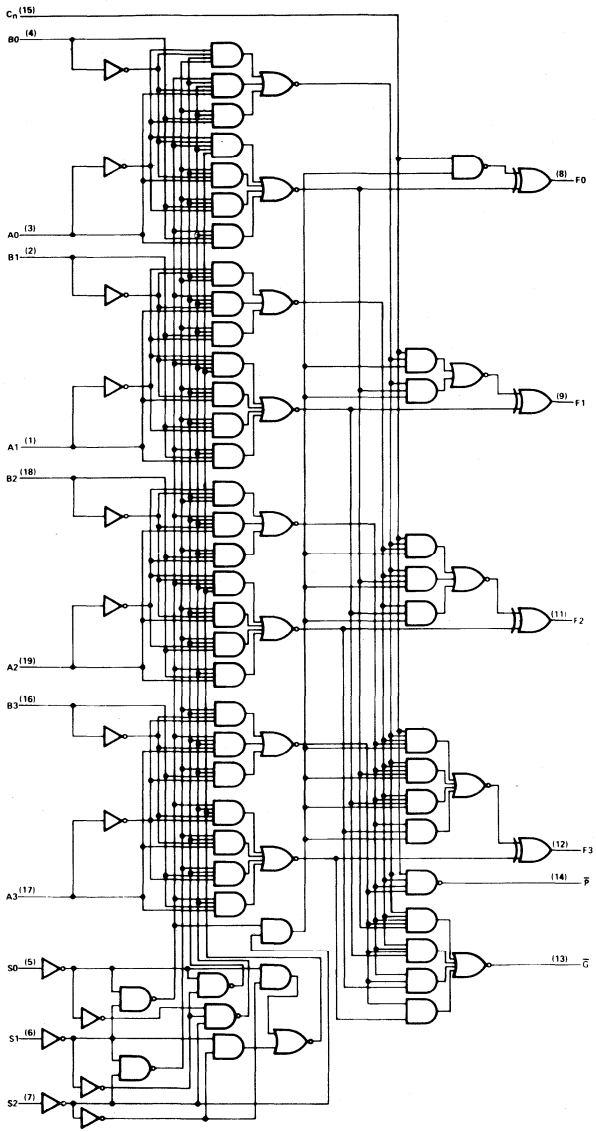
SELECTION			ARITHMETIC/LOGIC
S2	S1	S0	OPERATION
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

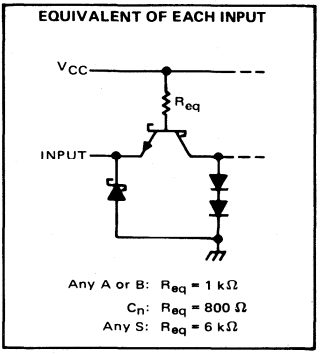
H = high level, L = low level

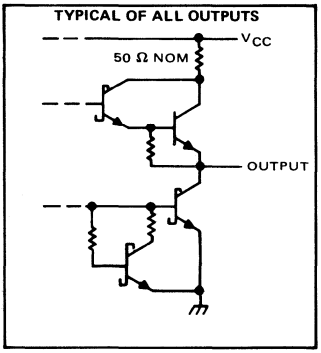
description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading SN54182/SN74182 or SN54S182/SN74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the '182 and 'S182. The typical addition times shown above illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

functional block diagram and schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54S381 . . . . . −55°C to 125°C
SN74S381 . . . . . 0°C to 70°C
Storage free-air temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with its respective B input; for example A0 with B0, etc.

recommended operating conditions

	SN54S381			SN74S381			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2	V
V_{OH}	High-level output voltage	SN54S381	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.4		V
		SN74S381	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Any S input	V_{CC} = MAX, V_I = 2.7 V			50	μA
		C_n				250	
		All others				200	
I_{IL}	Low-level input current	Any S input	V_{CC} = MAX, V_I = 0.5 V			−2	mA
		C_n				−8	
		All others				−6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX		105	160	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	Any F	C_L = 15 pF, R_L = 280 Ω, See Note 3		10	17	ns
t_{PHL}					10	17	
t_{PLH}	Any A or B	$\overline{G}$			12	20	ns
t_{PHL}					12	20	
t_{PLH}	Any A or B	$\overline{P}$			11	18	ns
t_{PHL}					11	18	
t_{PLH}	A_i or B_i	F_i			18	27	ns
t_{PHL}					16	25	
t_{PLH}	Any S	Any			18	30	ns
t_{PHL}					18	30	

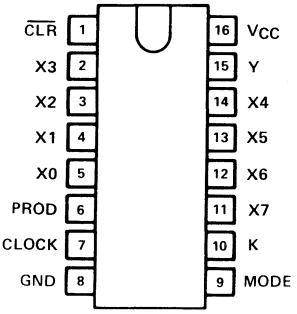
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54LS384, SN74LS384
8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

D2419, JANUARY 1981

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency
- Equivalent to 25LS14

SN54LS384 . . . J OR W PACKAGE
SN74LS384 . . . J OR N PACKAGE
(TOP VIEW)

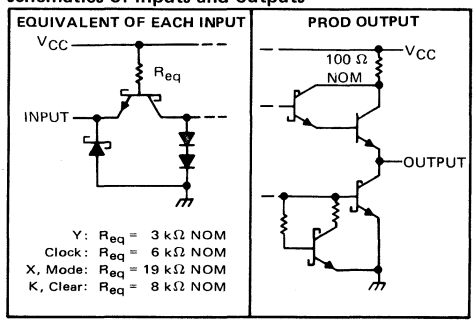


description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

schematics of inputs and outputs



The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

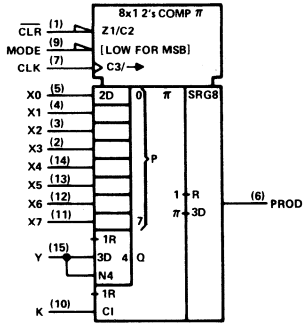
The SN54LS384 will be characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS384 will be characterized for operation from 0°C to 70°C.

FUNCTION TABLE

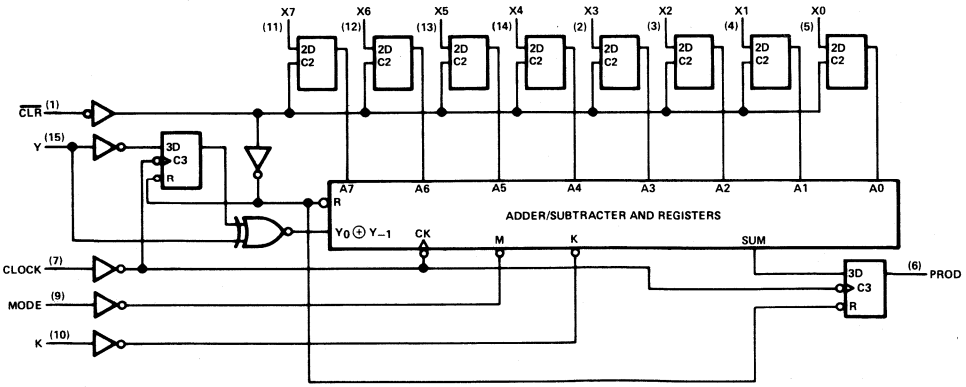
INPUTS				INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	X_i	Y	Y_{-1}	PROD	
L	X	Data	X	L	L	Load new multiplicand and clear internal sum and carry registers
H	↑	X	L	L	Output	Shift sum register
H	↑	X	L	H	per	Add multiplicand to sum register and shift
H	↑	X	H	L	Booth's	Subtract multiplicand from sum register and shift
H	↑	X	H	H	algorithm	Shift sum register

H = high-level, L = low-level, X = irrevelant, ↑ = low-to-high-level transition

logic symbol



functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS384 . . . . . −55°C to 125°C
SN74LS384 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54LS384			SN74LS384			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Setup time, t_{su}	Y before Clock ↑	45			38			ns
	K before Clock ↑	30			24			
	X before Clear ↓	23			19			
Clear inactive-state set up time before Clock ↑		30			20			ns
Hold time, t_h	Y after Clock ↑	0			0			
	K after Clock ↑	0			0			
	X after Clear ↓	2			2			
Pulse width, t_w	Clock high	20			20			ns
	Clock low	20			20			
	Clear low	38			33			
Operating free-air temperature, t_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS384			SN74LS384			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	X, Mode	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		K, Clear						30			30	
		Clock						40			40	
		Y						80			80	
I_{IL}	Low-level input current	X, Mode	V_{CC} = MAX,	V_I = 0.4 V				−0.48			−0.48	mA
		K, Clear						−1.2			−1.2	
		Clock						−1.6			−1.6	
		Y						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			91	155		91	155	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 4	25	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			15	23	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			17	25	ns

NOTE 4: Load circuit and waveforms are shown on page 3-11

TYPICAL APPLICATION DATA

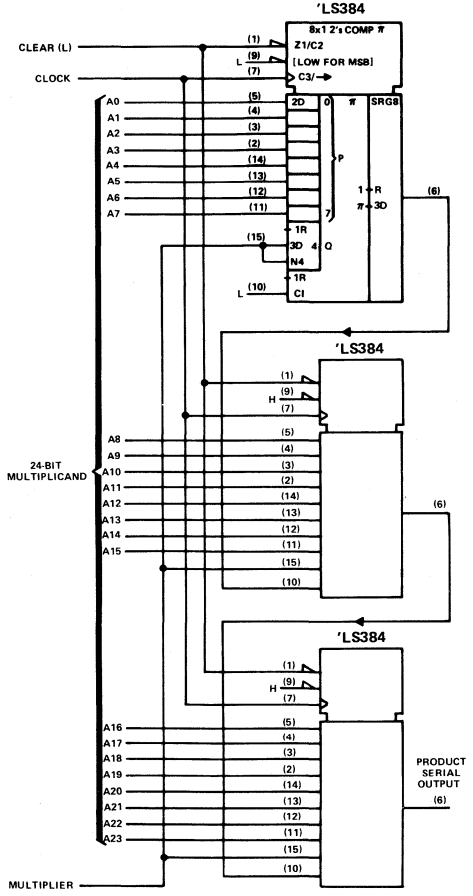


FIGURE 1–BASIC 24-BIT SERIAL/PARALLEL CONNECTION

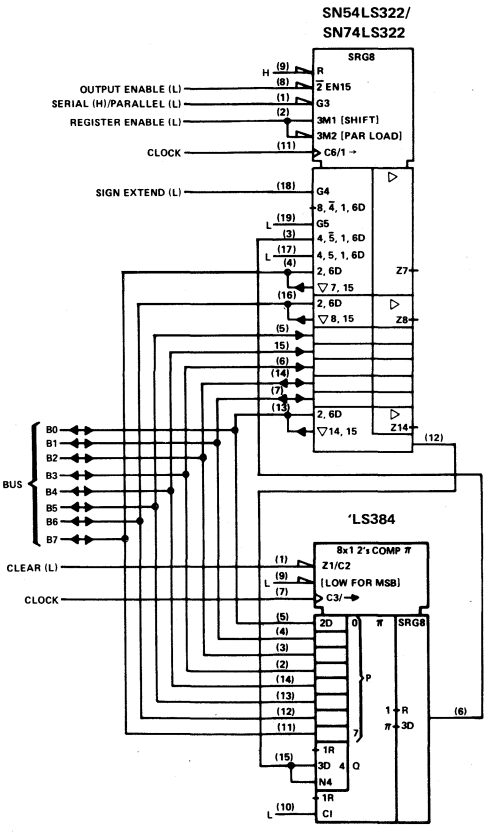


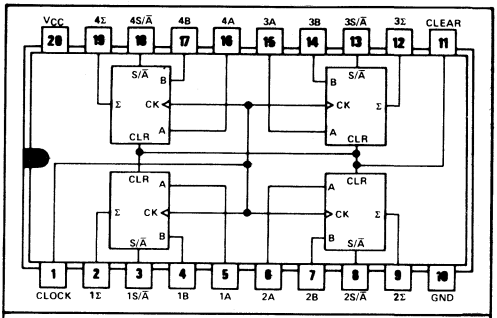
FIGURE 2–8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED WITH 8-BIT TRUNCATED PRODUCT

TYPES SN54LS385, SN74LS385
QUADRUPLE SERIAL ADDERS/SUBTRACTORS

D2412, NOVEMBER 1977

- **Four Synchronous Elements in a Single 20-Pin Package**
- **Buffered Clock and Direct Clear Inputs**
- **Independent Two's-Complement Addition/Subtraction**
- **Equivalent to 25LS15**

SN54LS385 . . . . J PACKAGE
SN74LS385 . . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

The 'LS385 is a general purpose adder/subtractor and is particularly useful as a companion part to the SN54LS384/SN74LS384 serial/parallel two's-complement multiplier. The 'LS385 contains four independent adder/subtractor elements with common clock and clear.

Each of the four independent sum (Σ) outputs reflects its respective A and B input as controlled by the S/$\overline{A}$ control. When S/$\overline{A}$ is high the Σ function is A minus B. When S/$\overline{A}$ is low the Σ function is A plus B.

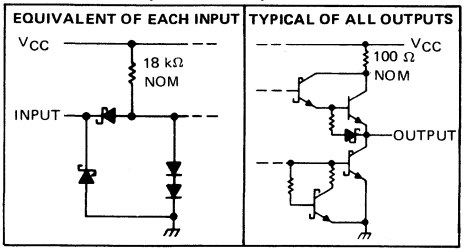
When low, the clear input asynchronously resets the sum flip-flop low and the carry flip-flop either high in the subtract mode or low in the add mode. The clock is positive-edge triggered and controls the sum and carry flip-flops according to the function table.

FUNCTION TABLE

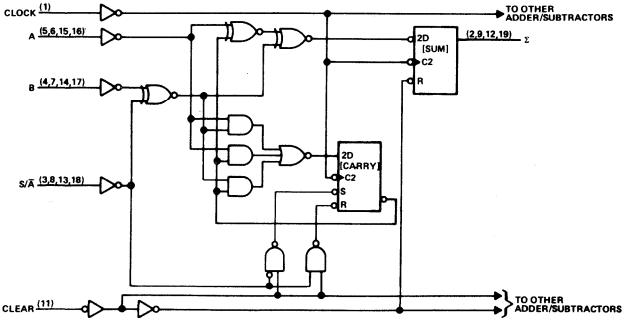
SELECTED	INPUTS					DATA IN CARRY FLIP-FLOP		Σ OUTPUT
FUNCTION	CLEAR	S/$\overline{A}$	A	B	CLOCK	BEFORE ↑	AFTER ↑	AFTER ↑
Clear	L	L	X	X	X	L	L	L
	L	H	X	X	X	H	H	L
Add	H	L	L	L	↑	L	L	L
	H	L	L	L	↑	H	L	H
	H	L	L	H	↑	L	L	H
	H	L	L	H	↑	H	H	L
	H	L	H	L	↑	L	L	H
	H	L	H	L	↑	H	H	L
	H	L	H	H	↑	L	H	L
	H	L	H	H	↑	H	H	H
Subtract	H	H	L	L	↑	L	L	H
	H	H	L	L	↑	H	H	L
	H	H	L	H	↑	L	L	L
	H	H	L	H	↑	H	L	H
	H	H	H	L	↑	L	H	L
	H	H	H	L	↑	H	H	H
	H	H	H	H	↑	L	L	H
	H	H	H	H	↑	H	H	L

H = high level, L = low level, X = irrelevant,
↑ = transition from low to high level at the clock input

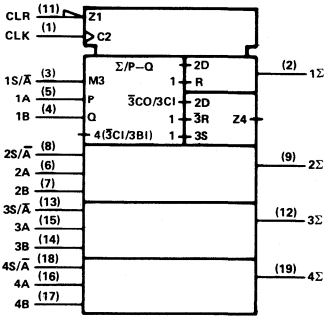
schematics of inputs and outputs



functional block diagram (each adder/subtractor, positive logic)



logic symbol



recommended operating conditions

	SN54LS385			SN74LS385			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	16			16			ns
Setup time, t_{su}	10			10			ns
Hold time, t_h	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS385			SN74LS385			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			48	75		48	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Note 3	30	40		MHz
t_{PLH}	Clock	Σ			14	22	ns
t_{PHL}					18	27	
t_{PHL}	Clear	Σ			18	30	ns

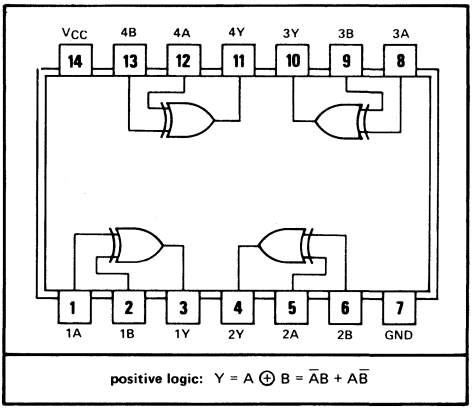
◇f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112.

TYPES SN54LS386A, SN74LS386A
QUADRUPLE 2-INPUT-EXCLUSIVE-OR GATES

BULLETIN NO. DL-S 7612118, MARCH 1974 – REVISED MARCH 1984

- Electrically Identical to SN54LS86/SN74LS86
- Total Average Propagation Delay Times . . . 10 ns
- Typical Total Power Dissipation . . . 30.5 mW

SN54LS386A . . . J OR W PACKAGE
SN74LS386A . . . J OR N PACKAGE
(TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

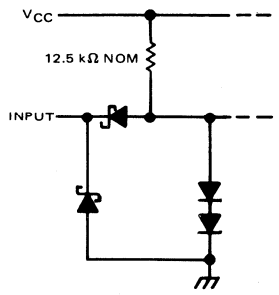
FUNCTION TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

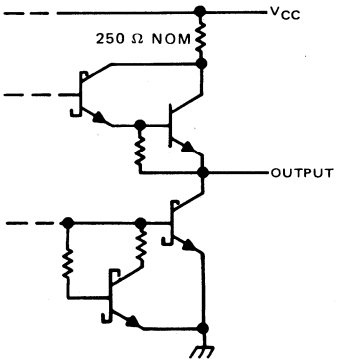
H = high level
L = low level

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS386A . . . . . −55°C to 125°C
SN74LS386A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS386A			SN74LS386A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS386A			SN74LS386A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 3		12	23	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			20	30	ns
t_{PHL}					13	22	

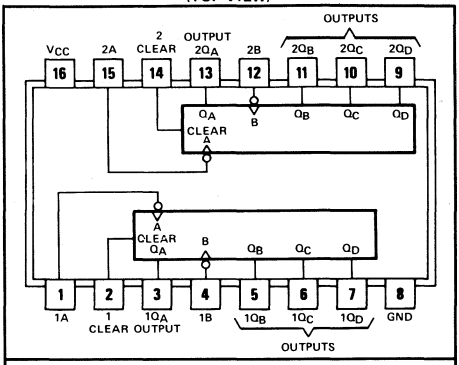
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54390, SN54LS390, SN54393, SN54LS393, SN74390, SN74LS390, SN74393, SN74LS393 DUAL 4-BIT DECADE AND BINARY COUNTERS

BULLETIN NO. DL-S 7612099, OCTOBER 1976

- Dual Versions of the Popular '90A, 'LS90 and '93A, 'LS93
- '390, 'LS390. . .Individual Clocks for A and B Flip-Flops Provide Dual ÷2 and ÷5 Counters
- '393, 'LS393. . .Dual 4-Bit Binary Counter with Individual Clocks
- All Have Direct Clear for Each 4-Bit Counter
- Dual 4-Bit Versions Can Significantly Improve System Densities by Reducing Counter Package Count by 50%
- Typical Maximum Count Frequency . . . 35 MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54390, SN54LS390 . . . J OR W PACKAGE
SN74390, SN74LS390 . . . J OR N PACKAGE
(TOP VIEW)



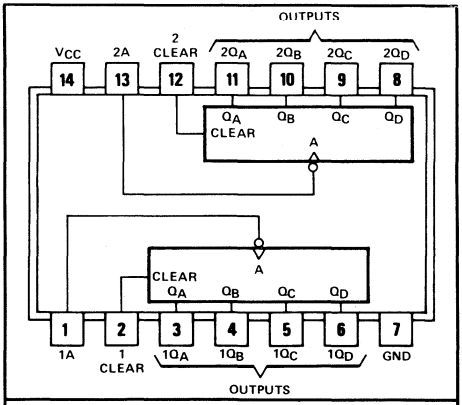
positive logic: High input to clear resets all four outputs low

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The '390 and 'LS390 incorporate dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The '393 and 'LS393 each comprise two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The '390, 'LS390, '393, and 'LS393 have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Series 54 and Series 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74LS circuits are characterized for operation from 0°C to 70°C.

SN54393, SN54LS393 . . . J OR W PACKAGE
SN74393, SN54LS393 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low

FUNCTION TABLES

'390, 'LS390
BCD COUNT SEQUENCE
(EACH COUNTER)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'390, 'LS390
BI-QUINARY (5-2)
(EACH COUNTER)
(See Note B)

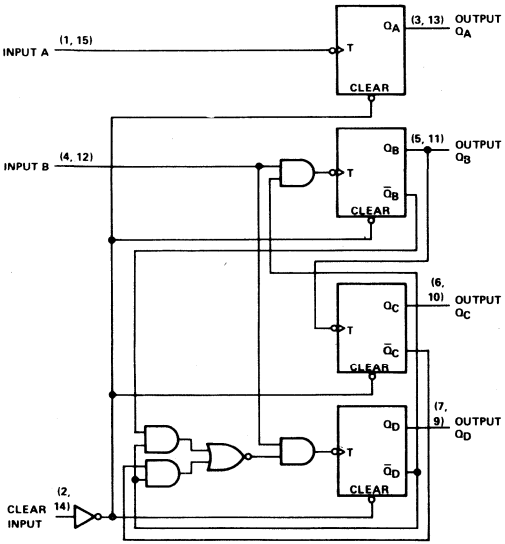
COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)

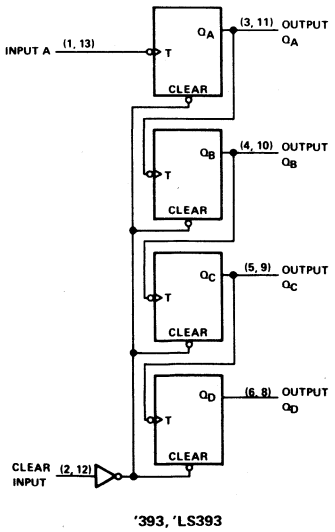
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. H = high level, L = low level.

functional block diagrams



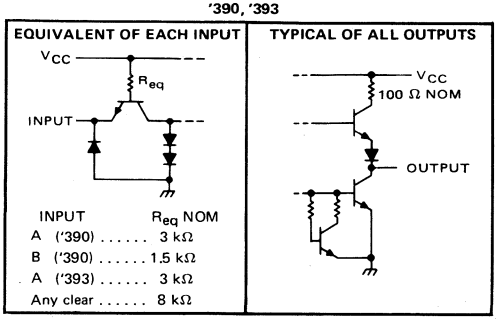
'390, 'LS390



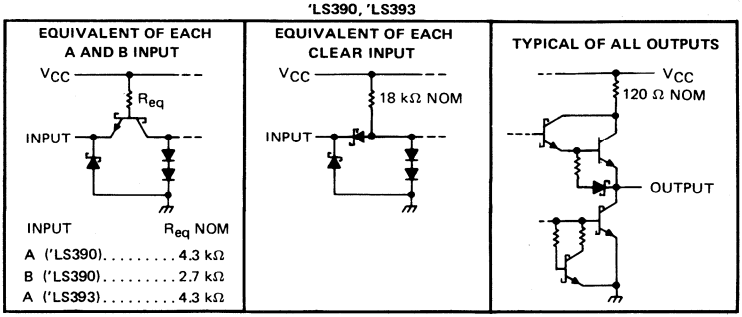
'393, 'LS393

schematics of inputs and outputs

'390, '393



'LS390, 'LS393



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54390, SN54393 . . . . . −55°C to 125°C
SN74390, SN74393 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54390 SN54393			SN74390 SN74393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		20	0		20	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	25			25			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'390 MIN	'390 TYP‡	'390 MAX	'393 MIN	'393 TYP‡	'393 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Clear	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Input A					80			80	
		Input B					120				
I_{IL}	Low-level input current	Clear	V_{CC} = MAX, V_I = 0.4 V				−1			−1	mA
		Input A					−3.2			−3.2	
		Input B					−4.8				
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			42	69		38	64	mA

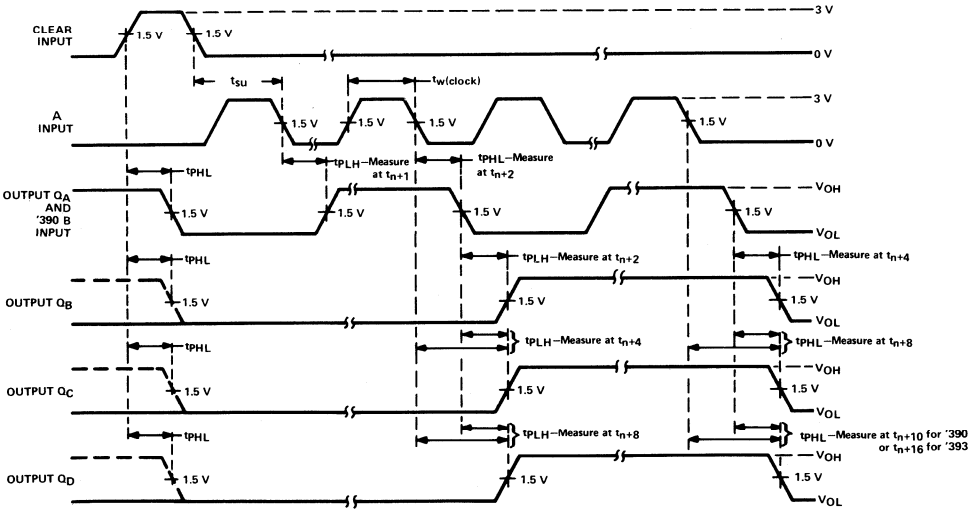
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶The Q_A outputs of the '390 are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'390			'393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 3 and Figure 1	25	35		25	35		MHz
	B	Q_B		20	30					
t_{PLH}	A	Q_A			12	20		12	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	A	Q_C of '390 Q_D of '393			37	60		40	60	ns
t_{PHL}					39	60		40	60	
t_{PLH}	B	Q_B			13	21				ns
t_{PHL}					14	21				
t_{PLH}	B	Q_C			24	39				ns
t_{PHL}					26	39				
t_{PLH}	B	Q_D			13	21				ns
t_{PHL}					14	21				
t_{PHL}	Clear	Any			24	39		24	39	ns

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit is shown on page 3-10.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Clear input voltage . . . . . 7 V
Any A or B clock input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS390, SN54LS393 . . . . . −55°C to 125°C
SN74LS390, SN74LS393 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS390 SN54LS393			SN74LS390 SN74LS393			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count}	A input	0		25	0		25	MHz
	B input	0		12.5	0		12.5	
Pulse width, t_w	A input high or low	20			20			ns
	B input high or low	40			40			
	Clear high	20			20			
Clear inactive-state setup time, t_{su}		25↓			25↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA¶					0.35	0.5	
I_I Input current at maximum input voltage	Clear	V_{CC} = MAX	V_I = 7 V			0.1			0.1	mA
	Input A		V_I = 5.5 V			0.2			0.2	
	Input B					0.4			0.4	
I_{IH} High-level input current	Clear	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
	Input A					100			100	
	Input B					200			200	
I_{IL} Low-level input current	Clear	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Input A					−1.6			−1.6	
	Input B					−2.4			−2.4	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2	'LS390		15	26		15	26	mA
			'LS393		15	26		15	26	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ The Q_A outputs of the 'LS390 are tested at I_{OL} = MAX plus the limit value for I_{IL} for the clock B input. This permits driving the clock B input while maintaining full fan-out capability.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

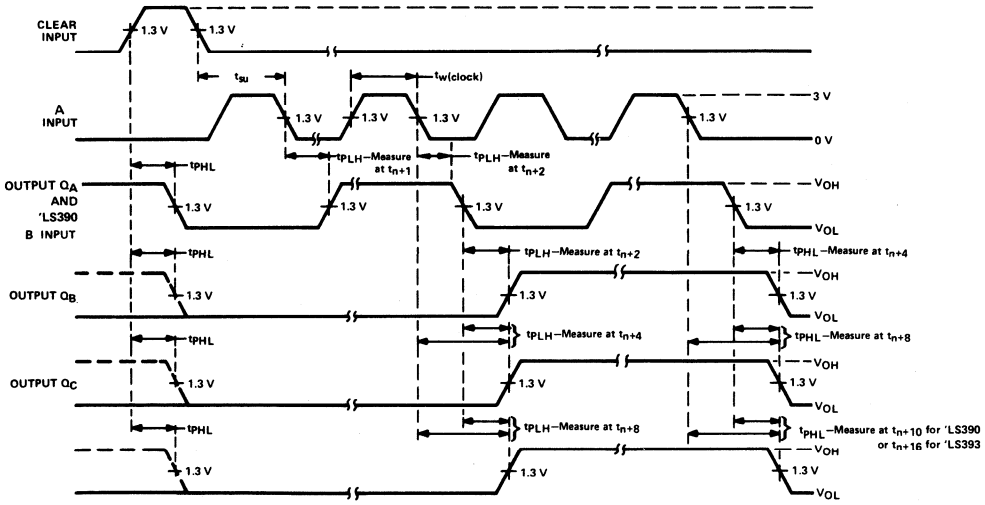
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS390			'LS393			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Note 4 and Figure 2	25	35		25	35		MHz
	B	Q_B		12.5	20					
t_{PLH}	A	Q_A			12	20		12	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	A	Q_C of 'LS390 Q_D of 'LS393			37	60		40	60	ns
t_{PHL}					39	60		40	60	
t_{PLH}	B	Q_B			13	21				ns
t_{PHL}					14	21				
t_{PLH}	B	Q_C			24	39				ns
t_{PHL}					26	39				
t_{PLH}	B	Q_D			13	21				ns
t_{PHL}					14	21				
t_{PHL}	Clear	Any			24	39		24	39	ns

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuit is shown on page 3-11.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

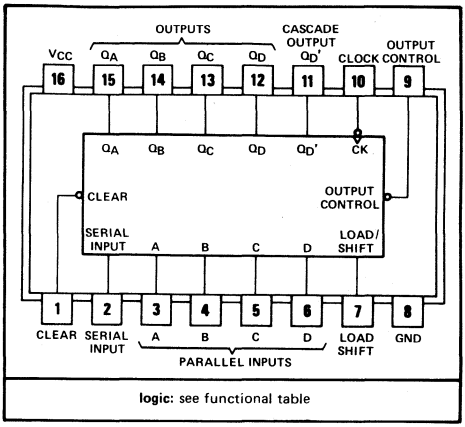
NOTE A: Input pulses are supplied by a generator having the following characteristics $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

TYPES SN54LS395A, SN74LS395A
4-BIT CASCADABLE SHIFT REGISTERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612114, OCTOBER 1976

- Three-State, 4 Bit, Cascadable, Parallel-In, Parallel-Out Registers
- 'LS395A Offers Three Times the Sink-Current Capability of 'LS395
- Low Power Dissipation . . . 75 mW Typical (Enabled)
- Applications:
  - N-Bit Serial-To-Parallel Converter
  - N-Bit Parallel-To-Serial Converter
  - N-Bit Storage Register

SN54LS395A . . . J OR W PACKAGE
SN74LS395A . . . J OR N PACKAGE
(TOP VIEW)



logic: see functional table

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D' is still available for cascading.

7

FUNCTION TABLE

INPUTS								3-STATE OUTPUTS				CASCADE OUTPUT
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	Q_D'
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

See explanation of function tables on page 3-8.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS395A . . . . . −55°C to 125°C
SN74LS395A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS395A			SN74LS395A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			−1			−2.6	mA
	Q_D'			−400			−400	μA
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D			12			24	mA
	Q_D'			4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock pulse, $t_{w(clock)}$		16			16			ns
Setup time, high-level or low-level data, t_{su}	Load/Shift input	40			40			ns
	All other inputs	20			20			
Hold time, high-level or low-level data, t_h		10			10			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS395A			SN74LS395A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	Q_A, Q_B, Q_C, Q_D	2.4	3.4		2.4	3.1		V
				Q_D'	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{IH} = 2 V	Q_A, Q_B, Q_C, Q_D	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
			Q_D	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.7 V	V_{IH} = 2 V,	Q_A, Q_B, Q_C, Q_D			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.4 V	V_{IH} = 2 V,	Q_A, Q_B, Q_C, Q_D			−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		Q_A, Q_B, Q_C, Q_D	−30		−130	−30		−130	mA
				Q_D'	−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	Condition A		22	34		22	34	mA
				Condition B		21	31		21	31	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time,and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:
A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

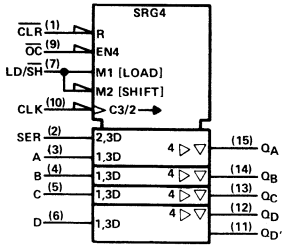
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	See Note 3, Q_A, Q_B, Q_C, Q_D outputs: R_L = 667 Ω, C_L = 45 pF; Q_D' output: R_L = 2 kΩ, C_L = 15 pF	30	45		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	30	ns
t_{PZH}	Output enable time to high level			15	25	ns
t_{PZL}	Output enable time to low level			17	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF, See Note 3		11	17	ns
t_{PLZ}	Output disable time from low level			12	20	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

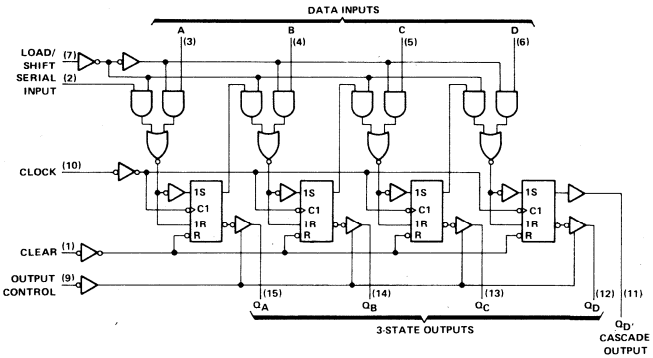
functional block diagram

logic symbol

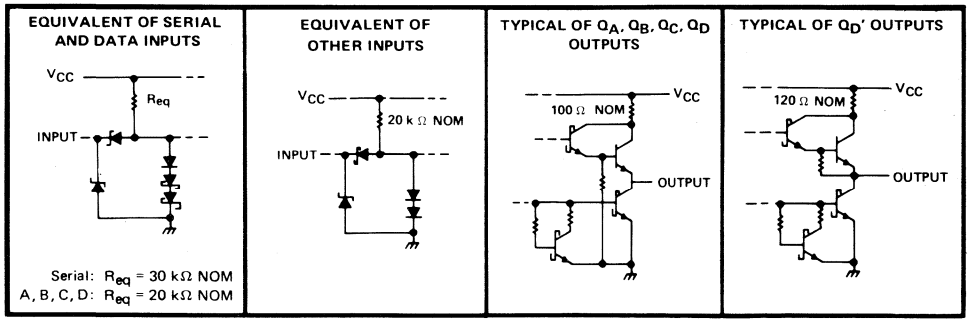


Pin numbers shown are for J and N packages.

logic diagram (positive logic)



schematics of inputs and outputs

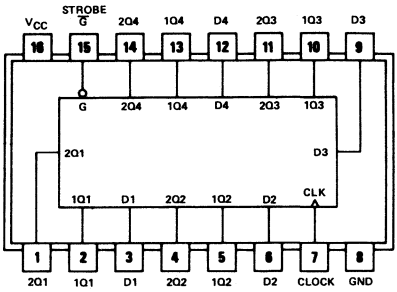


TYPES SN54LS396, SN74LS396
OCTAL STORAGE REGISTERS

D2329, MARCH 1977

- Parallel Access
- Typical Propagation Delay Time . . . 20 ns
- Typical Power Dissipation . . . 120 mW
- Applications:
  N-Bit Storage Files
  Hex/BCD Serial-To-Parallel Converters

SN54LS396 . . . J OR W PACKAGE
SN74LS396 . . . J OR N PACKAGE
(TOP VIEW)



description

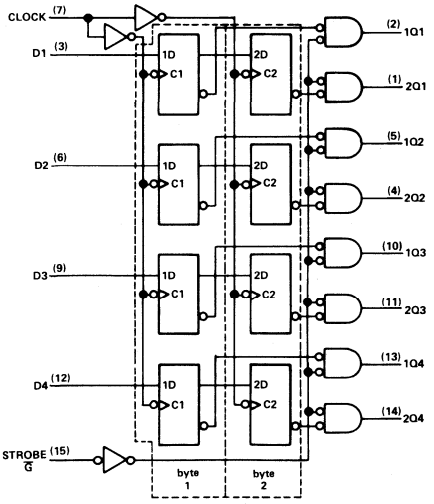
These octal registers are organized as two 4-bit bytes of storage. Upon application of a positive-going clock signal, the information stored in byte 1 is transferred into byte 2 as a new 4-bit byte is loaded into the byte 1 location via the four data lines. The full 8-bit word is available at the outputs after two clock cycles. Both the clock and the strobe lines are fully buffered.

FUNCTION TABLE

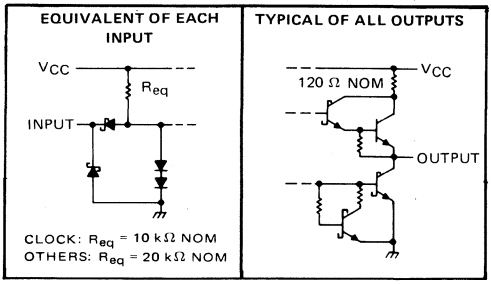
INPUTS						OUTPUTS							
STROBE $\overline{G}$	CLOCK	DATA				BYTE 1				BYTE 2			
		D1	D2	D3	D4	1Q1	1Q2	1Q3	1Q4	2Q1	2Q2	2Q3	2Q4
H	X	X	X	X	X	L	L	L	L	L	L	L	L
L	↑	a	b	c	d	a	b	c	d	$1Q1_n$	$1Q2_n$	$1Q3_n$	$1Q4_n$

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↑ = transition from low to high level
$1Q1_n$, $1Q2_n$, $1Q3_n$, $1Q4_n$ = the level of 1Q1, 1Q2, 1Q3, and 1Q4, respectively, before the most recent ↑ transition of the clock.

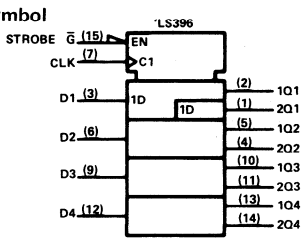
functional block diagram



schematics of inputs and outputs



logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS396 . . . . . −55°C to 125°C
SN74LS396 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS396			SN74LS396			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS396			SN74LS396			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Clock input	V_{CC} = MAX,	V_I = 7 V			0.2			0.2	mA
		Other inputs					0.1			0.1	
I_{IH}	High-level input current	Clock input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Other inputs					20			20	
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX,	V_I = 0.4 V			−0.8			−0.8	mA
		Other inputs					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		24	40		24	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from strobe			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from strobe			20	30	

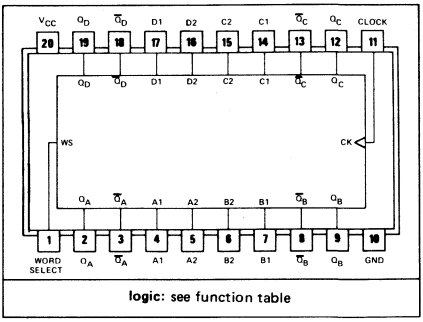
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS398, SN54LS399
SN74LS398, SN74LS399
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

BULLETIN NO. DL-S 7612465, OCTOBER 1976

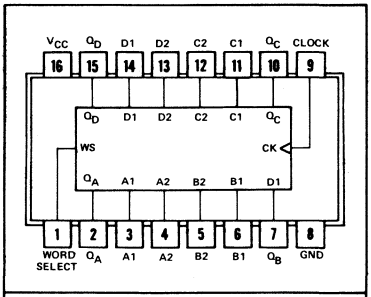
- Double-Rail Outputs on 'LS398
- Single-Rail Outputs on 'LS399
- 'LS398 is Similar to 'LS298, Which Has Inverted Clock
- Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock
- Applications:
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
  - Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities
- 'LS399 is equivalent to 25LS09

SN54LS398 . . . J OR W PACKAGE
SN74LS398 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

SN54LS399 . . . J OR W PACKAGE
SN74LS399 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54LS157/SN74LS157 and SN54LS175/SN74LS175) in a single 16-pin or 20-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the positive-going edge of the clock pulse.

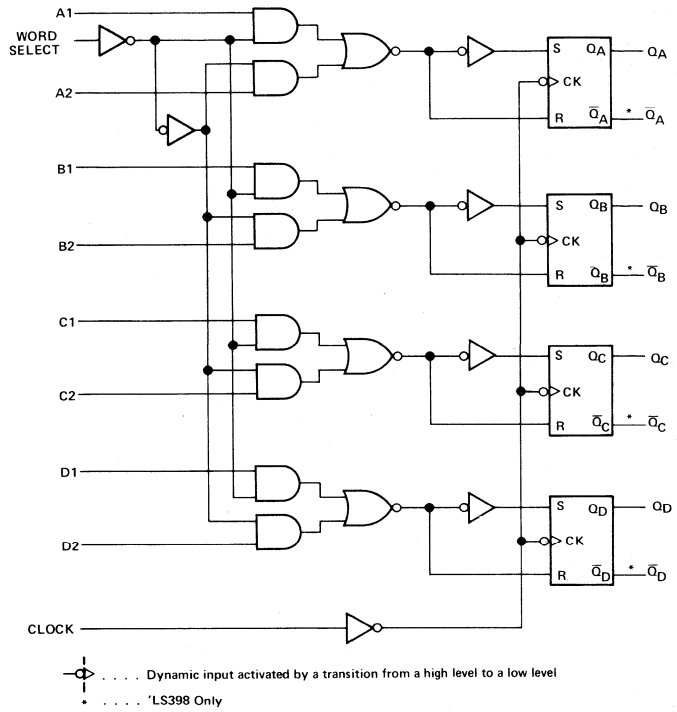
Typical power dissipation is 37 milliwatts. SN54LS398 and SN54LS399 are characterized for operation over the full military range of −55°C to 125°C, SN74LS398 and SN74LS399 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

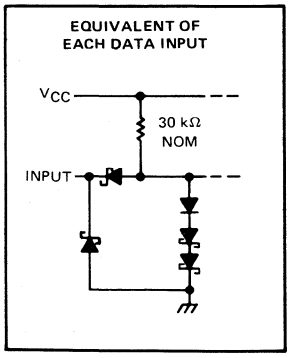
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↑	a1	b1	c1	d1
H	↑	a2	b2	c2	d2
X	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

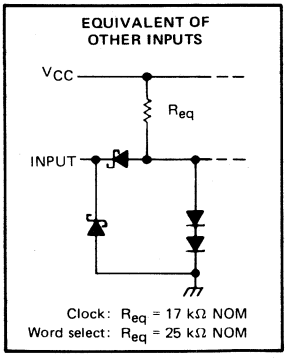
See explanation of function tables on page 3-8.

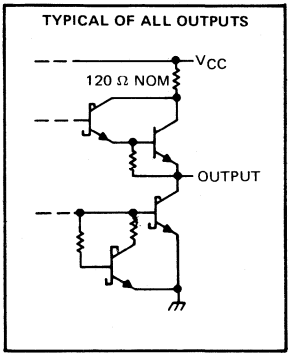
functional block diagram



schematics of inputs and outputs







TYPES SN54LS398, SN54LS399, SN74LS398, SN74LS399
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

REVISED JANUARY 1981

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{su}	Data	25			25			ns
	Word select	45			45			
Hold time, t_h	Data	0			0			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			7.3	13		7.3	13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 2 kΩ, See Note 3		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	

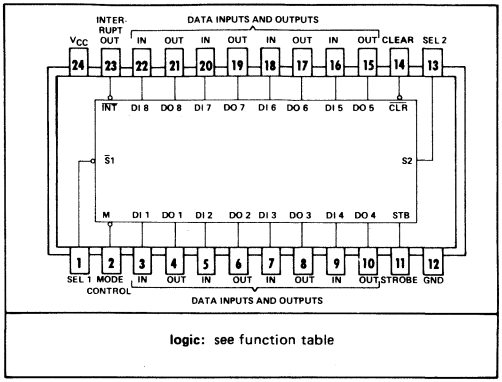
NOTE 3: Load circuit and waveforms are shown on page 3-11.

TYPES SN54S412, SN74S412 (TIM8212)
MULTI-MODE BUFFERED LATCHES

BULLETIN NO. DL-S 7512351, OCTOBER 1975

- P-N-P Inputs and 3-State Outputs Maximize I/O and Data Bus Capabilities
- Data Latch Transparency Permits Asynchronous or Latched Receiver Modes
- Mode and Select Inputs Permit Storing With Outputs Enabled or Disabled
- Strobe-Controlled Flag Flip-Flop Indicates Status or Interrupt
- Asynchronous Clear Sets All Eight Data Lines Low and Initializes Status Flag
- High-Level Output Voltage, Typically 4 V, Drives Most MOS Functions Directly
- Direct Replacement for Intel 3212 or 8212

SN54S412 . . . J PACKAGE
SN74S412 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

description

This high-performance eight-bit parallel expandable buffer register incorporates package and mode selection inputs and an edge-triggered status flip-flop designed specifically for implementing bus-organized input/output ports. The three-state data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides package busy or request interrupt commands. The outputs, with a 4-volt typical high-level voltage, are compatible for driving low-threshold MOS directly.

7

DATA LATCHES

The eight data latches are fully transparent when the internal gate enable, G, input is high and the outputs are enabled (OE = H). Latch transparency is selected by the mode control (M), select ($\overline{S1}$ and S2), and the strobe (STB) inputs and during transparency each data output (DO_i) follows its respective data input (DI_i). This mode of operation can be terminated by clearing, de-selecting, or holding the data latches. See data latches function table.

MODE SELECTION

An input mode or an output mode is selectable from this single input line. In the input mode, MD = L, the eight data latch inputs are enabled when the strobe is high regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken low, the latches will store the most-recently setup data.

In the output mode, M = H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S1}$ and S2) inputs. See data latches function table.

STATUS FLIP-FLOP

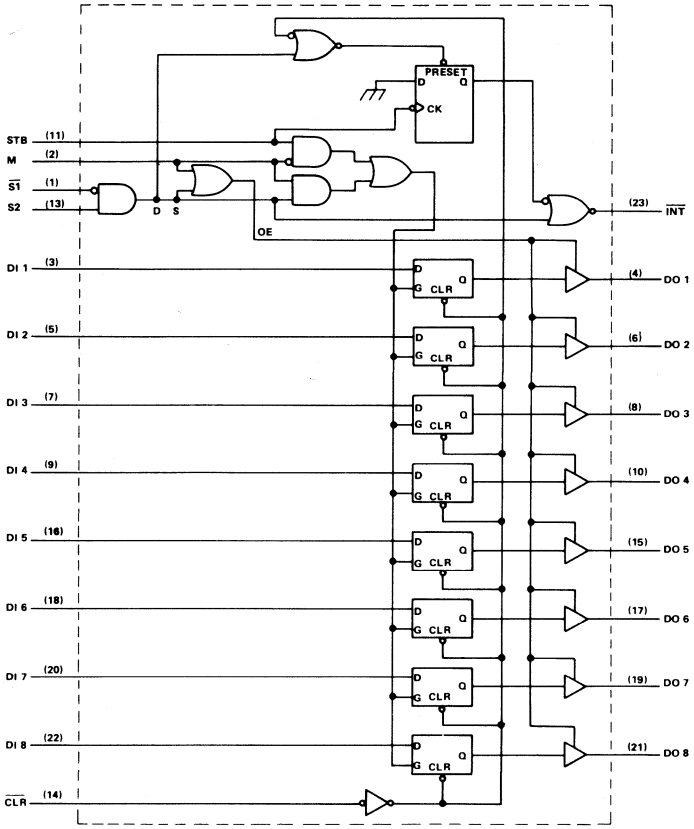
The status flip-flop provides a low-level output signal when:

a. the package is selected

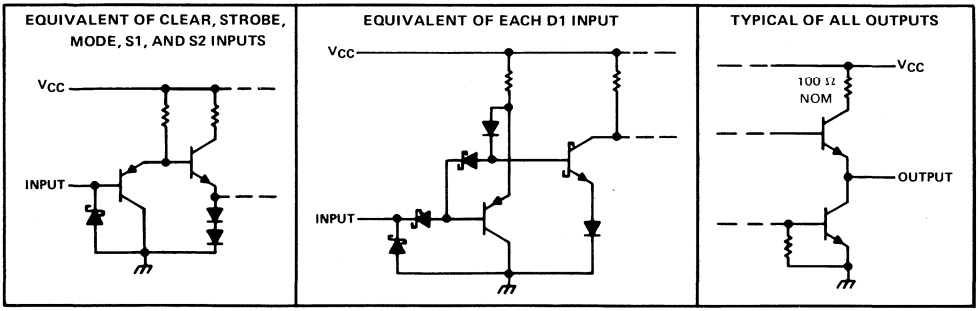
b. a strobe input is received.

This status signal can be used to indicate that the register is busy or to initiate an interrupt type command.

functional block diagram



schematics of inputs and outputs



DATA LATCHES FUNCTION TABLE

FUNCTION	CLEAR	M	$\overline{S1}$	S2	STB	DATA IN	DATA OUT
Clear	L	H	H	X	X	X	L
	L	L	L	H	L	X	L
De-select	X	L	X	L	X	X	Z
	X	L	H	X	X	X	Z
Hold	H	H	H	L	X	X	Q_0
	H	L	L	H	L	X	Q_0
Data Bus	H	H	L	H	X	L	L
	H	H	L	H	X	H	H
Data Bus	H	L	L	H	H	L	L
	H	L	L	H	H	H	H

STATUS FLIP-FLOP FUNCTION TABLE

CLEAR	$\overline{S1}$	S2	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H ≡ high level (steady state)
L ≡ low level (steady state)
X ≡ irrelevant (any input, including transitions)
Z ≡ high impedance (off)
↓ ≡ transition from low to high level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S412 . . . . . −55°C to 125°C
SN74S412 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S412			SN74S412			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Pulse width, t_w (see Figures 1, 2, and 4)	STB or $\overline{S1}$ • S2	25			25			ns
	Clear low	25			25			
Setup time, t_{su} (see Figure 3)		15↓			15↓			ns
Hold time, t_h (see Figures 1 and 3)		20↓			20↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓ The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S412			SN74S412			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.85			0.85	V
V_{IK}	Input clamp voltage		V_{CC} = MIN;	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	3.4	4		3.65	4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 15 mA			0.45			0.45	V
				I_{OL} = 20 mA			0.5			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	DO 1 thru DO 8	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 5.25 V			20			10	μA
I_{IL}	Low-level input current	$\overline{S1}$	V_{CC} = MAX,	V_I = 0.4 V			−1			−1	mA
		M					−0.75			−0.75	
		All others					−0.25			−0.25	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−65	−20		−65	mA
I_{CC}	Supply current		V_{CC} = MAX,	see Note 2		82			82	130	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open, clear input at 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM	TO	FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	STB, $\overline{S1}$, or S2	Any DO	1	C_L = 30 pF, See Note 3		18	27	ns
t_{PHL}						15	25	
t_{PHL}	$\overline{CLR}$	Any DO	2			18	27	ns
t_{PLH}	DI_i	DO_i	3			12	20	ns
t_{PHL}						10	20	
t_{PLH}	$\overline{S1}$ or S2	$\overline{INT}$	4	C_L = 30 pF, See Note 3		12	20	ns
t_{PHL}	STB	$\overline{INT}$	4			16	25	
t_{PZH}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 30 pF, See Note 3		21	35	ns
t_{PZL}						25	40	
t_{PHZ}	$\overline{S1}$, S2, or M	Any DO	5	C_L = 5 pF, See Note 3		9	20	ns
t_{PLZ}						12	20	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

PARAMETER MEASUREMENT INFORMATION

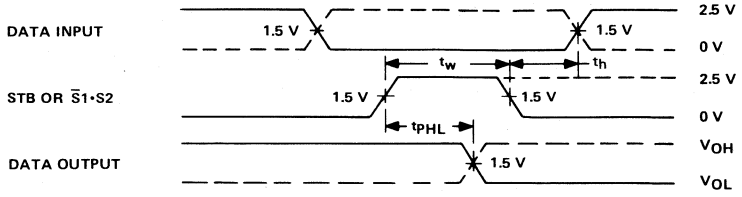


FIGURE 1 – STROBE OR SELECT TO DATA OUTPUT

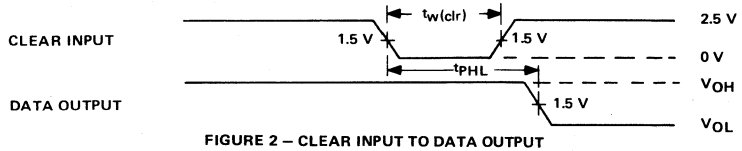


FIGURE 2 – CLEAR INPUT TO DATA OUTPUT

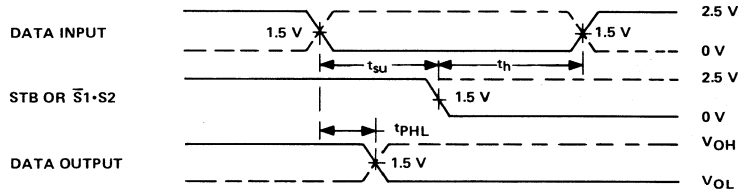


FIGURE 3 – DATA INPUT TO DATA OUTPUT

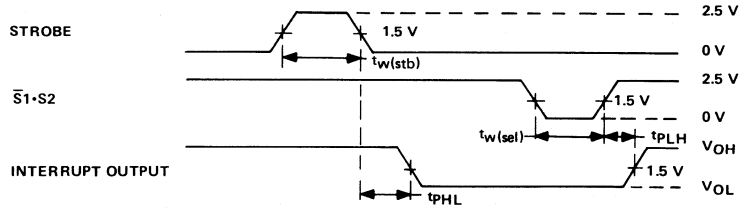


FIGURE 4 – STROBE OR SELECT TO INTERRUPT OUTPUT

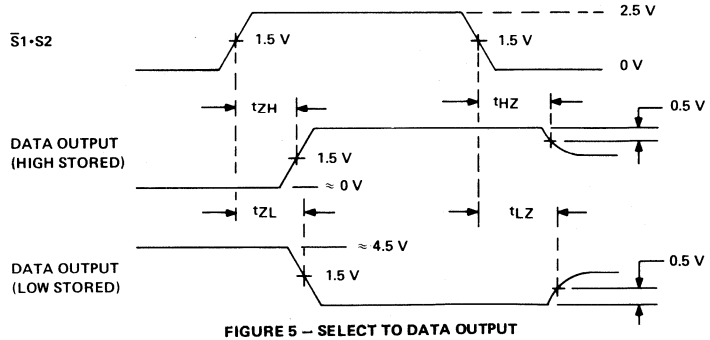


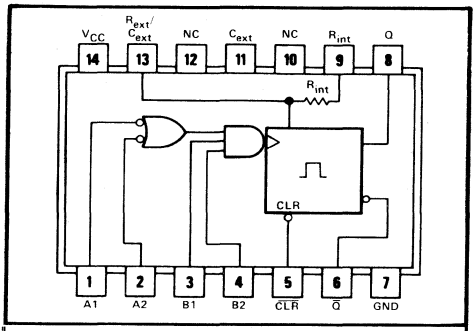
FIGURE 5 – SELECT TO DATA OUTPUT

TYPES SN54LS422, SN54LS423, SN74LS422, SN74LS423
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

D2536, JANUARY 1980

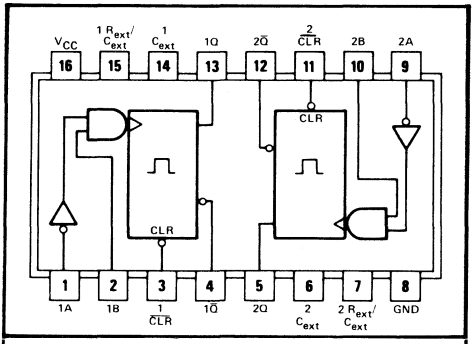
- **Will Not Trigger from Clear**
- **D-C Triggered from Active-High or Active-Low Gated Logic Inputs**
- **Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle**
- **Overriding Clear Terminates Output Pulse**
- **Compensated for V_{CC} and Temperature Variations**
- **'LS422 Has Internal Timing Resistor**

SN54LS422 . . . J OR W PACKAGE
SN74LS422 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see functional table

SN54LS423 . . . J OR W PACKAGE
SN74LS423 . . . J OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



logic: see functional table

description

The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C.

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of 'LS422, connect R_{int} to V_{CC}.
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

description (continued)

'LS422
FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎

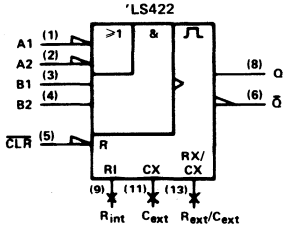
'LS423
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

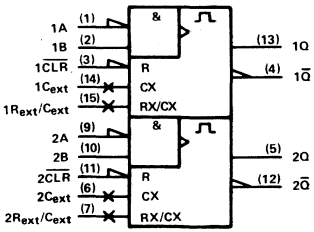
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input, including transitions)
⎍ = one high-level pulse
⎎ = one low-level pulse

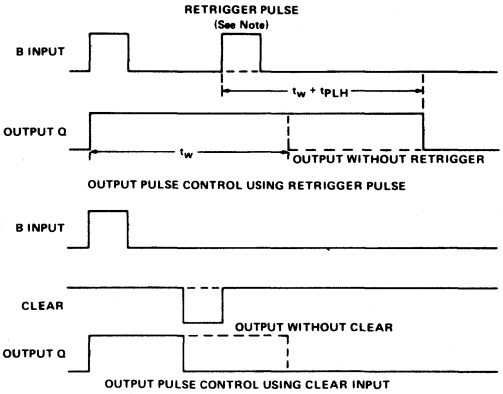
logic symbols

'LS422



'LS423

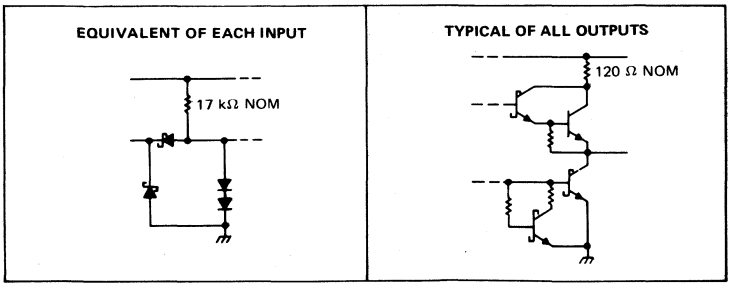




NOTE: If retrigger pulse starts before 0,22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse, output pulse extension may be shorter than $t_w + t_{PLH}$.

FIGURE 1–TYPICAL INPUT/OUTPUT PULSES

schematics of inputs and outputs



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_w	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	kΩ
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current (quiescent or triggered)	V_{CC} = MAX,	See Note 6	'LS422		6	11		6	11	mA
				'LS423		12	20		12	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 5. To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.
6. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 7

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, C_L = 15 pF,	R_{ext} = 5 kΩ, R_L = 2 kΩ		23	33	ns
	B					23	44	
t_{PHL}	A	$\overline{Q}$				32	45	ns
	B					34	56	
t_{PHL}	Clear	Q				20	27	ns
t_{PLH}		$\overline{Q}$				28	45	
t_{wQ} (min)	A or B	Q				116	200	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 2 kΩ	4	4.5	5	μs

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
NOTE 7: Load circuit and voltage waveforms are shown on page 3-11 of "The TTL Data Book for Design Engineers", second edition.

TYPICAL APPLICATION DATA

The basic output pulse width is determined by the value of external capacitance and timing resistance.

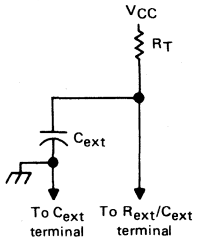
Figure 3 gives curves for output pulse widths ranging from 0.1 μs to 100 μs for several R_T and C_{ext} values. For output pulse widths greater than 100 μs or external capacitance greater than 1000 pF the following equation should be used.

$$t_w = K \cdot R_T \cdot C_{ext}$$

where

t_w is in ns
K is the multiplying factor and is approximately 0.45 for $C_{ext} \geq 1000$ pF.
C_{ext} is in pF

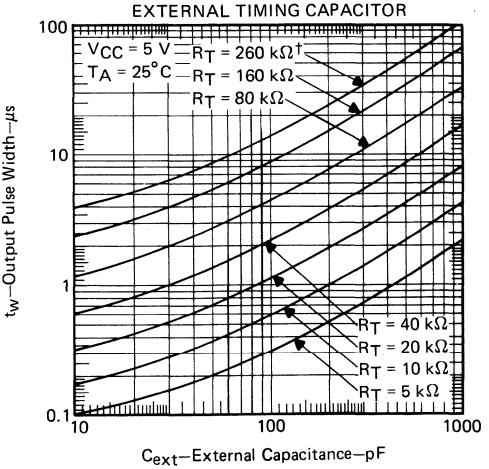
For best results, system ground should be applied to the C_{ext} terminal. These devices do not require a switching diode in series with the R_{ext}/C_{ext} terminal (as required by some other monostable multivibrators).



TIMING COMPONENT CONNECTIONS

FIGURE 2

TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITOR



†This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3

TYPES SN74S428(TIM8228), SN74S438(TIM8238) CONTROLLER AND BUS DRIVER FOR 8080A SYSTEMS

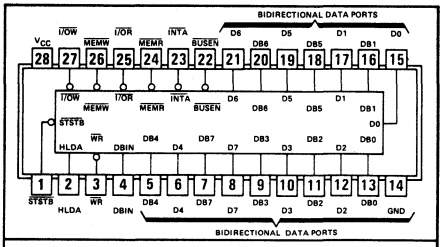
BULLETIN NO. DL-S 12468, OCTOBER 1976

- **Designed to Be Interchangeable with Intel 8228 and 8238**

PIN DESIGNATIONS

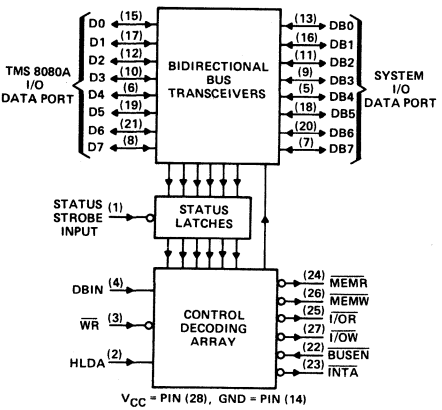
DESIGNATION	PIN NOS.	FUNCTION
D0 thru D7	15, 17, 12, 10, 6, 19, 21, 8	BIDIRECTIONAL DATA PORT (TO TMS 8080A)
DB0 thru DB7	13, 16, 11, 9, 5, 18, 20, 7	BIDIRECTIONAL DATA PORT (TO SYSTEM BUS)
$\overline{I/OR}$	25	READ OUTPUT TO I/O (ACTIVE LOW)
$\overline{IO/W}$	27	WRITE OUTPUT TO I/O (ACTIVE LOW)
$\overline{MEMR}$	24	READ OUTPUT TO MEMORY (ACTIVE LOW)
$\overline{MEMW}$	26	WRITE OUTPUT TO MEMORY (ACTIVE LOW)
DBIN	4	INPUT TO INDICATE TMS 8080A IS IN INPUT MODE (ACTIVE HIGH)
$\overline{INTA}$	23	INTERRUPT ACKNOWLEDGE OUTPUT (ACTIVE LOW)
HLDA	2	HOLD ACKNOWLEDGE INPUT (ACTIVE HIGH) FROM TMS 8080A
$\overline{WR}$	3	INPUT TO INDICATE TMS 8080A IS IN WRITE MODE (ACTIVE LOW)
$\overline{BUSEN}$	22	SYSTEM DATA PORT ENABLE INPUT (ACTIVE LOW)
$\overline{STSTB}$	1	SYNCHRONIZING STATUS STROBE INPUT FROM SN74LS424 (TIM8224)
V_{CC}	28	SUPPLY VOLTAGE (5 V)
GND	14	GROUND

N PACKAGE
(TOP VIEW)



logic: see description

functional block diagram



description

These monolithic Schottky-clamped †TTL system controllers are designed specifically to provide bus-driving and peripheral-control capabilities for interfacing memory and I/O devices with the 8080A in small to medium-large microcomputer systems.

A bidirectional eight-bit parallel bus driver is provided that isolates the 8080A bus from the memory and I/O data bus allowing the system designed to utilize cost-effective memory and peripheral devices while obtaining the maximum efficiency from the microprocessor. The TTL system drivers also provide increased fan-out with a lower impedance that enhances noise margins on the system bus.

Implementation of the status latches and control decoding array of the SN74S428/SN74S438 provides for using either a single-level interrupt vector RST7 for small systems, or multiple-byte call instructions for systems needing unlimited interrupt levels.

TEXAS INSTRUMENTS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

description (continued)

With respect to the system clocks, the SN74S438 is configured to generate an advanced response for I/O or memory write output signals to further simplify peripheral control implementation of complex systems. See Figure 3.

8-bit parrallel bus transceiver

The 8-bit parallel bus transceiver buffers the 8080A data bus from the memory and I/O system bus by providing one port (DO through D7) to interface with the 8080A and another port (DBO through DB7) to interface with the system devices. The 8080A side of the transceiver is designed specifically to interface with the microprocessor data bus ensuring not only that the processor output drive capabilities are adequate, but also that the inputs are driven with enhanced noise margins. The system bus side features high fan-out buffers designed to drive a number of system devices simultaneously and directly. The system port is rated to sink ten milliamperes of current and to source one milliampere of current at standard low-threshold voltage levels.

Status lines from the 8080A instruction-status decoder and the system bus enable input (BUSEN) provide complete transceiver directional and enable control to ensure integrity of both the processor data and the system bus data.

status latches

During the beginning of each machine cycle, the six status latches receive status information from the 8080A data bus indicating the type of operation that will be performed. When the $\overline{\text{STSTB}}$ input goes low, the latches store the status data and generate the signals needed to enable and sequence the memory and I/O control outputs. The status words and types of machine cycles are enumerated in Table A.

TABLE A – STATUS WORDS

STATUS WORD	8080A STATUS OUTPUT								TYPE OF MACHINE CYCLE	'S428/'S438 COMMAND GENERATED
	D0	D1	D2	D3	D4	D5	D6	D7		
1	L	H	L	L	L	H	L	H	Instruction fetch	$\overline{\text{MEMR}}$
2	L	H	L	L	L	L	L	H	Memory read	$\overline{\text{MEMR}}$
3	L	L	L	L	L	L	L	L	Memory write	$\overline{\text{MEMW}}$
4	L	H	H	L	L	L	L	H	Stack read	$\overline{\text{MEMR}}$
5	L	L	H	L	L	L	L	L	Stack write	$\overline{\text{MEMW}}$
6	L	H	L	L	L	L	H	L	Input read	$\overline{\text{I/OR}}$
7	L	L	L	L	H	L	L	L	Output write	$\overline{\text{I/OW}}$
8	H	H	L	L	L	H	L	L	Interrupt acknowledge	$\overline{\text{INTA}}$
9	L	H	L	H	L	L	L	H	Halt acknowledge	NONE
10	H	H	L	H	L	H	L	L	Interrupt acknowledge at halt	$\overline{\text{INTA}}$
	INTA	$\overline{\text{WO}}$	STACK	HLTA	OUT	M1	INP	MEMR		
	STATUS INFORMATION									

decoding array

The decoding array receives enabling commands from the status latches and sequencing commands from the 8080A and generates memory and I/O read/write commands and an interrupt acknowledgement.

description (continued)

The read commands ($\overline{MEMR}$, $\overline{I/OR}$) and the interrupt acknowledgement ($\overline{INTA}$) are derived from the status bit(s) and the data bus input mode (DBIN) signal. The write commands ($\overline{MEMW}$, $\overline{I/OW}$) are derived from the status bit(s) and the write mode ($\overline{WR}$) signal. (See Table A.) All control commands are active low to simplify interfacing with memory and I/O controllers.

The interrupt acknowledgement ($\overline{INTA}$) command output is actually a dual function pin. As an output, its function is to provide the $\overline{INTA}$ command to the memory and I/O peripherals as decoded from the status inputs and latches. When CALL is used as an interrupt instruction, the SN74S428/SN74S428 generates the proper sequence of control signals. Additionally, the terminal includes high-threshold decoding logic that permits it to be biased through a one-kilohm series resistor to the 12-volt supply to implement an interrupt structure that automatically inserts an RST7 instruction on the bus when the DBIN input is active and an interrupt is acknowledged. This capability provides a single-level interrupt vector with minimal hardware.

The asynchronous bus enable ($\overline{BUSEN}$) input to the decoding array is a control signal that protects the system bus. The system bus can be accessed and driven from the SN74S428/SN74S428 controller only when the $\overline{BUSEN}$ input is at a low voltage level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	D0 thru D7			−10	μA
	All others			−1	mA
Low-level output current, I_{OL}	D0 thru D7			2	mA
	All others			10	
Status strobe pulse width, $t_{w(STSTB)}$ (see Figure 3)		22			ns
Setup time, t_{su} (see Figure 3)	Status inputs D0 thru D7	8			ns
	System bus inputs to HLDA	10			
Hold time, t_h (see Figure 3)	Status inputs D0 thru D7	5			ns
	System bus inputs to HLDA	20			
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	D0 thru D7	V_{CC} = MIN,	V_{IH} = 2 V,	3.6	4		V
		All other outputs	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.45	V
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 5.25 V			100	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.45 V			−100	μA
I_{IH}	High-level input current	$\overline{INTA}$	V_{CC} = MIN,	See Figure 1			5	mA
		D0 thru D7	V_{CC} = MAX,	V_I = 5.25 V			20	μA
		All other inputs					100	
I_{IL}	Low-level input current	D2 or D6	V_{CC} = MAX,	V_I = 0.45 V			−750	μA
		$\overline{STSTB}$					−500	
		All other inputs					−250	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−15		−90	mA
I_{CC}	Supply current		V_{CC} = MAX			140	190	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

7

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see figure 3

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	D0 thru D7	DB0 thru DB7	C_L = 100 pF,	See Figure 2	5		40	ns
t_{PD}	DB0 thru DB7	D0 thru D7	C_L = 25 pF,	See Figure 2			30	ns
t_{PHL}	$\overline{STSTB}$	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$, $\overline{I/OW}$, $\overline{MEMW}$	C_L = 100 pF,	See Figure 2	20		60	ns
t_{PD}	$\overline{WR}$	$\overline{I/OW}$, $\overline{MEMW}$			5		45	ns
t_{PLH}	DBIN	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					30	ns
t_{PLH}	HLDA	$\overline{INTA}$, $\overline{I/OR}$, $\overline{MEMR}$					25	ns
t_{PZX}	DBIN	D0 thru D7	C_L = 25 pF,	See Figure 2			45	ns
t_{PXZ}	DBIN	D0 thru D7					45	ns
t_{PZX}	$\overline{STSTB}$, $\overline{BUSEN}$	DB0 thru DB7	C_L = 100 pF,	See Figure 2			30	ns
t_{PXZ}	$\overline{BUSEN}$	DB0 thru DB7					30	ns

¶ t_{PD} ≡ propagation delay time
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PZX} ≡ output enable time from high-impedance state
t_{PXZ} ≡ output disable time to high-impedance state

PARAMETER MEASUREMENT INFORMATION

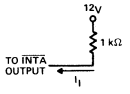


FIGURE 1—$\overline{\text{INTA}}$ INPUT CURRENT TEST CIRCUIT

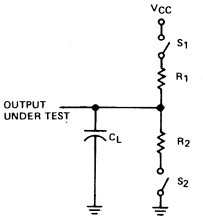
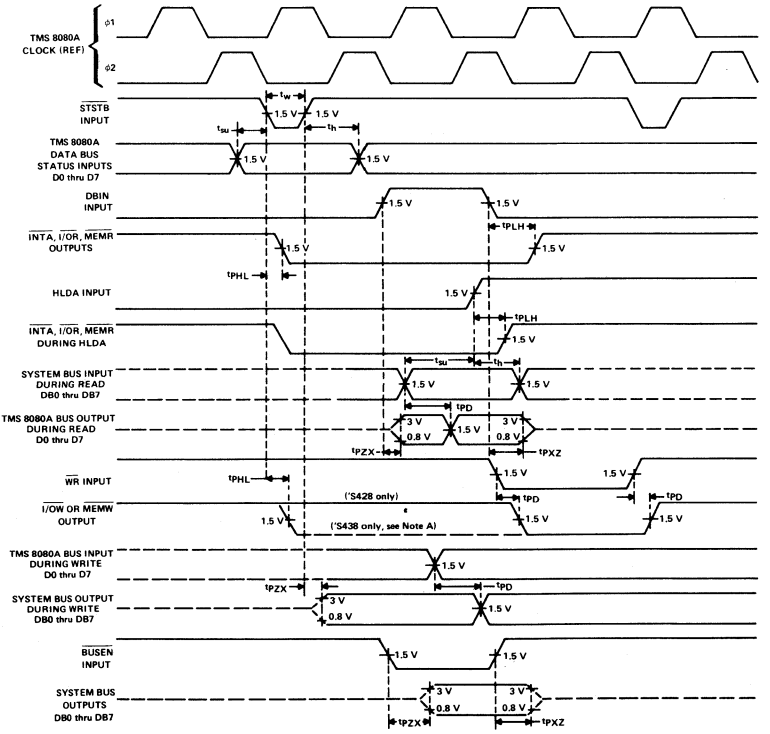


FIGURE 2—SWITCHING CHARACTERISTICS LOAD CIRCUIT



NOTE A: Advanced response of $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ for the SN74S438 is indicated by the dashed line.

FIGURE 3—VOLTAGE WAVEFORMS

TYPICAL APPLICATION DATA

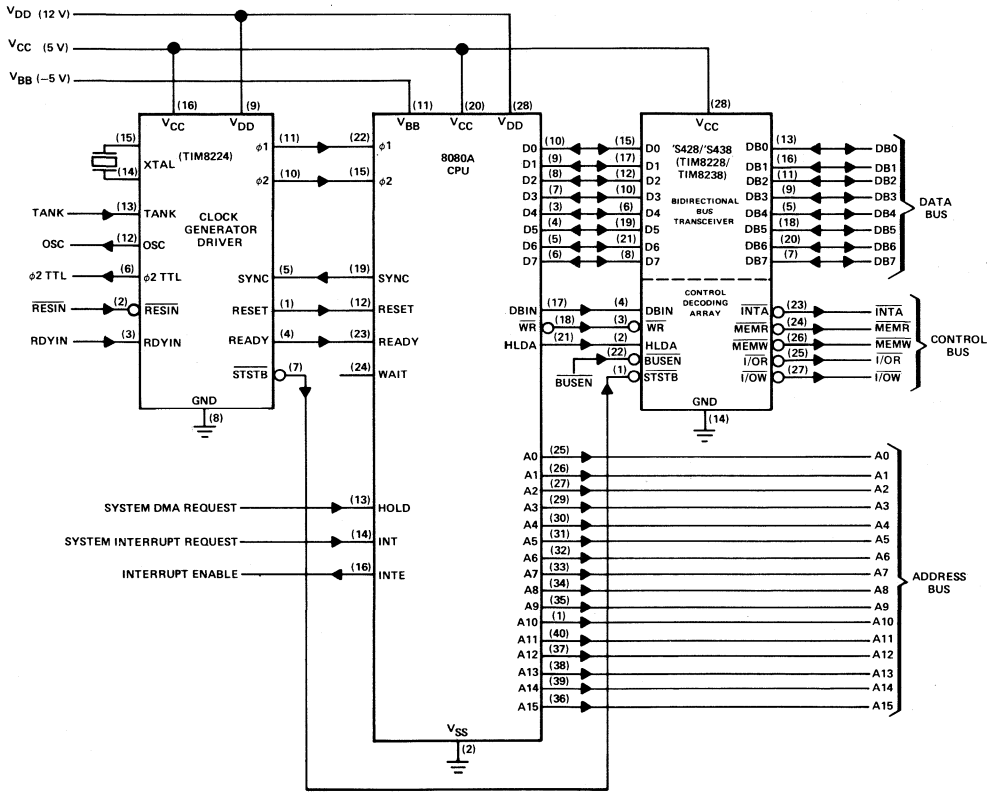


FIGURE 4—SYSTEM INTERFACING WITH CENTRAL PROCESSING UNIT

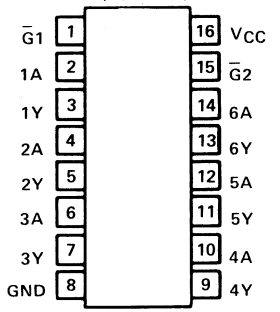
TYPES SN54S436, SN54S437, SN74S436, SN74S437
LINE DRIVER/MEMORY DRIVER CIRCUITS

D2630, JANUARY 1981

MOS MEMORY INTERFACE

- **Can Drive High-Impedance Loads**
- **Interchangeable with National DS16149/36149 DS16179/36179 Drivers**
- **High-Speed Switching**
- **Minimum Input Current Required**
- **Damping Output Resistor Reduces Transients**

SN54S436, SN54S437 . . . J OR W PACKAGE
SN74S436, SN74S437 . . . J OR N PACKAGE
(TOP VIEW)



description

The SN54S436, SN54S437, SN74S436 and SN74S437 are monolithic integrated TTL-to-MOS drivers and interface circuits. The devices accept standard TTL and DTL input signals. The p-n-p input transistors use minimum current allowing increased fan-out to these drivers. Schottky-clamped transistor logic permits high-speed operation, minimum propagation time.

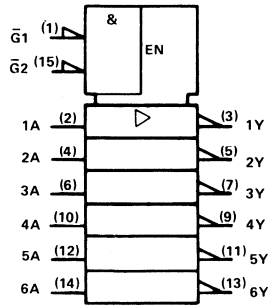
A small series damping resistor has been included in the design of the 'S436 to eliminate undesired output transient overshoot. Either enable, G, when high, sets the outputs to the high level for MOS RAM refresh applications.

FUNCTION TABLE

ENABLE INPUTS		INPUT	OUTPUT
$\overline{G}1$	$\overline{G}2$		
L	L	L	H
L	L	H	L
X	H	X	H
H	X	X	H

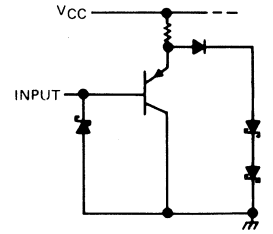
H = high level, L = low level, X = irrelevant

logic symbol

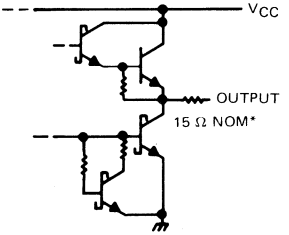


schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



*On SN54S436 and SN74S436 only

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range . . . . . −1.5 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)
J package . . . . . 1375 mW
N package . . . . . 1150 mW
W package . . . . . 1000 mW
Operating free-air temperature range: SN54S436, SN54S437 . . . . . −55°C to 125°C
SN74S436, SN74S437 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.
2: For operation above 25°C free-air temperature, derate as follows: J package, 11.0 mW/°C, N package, 9.2 mW/°C, W package, 8.0 mW/°C.

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54S'			SN74S'			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V, I_I = −18 mA			−0.75	−1.2		−0.75	−1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −10 μA		3.4	4.3		3.5	4.3		V
		V_{CC} = 4.5 V, I_{OH} = −1 mA	'S436	2.4	3.5		2.6	3.5		
			'S437	2.5	3.5		2.7	3.5		
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 10 μA			0.25	0.4		0.25	0.35	V
		V_{CC} = 4.5 V, I_{OL} = 20 mA	'S436		0.6	1.1		0.6	1	
			'S437		0.4	0.5		0.4	0.5	
I_{OL}	Low-level output current	V_{CC} = 4.5 V, V_I = 2 V,	V_O = 4.5 V, See Note 3		150			150		mA
I_{OS}	Short-circuit output current	V_{CC} = 4.5 V, See Note 3	V_O = 0 V,		−250			−250		mA
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_{IH} = 5.5 V		0.1	40		0.1	40	μA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_{IL} = 0.5 V		−50	−250		−50	−250	μA
I_{CC}	Supply current	V_{CC} = 5.5 V, All other inputs at 3 V	$\overline{G}$ inputs at 0 V,		33	60		33	60	mA
		V_{CC} = 5.5 V,	All inputs at 0 V		14	20		14	20	

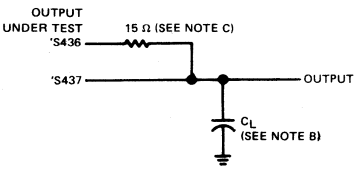
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: When measuring output current on the SN54S437/SN74S437, a 15-Ω resistor should be placed in series with each output.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

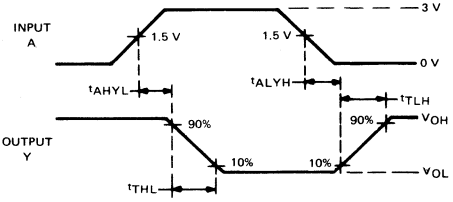
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{AHYL}	Delay time from A high to Y starting low	See Figure 1	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	
t_{ALYH}	Delay time from A low to Y starting high	See Figure 1	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	
t_{GHYH}	Delay time from $\overline{G}$ high to Y starting high	R_L = 2 kΩ to Gnd, See Figure 2	C_L = 50 pF,		10	18	ns
t_{GLYL}	Delay time from $\overline{G}$ low to Y starting low	R_L = 2 kΩ to V_{CC}, See Figure 3	C_L = 50 pF,		11	18	ns
t_{THL}	Transition time, high-to-low-level output	See Figure 1	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	
t_{TLH}	Transition time, low-to-high-level output	See Figure 1	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	

NOTE 3: When measuring switching times on the SN54S437/SN74S437, a 15-Ω resistor should be placed in series with each output.

PARAMETER MEASUREMENT INFORMATION

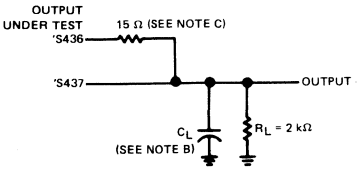


LOAD CIRCUIT

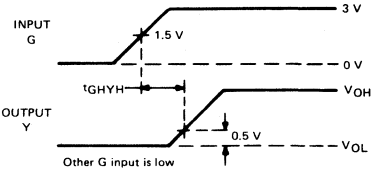


VOLTAGE WAVEFORMS

FIGURE 1

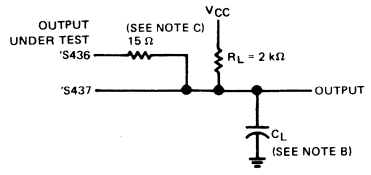


LOAD CIRCUIT

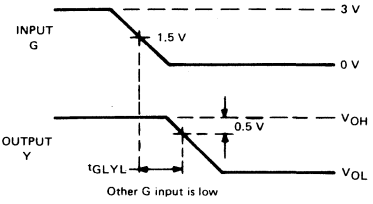


VOLTAGE WAVEFORMS

FIGURE 2



LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3

NOTES: A. Input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r ≤ 5 ns.
B. C_L includes probe and jig capacitance.
C. This 15-Ω resistor is required for testing the SN54S437/SN74S437, but it is internal to the SN54S436/SN74S436 and therefore an external resistor is not used for testing these devices.

TYPICAL APPLICATION DATA

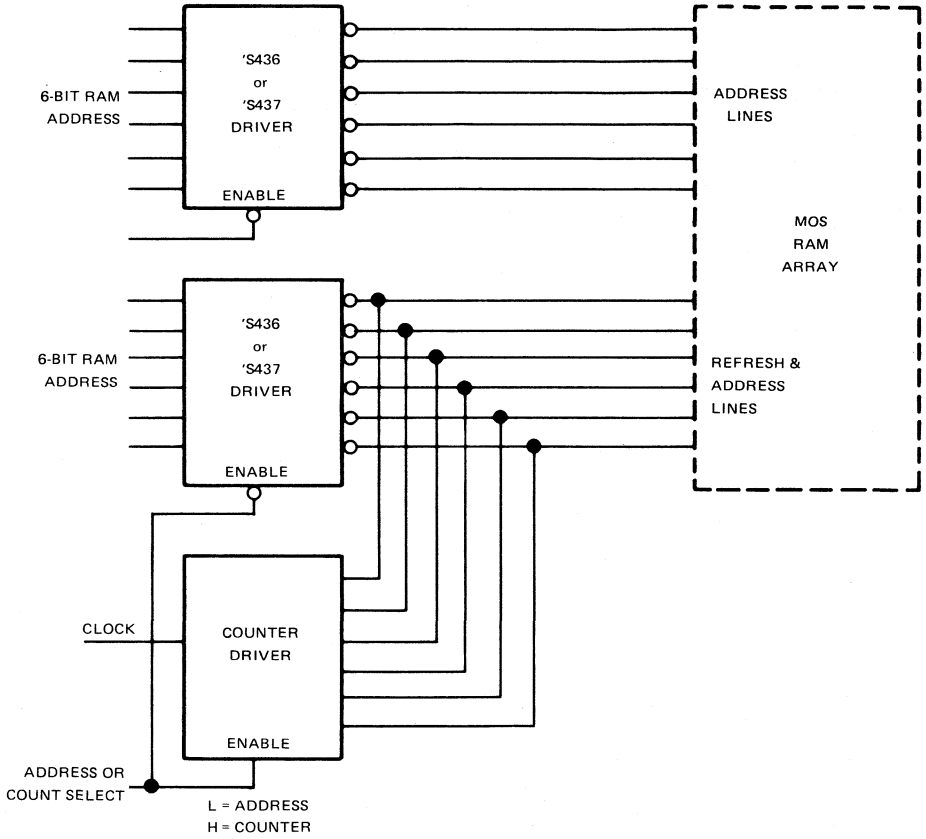


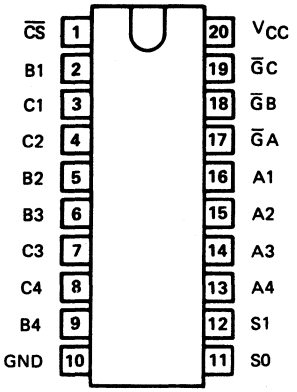
FIGURE 4

TYPES SN54LS440 THRU SN54LS444, SN54LS448, SN74LS440 THRU SN74LS444, SN74LS448 QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS

D2425, AUGUST 1979

- 3-Way Asynchronous Communication
- On-Chip Bus Selection Decoding
- Input Hysteresis Improves Noise Margin
- Choice of Open-Collector or 3-State Outputs

SN54LS' . . . . . J PACKAGE
SN74LS' . . . . . J OR N PACKAGE
(TOP VIEW)



description

These bus transceivers are designed for asynchronous three-way communication between four-line data buses. They give the designer a choice of selecting inverting, noninverting, or a combination of inverting and noninverting data paths with either 3-state or open-collector outputs.

The S0 and S1 inputs select the bus from which data are to be transferred. The $\overline{G}$ inputs enable the bus or buses to which data are to be transferred. The port for any bus selected for input and any other bus not enabled for output will be at high impedance including those of the open-collector devices.

The SN54LS440 through SN54LS444 and SN54LS448 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS440 through SN74LS444 and SN74LS448 are characterized for operation from 0°C to 70°C.

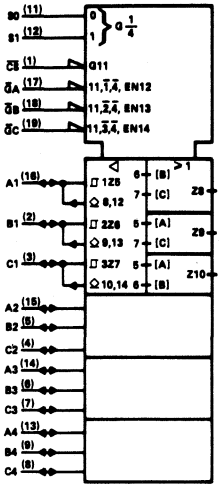
DEVICE	OUTPUT	LOGIC
'LS440	Open-Collector	True
'LS441	Open-Collector	Inverting
'LS442	3-State	True
'LS443	3-State	Inverting
'LS444	3-State	True/Inverting
'LS448	Open-Collector	True/Inverting

FUNCTION TABLE

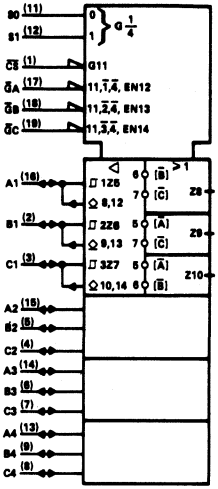
INPUTS						TRANSFERS BETWEEN BUSES		
$\overline{CS}$	S1	S0	$\overline{G}A$	$\overline{G}B$	$\overline{G}C$	'LS440 'LS442	'LS441 'LS443	'LS444 'LS448
H	X	X	X	X	X	None	None	None
X	H	H	X	X	X	None	None	None
X	X	X	H	H	H	None	None	None
X	L	L	X	H	H	None	None	None
X	L	H	H	X	H	None	None	None
X	H	L	H	H	X	None	None	None
L	L	L	X	L	L	A → B, A → C	$\overline{A}$ → B, $\overline{A}$ → C	$\overline{A}$ → B, $\overline{A}$ → C
L	L	H	L	X	L	B → C, B → A	$\overline{B}$ → C, $\overline{B}$ → A	B → C, $\overline{B}$ → A
L	H	L	L	L	X	C → A, C → B	$\overline{C}$ → A, $\overline{C}$ → B	$\overline{C}$ → A, C → B
L	L	L	X	L	H	A → B	$\overline{A}$ → B	$\overline{A}$ → B
L	L	H	H	X	L	B → C	$\overline{B}$ → C	B → C
L	H	L	L	H	X	C → A	$\overline{C}$ → A	$\overline{C}$ → A
L	L	L	X	H	L	A → C	$\overline{A}$ → C	$\overline{A}$ → C
L	L	H	L	X	H	B → A	$\overline{B}$ → A	$\overline{B}$ → A
L	H	L	H	L	X	C → B	$\overline{C}$ → B	C → B

logic symbols

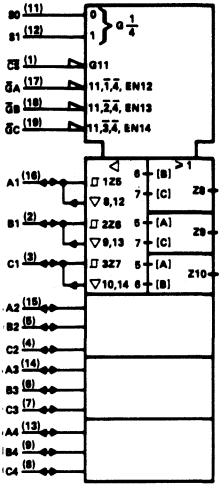
'LS440



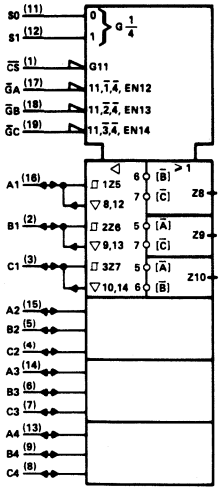
'LS441



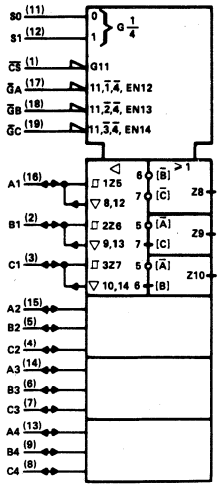
'LS442



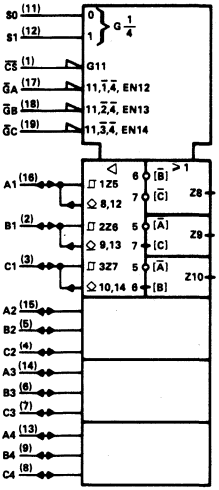
'LS443



'LS444

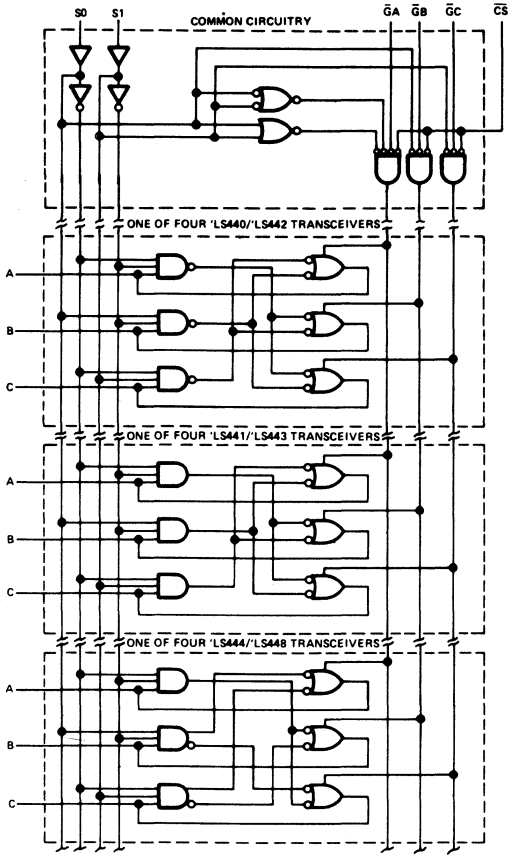


'LS448



7

functional block diagram (composite showing one of four transceivers from each type, positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS'	−55°C to 125°C
SN74LS'	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS440 SN54LS441 SN54LS448			SN74LS440 SN74LS441 SN74LS448			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL}max			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IL} = V_{IL}max	I_{OL} = 24 mA					0.35	0.5	V
I_I	Input current at maximum input voltage	A,B,C input	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	Outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs disabled				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, R_L = 667 Ω, C_L = 45 pF, T_A = 25°C, see Note 2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	'LS440			'LS441			'LS448			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A	B		24	35		21	30		21	30	ns
		A	C		24	35		21	30		21	30	
		B	A		24	35		21	30		21	30	
		B	C		24	35		21	30		24	35	
		C	A		24	35		21	30		21	30	
		C	B		24	35		21	30		24	35	
t_{PHL}	Propagation delay time, high-to-low level output	A	B		20	30		9	15		9	15	ns
		A	C		20	30		9	15		9	15	
		B	A		20	30		9	15		9	15	
		B	C		20	30		9	15		20	30	
		C	A		20	30		9	15		9	15	
		C	B		20	30		9	15		20	30	
t_{PLH}	Propagation delay time, low-to-high level output	any $\overline{G}$	A, B, C		29	45		23	35		25	40	ns
		S0, S1	A, B, C		33	50		27	40		26	40	
		$\overline{CS}$	A, B, C		31	45		26	40		25	40	
t_{PHL}	Propagation delay time, high-to-low level output	any $\overline{G}$	A, B, C		27	40		20	30		22	35	ns
		S0, S1	A, B, C		32	50		26	40		27	40	
		$\overline{CS}$	A, B, C		28	45		21	30		22	35	

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

recommended operating conditions

	SN54LS442 SN54LS443 SN54LS444			SN74LS442 SN74LS443 SN74LS444			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	A,B,C input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, $\overline{CS}$ at 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−400			−400	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs low	V_{CC} = MAX,	Outputs open		62	90		62	90	mA
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

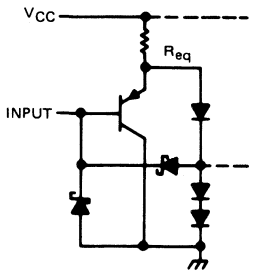
switching characteristics, V_{CC} = 5 V, T_A = 25°C, see Note 2

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS442			'LS443			'LS444			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	A	B	C_L = 45 pF, R_L = 667 Ω		10	14		9	14		9	14	ns
		A	C			10	14		9	14		9	14	
		B	A			10	14		9	14		9	14	
		B	C			10	14		9	14		10	14	
		C	A			10	14		9	14		9	14	
		C	B			10	14		9	14		10	14	
t_{PHL}	Propagation delay time, high-to-low level output	A	B			13	20		7	13		7	13	ns
		A	C			13	20		7	13		7	13	
		B	A			13	20		7	13		7	13	
		B	C			13	20		7	13		13	20	
		C	A			13	20		7	13		7	13	
		C	B			13	20		7	13		13	20	
t_{PZL}	Output enable time to low level	Any $\overline{G}$	A, B, C			22	33		22	33		22	33	ns
		S0 or S1	A, B, C			28	42		28	42		28	42	
		$\overline{CS}$	A, B, C			23	36		24	36		23	36	
t_{PZH}	Output enable time to high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			21	32		20	32		24	32	ns
t_{PLZ}	Output disable time from low level	$\overline{G}$, S, $\overline{CS}$	A, B, C	C_L = 5 pF, R_L = 667 Ω		14	25		15	25		14	25	ns
t_{PHZ}	Output disable time from high level	$\overline{G}$, S, $\overline{CS}$	A, B, C			14	25		15	25		14	25	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

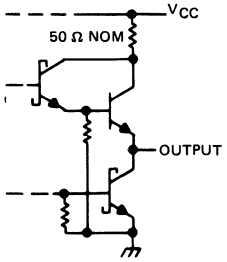
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

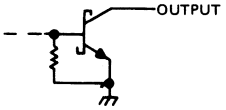


R_{eq}: $\overline{G}A$, $\overline{G}B$, $\overline{G}C$ = 9 kΩ NOM
All others = 5 kΩ NOM

TYPICAL OF 3-STATE OUTPUTS



TYPICAL OF OPEN-COLLECTOR OUTPUTS



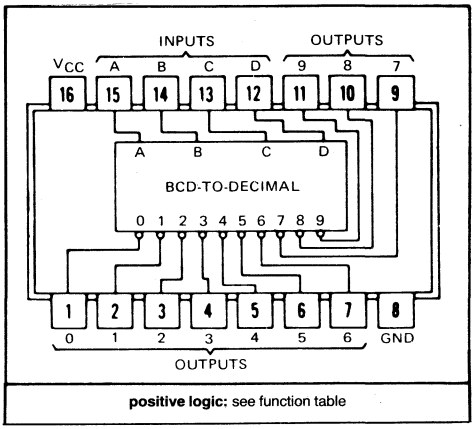
TYPES SN54LS445, SN74LS445
BCD-TO-DECIMAL DECODERS/DRIVERS

D2427, NOVEMBER 1977

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Low-Voltage Version of SN54LS145/ SN74LS145
- Full Decoding of Input Logic
- SN74LS445 Has 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation . . . 35 mW Typical

SN54LS445 . . . J OR W PACKAGE
SN74LS445 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

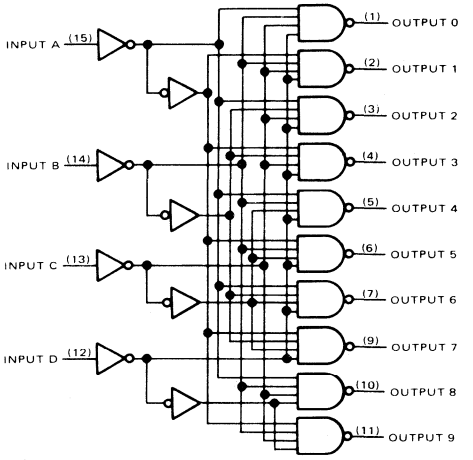
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monilithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/ relay drivers or as open-collector logic-circuit drivers. Each of the output transistors will sink up to 80 milliamperes of current. Each input is one Series 54LS/ 74LS standard load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 35 milliwatts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS445 . . . . . −55°C to 125°C
SN74LS445 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS445			SN74LS445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			7			7	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS445			SN74LS445			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
			I_{OL} = 80 mA					2.3	3	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		7	13		7	13	mA

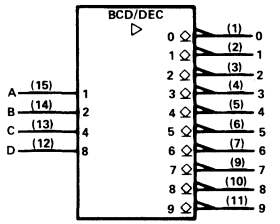
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

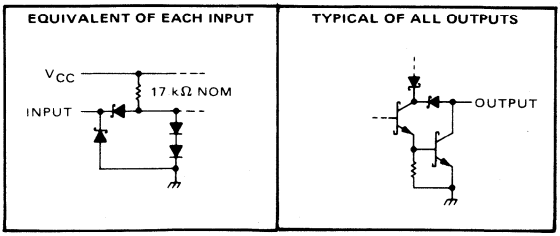
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 665 Ω, See Note 3		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			50	ns

NOTE 3: Load circuit and waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, second edition, LCC 4112.

logic symbol



schematic of inputs and outputs

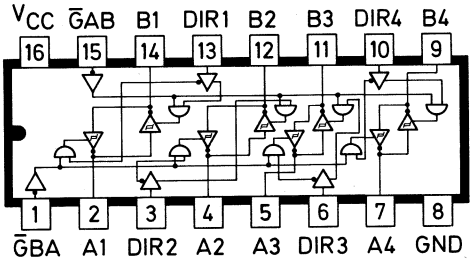


TYPES SN54LS446, SN54LS449, SN74LS446, SN74LS449
QUADRUPLE BUS TRANSCEIVERS WITH INDIVIDUAL DIRECTION CONTROLS

D2613, OCTOBER 1980

- 3-State Outputs Drive Bus Lines Directly
- P-N-P Inputs Reduce DC Loading on Bus Line
- Hysteresis at Bus Inputs Improves Noise Margins
- Flow-Thru Data Pinout (B Bus Opposite A Bus)
- Choice of True ('LS449) and Inverting ('LS446)

SN54LS . . . J PACKAGE
SN74LS' . . . J or N PACKAGE
(TOP VIEW)



description

These quadruple bus transceivers are designed for data transmission from individual lines of the A bus to individual lines of the B bus or the reverse, depending on the logic levels at the direction-control pins DIR1 through DIR4. These direction controls (one for each channel) allow maximum flexibility in timing. The enable inputs $\overline{G}BA$ and $\overline{G}AB$ can be used to disable the A or B outputs respectively, or to disable both buses for effective isolation.

The SN54LS446 and SN54LS449 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS446 and SN74LS449 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE $\overline{G}BA$	ENABLE $\overline{G}AB$	DIRECTION DIR	OPERATION 'LS446	OPERATION 'LS449
H	H	X	Isolation	Isolation
X	L	H	$\overline{A}$ data to B Bus	A data to B Bus
L	X	L	$\overline{B}$ data to A Bus	B data to A Bus
X	H	H	Isolation	Isolation
H	X	L	Isolation	Isolation

H = high level, L = low level, X = irrelevant

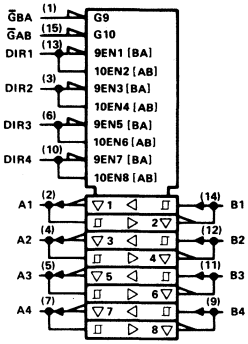
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

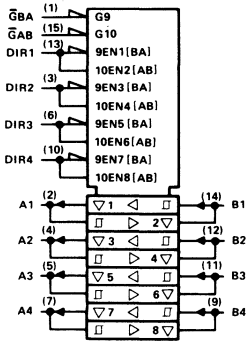
NOTE 1: Voltage values are with respect to the network ground terminal.

logic symbols†

'LS446



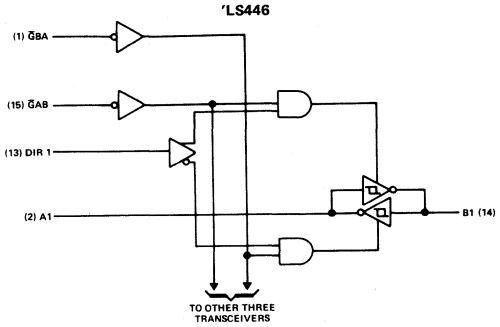
'LS449



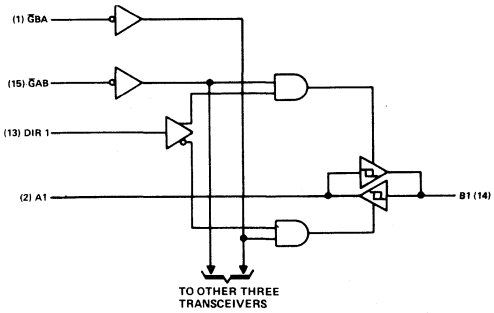
†These symbols are in accordance with IEEE Std 91/ANSI Y32 and current discussions IEC and IEEE.

functional block diagrams (positive logic)

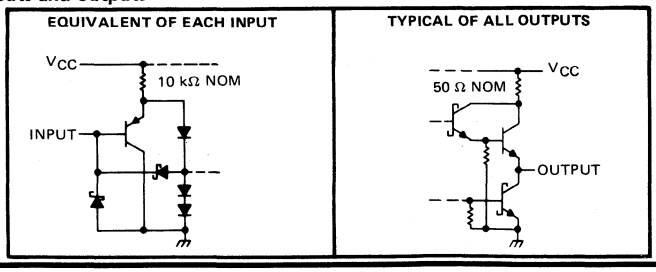
'LS446



'LS449



schematics of inputs and outputs



recommended operating conditions

PARAMETER	SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS446 SN54LS449			SN74LS446 SN74LS449			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.6			0.7	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$AB or $\overline{G}$BA		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS446	V_{CC} = MAX, Outputs open	Outputs high		35	56		35	56	mA
				Outputs low		39	63		39	63	
				Outputs at Hi-Z		42	68		42	68	
		'LS449		Outputs high		42	68		42	68	
				Outputs low		47	75		47	75	
				Outputs at Hi-Z		50	80		50	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS446			'LS449			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		8	13		10	15	ns
		B	A			8	13		10	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			7	12		11	17	ns
		B	A			7	12		11	17	
t_{PZL}	Output enable time to low level	$\overline{G}$BA	A			24	40		21	35	ns
		$\overline{G}$AB	B			24	40		21	35	
t_{PZH}	Output enable time to high level	$\overline{G}$BA	A			15	25		18	30	ns
		$\overline{G}$AB	B			15	25		18	30	
t_{PLZ}	Output disable time from low level	$\overline{G}$BA	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		14	25		14	25	ns
		$\overline{G}$AB	B			14	25		14	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$BA	A			10	15		10	15	ns
		$\overline{G}$AB	B			10	15		10	15	

NOTE 2: For load circuits and voltage waveforms, see page 3-10

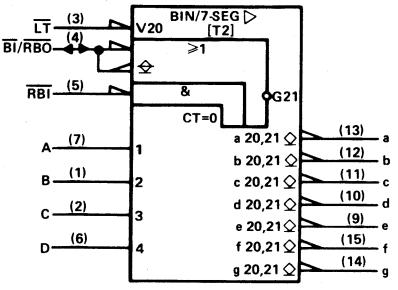
7

TYPES SN54LS447, SN74LS447
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

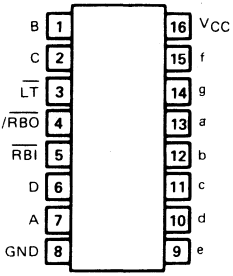
D2428, NOVEMBER 1977

- Low-Voltage Version of SN54LS247/SN74LS247
- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression
- Lamp Intensity Modulation Capability

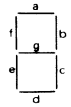
logic symbol



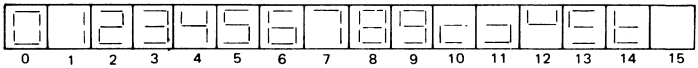
(TOP VIEW)



TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION	PACKAGES
	ACTIVE LEVEL	OUTPUT CONFIGURATION	SINK CURRENT	MAX VOLTAGE		
SN54LS247	low	open-collector	12 mA	7 V	35 mW	J, W
SN74LS247	low	open-collector	24 mA	7 V	35 mW	J, N



SEGMENT IDENTIFICATION



FONT TABLE T2 – NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Peak output current ($t_w \leq 1$ ms, duty cycle $\leq 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54LS447 . . . . . −55°C to 125°C
SN74LS447 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS447			SN74LS447			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			7			7	V
On-state output current, $I_{O(on)}$	a thru g			12			24	mA
High-level output current, I_{OH}	BI/RBO			−50			−50	μA
Low-level output current, I_{OL}	BI/RBO			1.6			3.2	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS447			SN74LS447			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −50 μA	2.4	4.2		2.4	4.2		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 1.6 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 3.2 mA					0.35	0.5	
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, $V_{O(off)}$ = 7 V			250			250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max	$I_{O(on)}$ = 12 mA		0.25	0.4		0.25	0.4	V
				$I_{O(on)}$ = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		BI/RBO					−1.2			−1.2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX		−0.3		−2	−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 665 Ω, See Note 4			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers*, Second Edition, LCC4112; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

TYPES SN54LS465 THRU SN54LS468, SN74LS465 THRU SN74LS468
OCTAL BUFFERS WITH 3-STATE OUTPUTS

D2631, JANUARY 1981

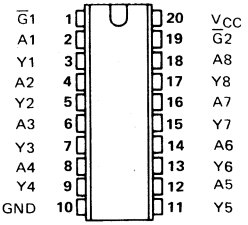
- **Mechanically and Functionally Interchangeable With DM71/81LS95 thru DM71/81LS98**
- **P-N-P Inputs Reduce Bus Loading**
- **3-State Outputs Rated at I_{OL} of 12 mA and 24 mA for 54LS and 74LS, Respectively**

DEVICE	DATA PATH
'LS465	True
'LS466	Inverting
'LS467	True
'LS468	Inverting

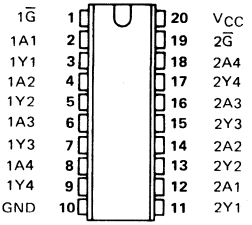
description

These octal buffers utilize the latest low-power Schottky technology. The 'LS465 and 'LS466 have a two-input active-low AND enable gate controlling all eight data buffers. The 'LS467 and 'LS468 have two separate active-low enable inputs each controlling four data buffers. In either case, a high level on any $\overline{G}$ places the affected outputs at high impedance.

SN54LS465 AND SN54LS466 . . J PACKAGE
SN74LS465 AND SN74LS466 . . J OR N PACKAGE
(TOP VIEW)

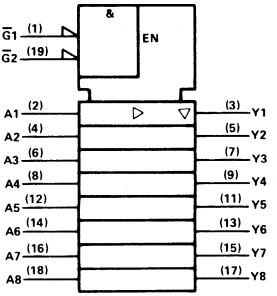


SN54LS467 AND SN54LS468 . . J PACKAGE
SN74LS467 AND SN74LS468 . . J OR N PACKAGE
(TOP VIEW)

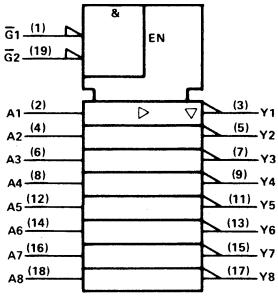


logic symbols

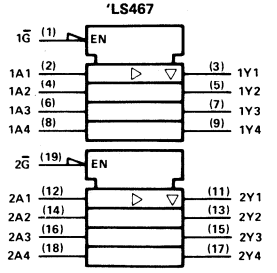
'LS465



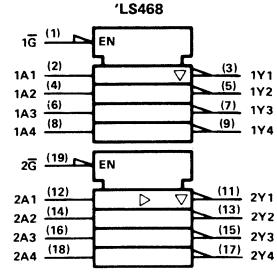
'LS466



'LS467



'LS468



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS465 thru SN54LS468 . . . . . −55°C to 125°C
SN74LS465 thru SN74LS468 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	3.3					V
				I_{OH} = −2.6 mA				2.4	3.1		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
I_{CC}	Supply current	'LS465, 'LS467	V_{CC} = MAX	Outputs low		14			19	32	mA
				Outputs high		7			13	22	
				Output Hi-Z		17			22	37	
		'LS466, 'LS468		Outputs low		10			14	23	
				Outputs high		4			6	10	
				Outputs Hi-Z		13			17	28	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

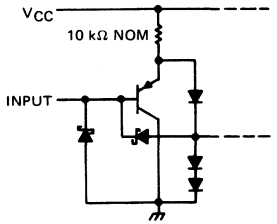
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS465, 'LS467			'LS466, 'LS468			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Ai	Yi	R_L = 667 Ω, C_L = 45 pF		9	15		7	12	ns
t_{PHL}	Ai	Yi			12	18		9	15	ns
t_{PZH}	$\overline{G}\downarrow$	Y			25	40		25	40	ns
t_{PZL}	$\overline{G}\downarrow$	Y			29	45		29	45	ns
t_{PHZ}	$\overline{G}\uparrow$	Y	R_L = 667 Ω, C_L = 5 pF		25	40		25	40	ns
t_{PLZ}	$\overline{G}\uparrow$	Y			30	45		30	45	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

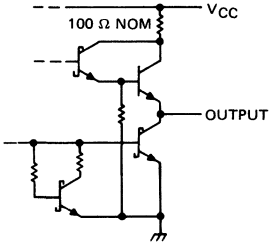
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS

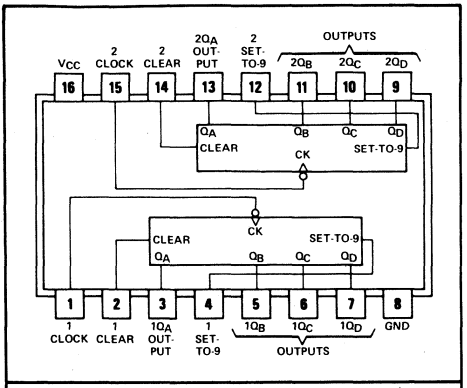


TYPES SN54490, SN54LS490, SN74490, SN74LS490
DUAL 4-BIT DECADE COUNTERS

BULLETIN NO. DL-S 7612089, OCTOBER 1976

- Dual Versions of Popular SN5490A, SN54LS90, SN7490A, and SN74LS90 Counters
- Individual Clock, Direct Clear, and Set-to-9 Inputs for Each Decade Counter
- Dual Counters Can Significantly Improve System Densities as Package Count Can Be Reduced by 50%
- Maximum Count Frequency . . . 35 MHz Typical
- Buffered Outputs Reduce Possibility of Collector Commutation

SN54490 . . . J OR W PACKAGE
SN74490 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low; high input to set-to-9 sets Q_A and Q_D high, Q_B and Q_C low.

description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual 4-bit decade counters in a single package. Each decade counter has individual clock, clear, and set-to-9 inputs. BCD count sequences of any length up to divide-by-100 may be implemented with a single '490 or 'LS490. Buffering on each output is provided to ensure that susceptibility to collector cummutation is reduced significantly. All inputs are diode-clamped to reduce the effects of line ringing. The counters have parallel outputs from each counter stage so that submultiples of the input count frequency are available for system timing signals.

The SN54490 and SN54LS490 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74490 and SN74LS490 are characterized for use in industrial systems operating from 0°C to 70°C.

BCD COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

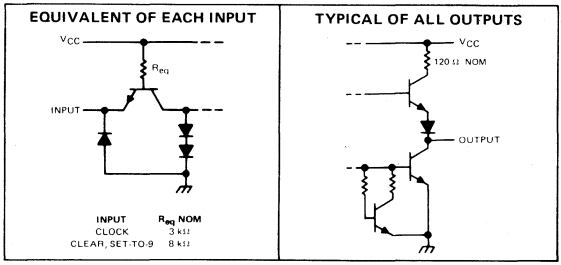
CLEAR/SET-TO-9
FUNCTION TABLE
(EACH COUNTER)

INPUTS		OUTPUTS			
CLEAR	SET-TO-9	Q_A	Q_B	Q_C	Q_D
H	L	L	L	L	L
L	H	H	L	L	H
L	L	COUNT			

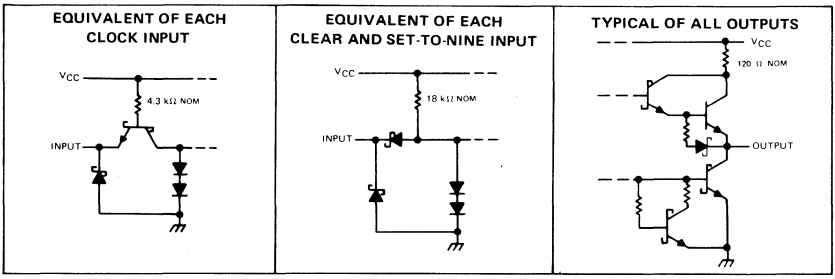
H = high level, L = low level

schematics of inputs and outputs

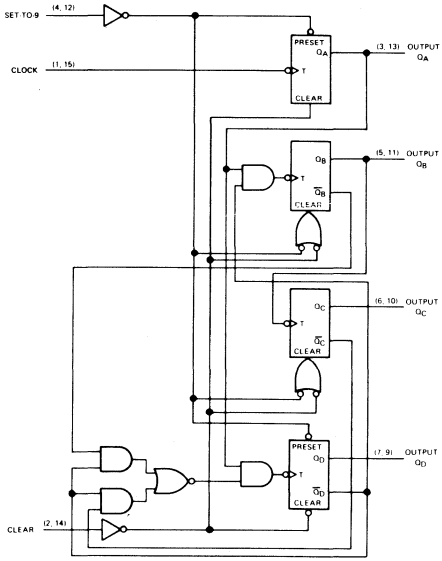
'490



'LS490



functional block diagram (each counter)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54490 . . . . . −55°C to 125°C
SN74490 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54490			SN74490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Count frequency, f_{count}	0		25	0		25	MHz
Pulse width, t_w (any input)		20			20		ns
Clear or set-to-9 inactive-state setup time, t_{su}	25↓			25↓			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

7

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Clear, set-to-9	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Clock					80	
I_{IL}	Low-level input current	Clear, set-to-9	V_{CC} = MAX, V_I = 0.4 V				−1	mA
		Clock					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54490	−20		−57	mA
				SN74490	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			45	70	mA

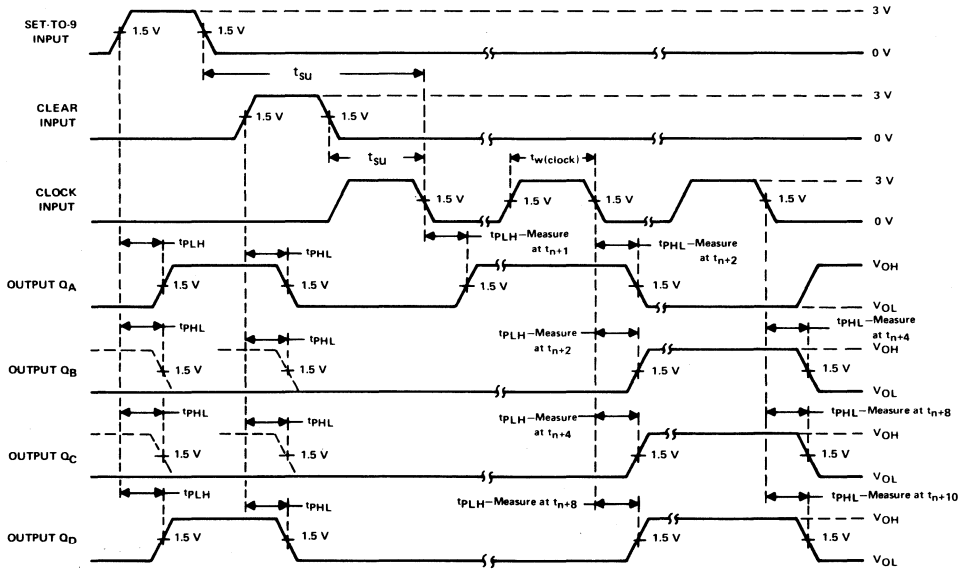
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Clock	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Note 3	25	35		MHz
t_{PLH}	Clock	Q_A			12	20	ns
t_{PHL}					13	20	
t_{PLH}	Clock	Q_B, Q_D			24	39	ns
t_{PHL}					26	39	
t_{PLH}	Clock	Q_C			32	54	ns
t_{PHL}					36	54	
t_{PHL}	Clear	Any			24	39	ns
t_{PLH}	Set-to-9	Q_A, Q_D			24	39	ns
t_{PHL}		Q_B, Q_C			20	36	

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 3: Load circuit is shown on page 3-10.



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

FIGURE 1

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Clear and set-to-9 input voltage . . . . . 7 V
Clock input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS490 . . . . . −55°C to 125°C
SN74LS490 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS490			SN74LS490			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Pulse width, t_w (any input)	20			20			ns
Clear or set-to-9 inactive-state setup time, t_{su}	25↓			25↓			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS490			SN74LS490			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2 V,	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Clear, set-to-9	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Clock		V_I = 5.5 V			0.2			0.2	
I_{IH}	High-level input current	Clear, set-to-9	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Clock					100			100	
I_{IL}	Low-level input current	Clear, set-to-9	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Clock					−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		15	26		15	26	mA

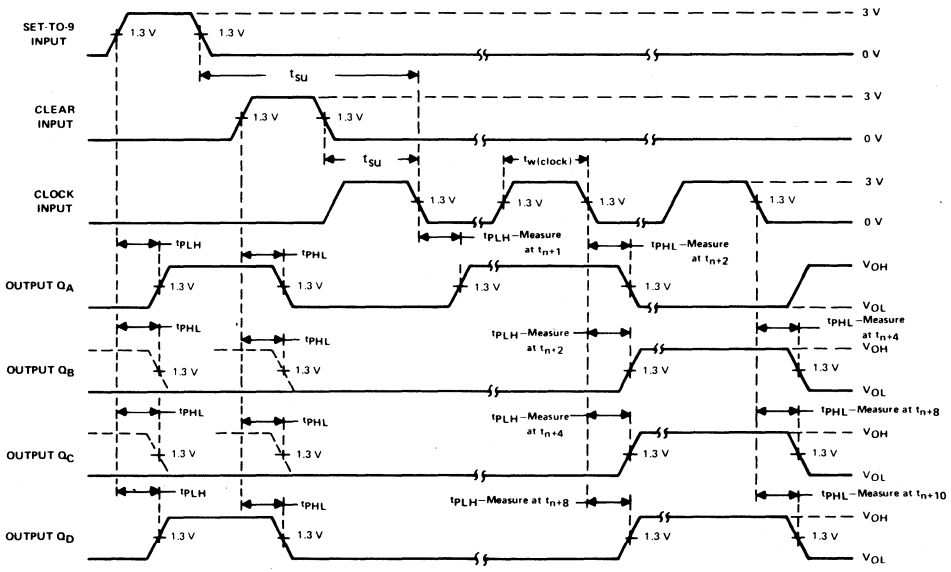
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Clock	Q_A	C_L = 15 pF, R_L = 2 kΩ See Figure 2 and Note 4	25	35		MHz
t_{PLH}	Clock	Q_A			12	20	ns
t_{PHL}					13	20	
t_{PLH}	Clock	Q_B, Q_D			24	39	ns
t_{PHL}					26	39	
t_{PLH}	Clock	Q_C			32	54	ns
t_{PHL}					36	54	
t_{PHL}	Clear	Any			24	39	ns
t_{PLH}	Set-to-9	Q_A, Q_D			24	39	ns
t_{PHL}		Q_B, Q_C			20	36	

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuit is shown on page 3-11.



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

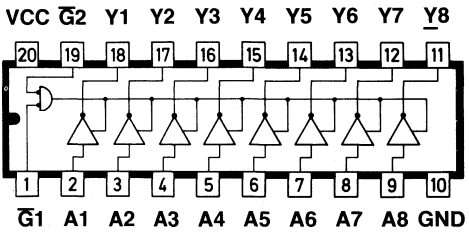
FIGURE 2

TYPES SN54LS540, SN54LS541, SN74LS540, SN74LS541 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

D2546, AUGUST 1979 – REVISED JUNE 1980

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins
- Data Flow-thru Pinout (All Inputs on Opposite Side from Outputs)

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54LS240/SN74LS240 series and, at the same time, offer a pinout having the inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

The three-state control gate is a 2-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

The 'LS540 offers inverting data and the 'LS541 offers true data at the outputs.

The SN54LS540 and SN54LS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS540 and SN74LS541 are characterized for operation from 0°C to 70°C.

TYPE	RATED I_{OL} (SINK CURRENT)	RATED I_{OH} (SOURCE CURRENT)	TYPICAL POWER DISSIPATION (ENABLED) 'LS540	'LS541
SN54LS'	12 mA	−12 mA	92.5 mW	120 mW
SN74LS'	24 mA	−15 mA	92.5 mW	120 mW

7

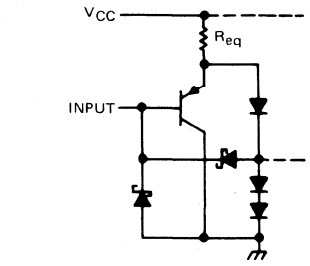
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS540, SN54LS541 . . . . . −55°C to 125°C
SN74LS540, SN74LS541 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

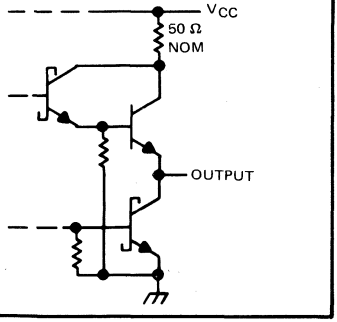
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



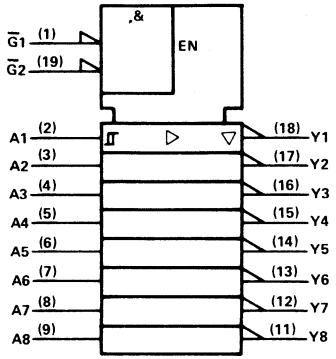
Enable Inputs: R_{eq} = 9 kΩ NOM
All Other Inputs: R_{eq} = 10 kΩ NOM

TYPICAL OF ALL OUTPUTS

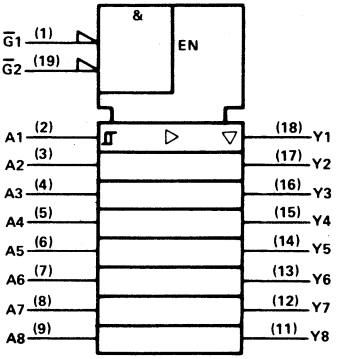


logic symbols

'LS540

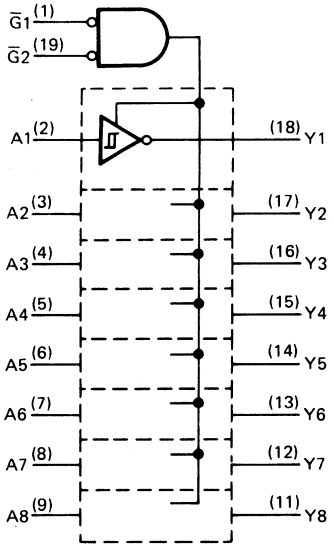


'LS541

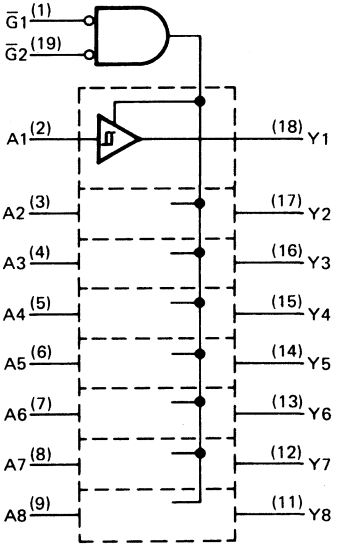


functional block diagram (positive logic)

'LS540



'LS541



recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5 V,	V_{IH} = 2 V, I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current♦	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current, Outputs high	V_{CC} = MAX, Outputs open	'LS540		13	25		13	25	mA
			'LS541		18	32		18	32	
	Outputs low		'LS540		24	45		24	45	
			'LS541		30	52		30	52	
	All outputs disabled		'LS540		30	52		30	52	
			'LS541		32	55		32	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'LS540			'LS541			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, See Note 2	R_L = 667 Ω,		9	15		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output				9	15		10	18	ns
t_{PZL}	Output enable time to low level				25	38		25	38	ns
t_{PZH}	Output enable time to high level				15	25		20	32	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, See Note 2	R_L = 667 Ω,		15	25		18	29	ns
t_{PHZ}	Output disable time from high level				10	18		10	18	ns

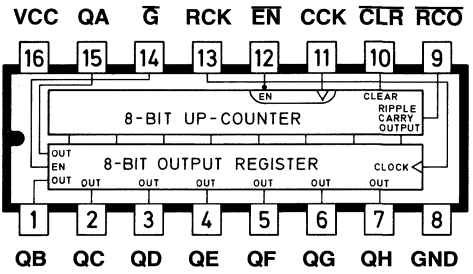
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11

TYPES SN54LS590, SN54LS591, SN74LS590, SN74LS591
8-BIT BINARY COUNTERS WITH OUTPUT REGISTERS

D2632, JANUARY 1981

- 8-Bit Counter with Register
- Parallel Register Outputs
- Counter has Direct Clear
- Choice of 3-State ('LS590) or Open-Collector ('LS591) Register Outputs
- Guaranteed Counter Frequency . . . . DC to 20 MHz

SN54LS590, SN54LS591 . . J OR W PACKAGE
SN74LS590, SN74LS591 . . J OR N PACKAGE
(TOP VIEW)

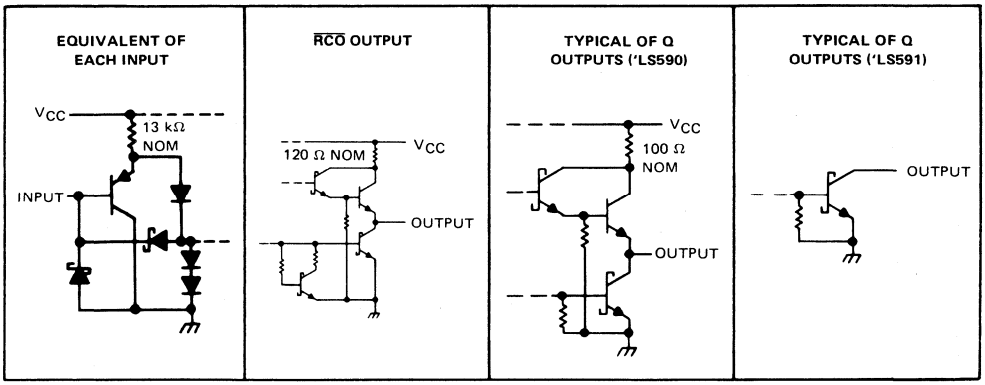


description

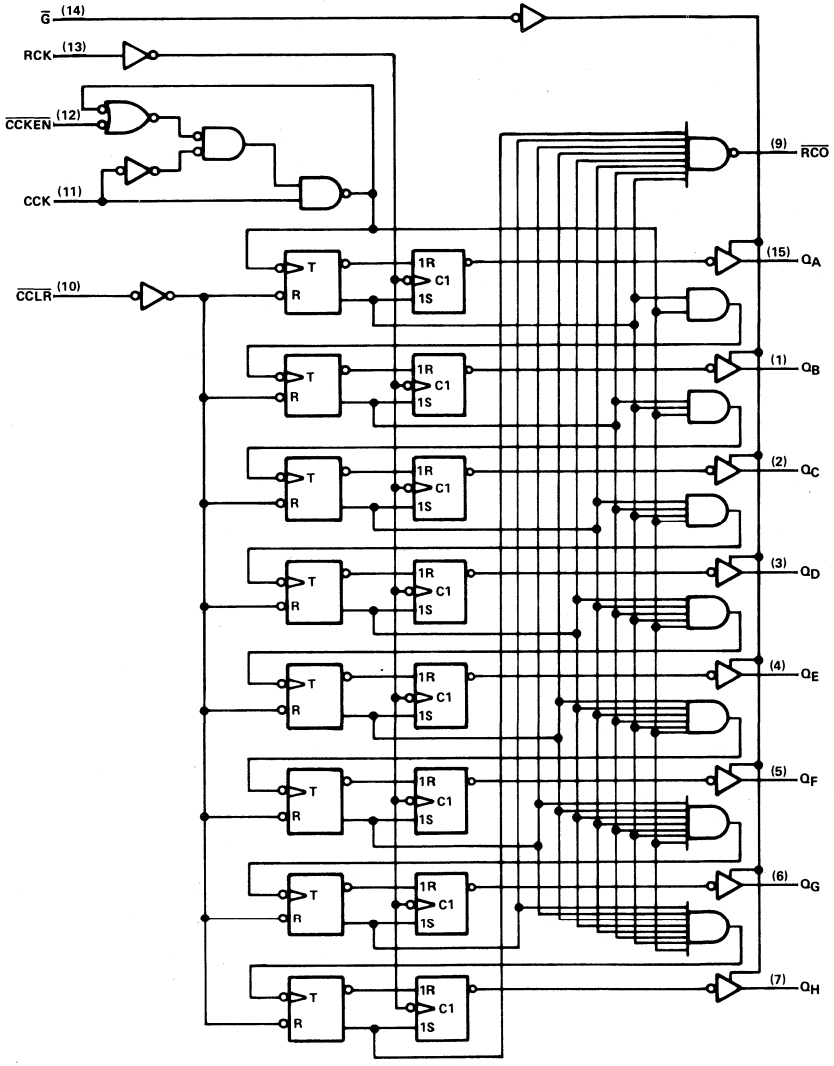
These devices contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output $\overline{RCO}$ is provided. Expansion is easily accomplished by tying $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

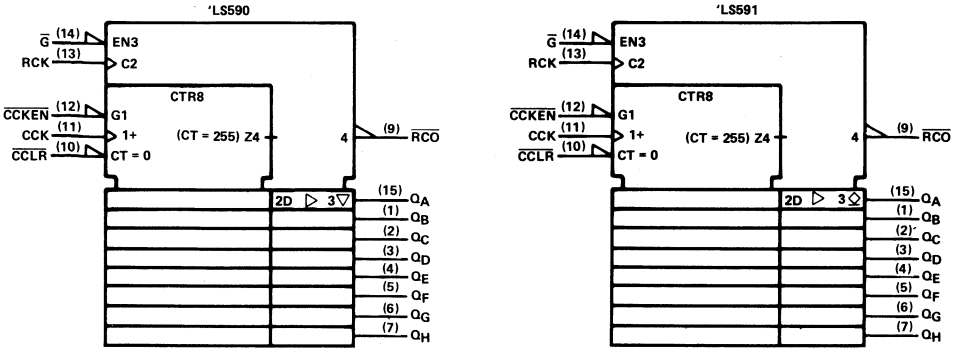
schematics of inputs and outputs



functional block diagram (positive logic)



logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS590, SN54LS591 . . . . . −55°C to 125°C
SN74LS590, SN74LS591 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q, 'LS591 only			5.5			5.5	V
High-level output current, I_{OH}	$\overline{RCO}$			−0.4			−1	mA
	Q, 'LS590 only			−1			−2.6	mA
Low-level output current, I_{OL}	$\overline{RCO}$			8			16	mA
	Q			12			24	
Counter clock frequency, f_{CCK}		0		20	0		20	MHz
Width of counter clock pulse, $t_{w(CCK)}$		25			25			ns
Width of counter clear pulse, $t_{w(CCLR)}$		20			20			ns
Width of register clock pulse, $t_{w(RCK)}$		20			20			ns
Count enable time, t_{enable}	$\overline{CCKEN}$↓ to CCK↑	20			20			ns
Clear inactive-state setup time, t_{su}	$\overline{CCLR}$↑ to CCK↑	20			20			ns
Setup time, t_{su} (see Note 1)	CCK↑ to RCK↑	40			40			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP*	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP*	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I =−18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS590 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.4	3.2					V
		$\overline{RCO}$		I_{OH} = −2.6 mA				2.4	3.1		
				I_{OH} = −1 mA				2.4	3.2		
I_{OH}	High-level output current	'LS591 Q	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	V_{OH} = 5.5 V,			100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC}=MIN, V_{IH}=2V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS590	V_{CC}=MAX, V_{IH}=2V, V_{IL}=V_{IL}max	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS590 Q	V_{CC}=MAX, V_{IH}=2V, V_{IL}=V_{IL}max	V_O =0.4V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=5.5V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	CCK			−0.8			−0.8	mA
			V_I = 0.4 V	Others			−0.2			−0.2	
I_{OS}	Short-circuit output current§	$\overline{RCO}$ Q	V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$ 'LS590	only		−20		−100	−20		−100	
I_{CC}	Supply current	'LS590	ICCH	V_{CC} = MAX, All possible inputs grounded, All outputs open		33	56		33	56	mA
			ICCL			44	65		44	65	
			ICCZ			46	65		46	65	
		'LS591	ICCH			35	55		35	55	
			ICCL			42	65		42	65	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

* All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS590 MIN	'LS590 TYP	'LS590 MAX	'LS591 MIN	'LS591 TYP	'LS591 MAX	UNIT
f_{max}	CCK	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	20	35		20	35		ns
t_{PLH}	CCK↑	$\overline{RCO}$			14	22		16	24	ns
t_{PHL}	CCK↑	$\overline{RCO}$				30		25	38	ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$			30	45		32	48	ns
t_{PLH}	RCK↑	Q	R_L = 667 kΩ, C_L = 45 pF		12	18		25	38	ns
t_{PHL}	RCK↑	Q			22	33		28	42	ns
t_{PZH}	$\overline{G}$↓	Q			25	38				ns
t_{PZL}	$\overline{G}$↓	Q			30	45				ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 kΩ, C_L = 5 pF		20	30				ns
t_{PLZ}	$\overline{G}$↑	Q			25	38				ns
t_{PLH}	$\overline{G}$↑	Q	R_L = 667 kΩ, C_L = 45 pF					34	50	ns
t_{PHL}	$\overline{G}$↓	Q						32	48	ns

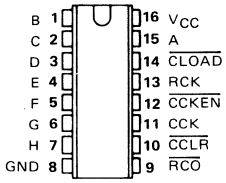
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

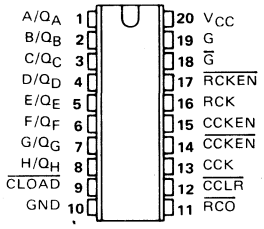
D2633, JANUARY 1984

- Parallel Register Inputs ('LS592)
- Parallel 3-State I/O: Register Inputs/Counter Outputs ('LS593)
- Counter has Direct Overriding Load and Clear
- Guaranteed Counter Frequency . . . DC to 20 MHz

SN54LS592 . . J OR W PACKAGE
SN74LS592 . . J OR N PACKAGE
(TOP VIEW)



SN54LS593 . . J PACKAGE
SN74LS593 . . J OR N PACKAGE
(TOP VIEW)



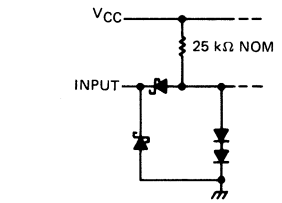
description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

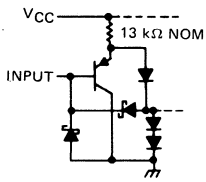
The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs.

schematics of inputs and outputs

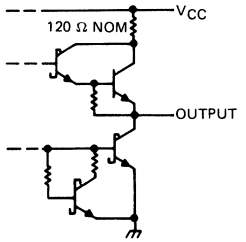
EQUIVALENT OF A THRU H INPUTS



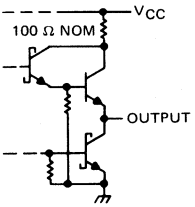
EQUIVALENT OF ALL OTHER INPUTS



$\overline{RCO}$ OUTPUT

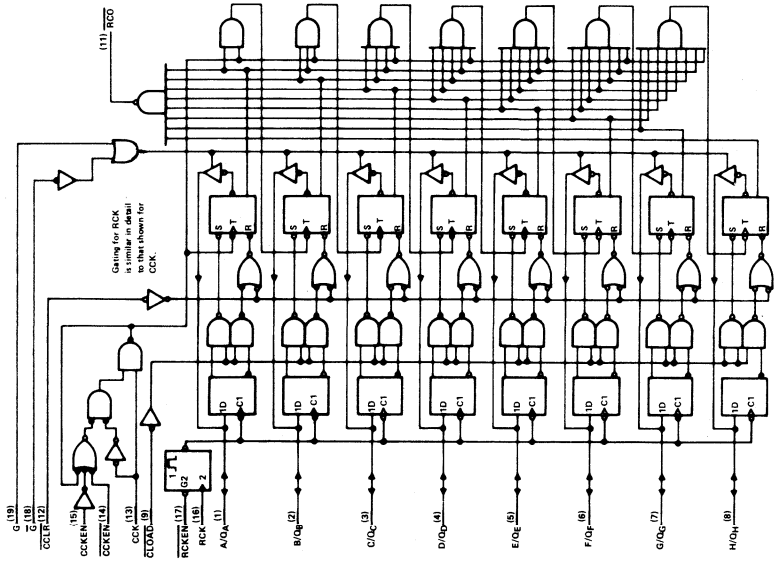


TYPICAL OF Q OUTPUTS
('LS593 ONLY)

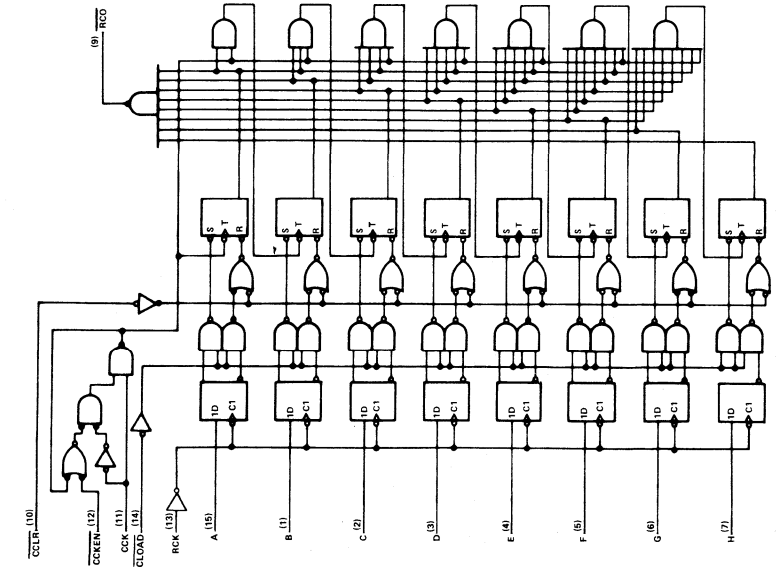


functional block diagrams (positive logic)

'LS593



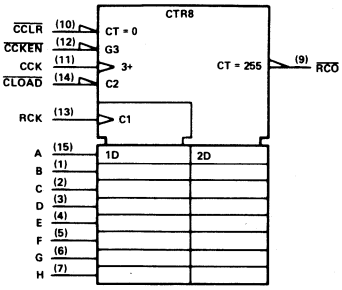
'LS592



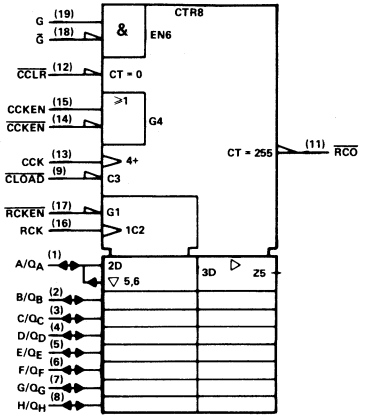
TYPES SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

logic symbols

'LS592



'LS593



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (excluding I/O ports) . . . . . 7 V
Off-state output voltage (including I/O ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593 . . . . . −55°C to 125°C
SN74LS592, SN74LS593 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	$\overline{RCO}$			−0.4			−1	mA
	Q 'LS593 only			−1			−2.6	mA
Low-level output current, I_{OL}	$\overline{RCO}$			8			16	mA
	Q 'LS593 only			12			24	
Counter clock frequency, f_{CCK}		0		20	0		20	MHz
Width of counter clock pulse, t_{wCCK}		25			25			ns
Width of counter clear pulse, $t_{w\overline{CCLR}}$		20			20			ns
Width of register clock pulse, t_{wRCK}		20			20			ns
Width of counter load pulse, $t_{w\overline{CLOAD}}$		20			20			ns
Count enable time, t_{enable}	$\overline{CCKEN}\downarrow$ to CCK↑, CCKEN↑ to CCK↑	20			20			ns
Register enable time, t_{enable}	$\overline{RCKEN}\downarrow$ to RCK↑ 'LS593 only	20			20			ns
Setup time, t_{su} (see note 2)	$\overline{CCLR}$↑ to CCK↑, $\overline{CLOAD}$↑ to CCK↑	20			20			ns
	RCK↑ to $\overline{CLOAD}$↑	30			30			
	Data A thru H to RCK↑	20			20			
Hold time, t_h	Data A thru H to RCK↑	0			0			ns
	All others	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: The RCK↑ to CLOAD↑ setup time insures data saved by RCK↑ will also be loaded into the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
						MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage			V_{CC}=MIN, I_I =−18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS593 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.4	3.2					V
		$\overline{RCO}$			I_{OH} = −2.6 mA				2.4	3.1		
					I_{OH} = −1 mA	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	'LS593 Q		V_{CC}=MIN, V_{IH}=2V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
					I_{OL} = 24 mA					0.35	0.5	
		$\overline{RCO}$			I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
					I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS593 Q		V_{CC}=MAX, V_{IH}=2V, V_{IL}=V_{IL}max	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS593 Q		V_{CC}=MAX, V_{IH}=2V, V_{IL}=V_{IL}max	V_O =0.4V			−200			−200	μA
I_I	Input current at maximum input voltage	'LS593 Q		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		Others			V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current			V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	Low-level input current			V_{CC} = MAX, V_I = 0.4 V	CCK			−0.8			−0.8	mA
					A thru H			−0.4			−0.4	
					Others			−0.2			−0.2	
I_{OS}	Short-circuit output current§	'LS593 Q		V_{CC} = MAX, V_O = 0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$				−20		−100	−20		−100	
I_{CC}	Supply current	'LS592	ICCH	V_{CC} = MAX, All possible inputs grounded, All outputs open			40	60		40	60	mA
			ICCL				40	60		40	60	
		'LS593	ICCH				47	70		47	70	
			ICCL				53	80		53	80	
			ICCZ				57	85		57	85	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS592			'LS593			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	Q	R_L = 667 kΩ, C_L = 45 pF					14	21	ns
t_{PHL}	CCK↑	Q						26	39	ns
t_{PLH}	$\overline{CLOAD}$↓	Q						34	51	ns
t_{PHL}	$\overline{CLOAD}$↓	Q						28	42	ns
t_{PHL}	$\overline{CCLR}$↓	Q						25	38	ns
t_{PZH}	G↑	Q						31	47	ns
t_{PZL}	G↑	Q						27	40	ns
t_{PZH}	$\overline{G}$↓	Q						29	45	ns
t_{PZL}	$\overline{G}$↓	Q						31	47	ns
t_{PHZ}	G↓	Q	R_L = 667 Ω, C_L = 5 pF					33	50	ns
t_{PLZ}	G↓	Q						35	52	ns
t_{PHZ}	$\overline{G}$↑	Q						26	39	ns
t_{PLZ}	$\overline{G}$↑	Q						28	42	ns
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF		15	23		14	21	ns
t_{PHL}	CCK↑	$\overline{RCO}$			20	30		20	30	ns
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$			–31	47		31	47	ns
t_{PHL}	$\overline{CLOAD}$↓	$\overline{RCO}$			–27	41		27	41	ns
t_{PLH}	$\overline{CLR}$↓	$\overline{RCO}$			30	45		30	45	ns
t_{PLH}	RCK↑	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF, $\overline{CLOAD}$ = L		35	53		42	63	ns
t_{PHL}	RCK↑	$\overline{RCO}$			30	45		33	50	ns

NOTE 3: For load circuit and voltage waveforms see page 3-11

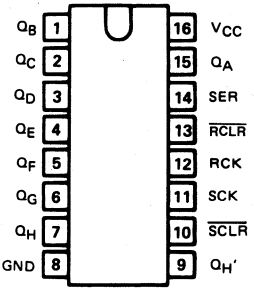
f_{max} = maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

TYPES SN54LS594, SN54LS599, SN74LS594, SN74LS599
8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

D2634, JANUARY 1981

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of totem pole ('LS594) or Open-Collector ('LS599) Parallel Outputs
- Shift Register Has Direct Clear
- Storage Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 20 MHz

SN54LS595, SN54LS596 . . . J OR W PACKAGE
SN74LS595, SN74LS596 . . . J OR N PACKAGE
(TOP VIEW)



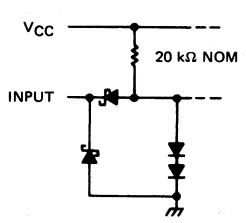
description

These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel buffer ('LS594) or open-collector ('LS599) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading. The storage register also has direct overiding clear.

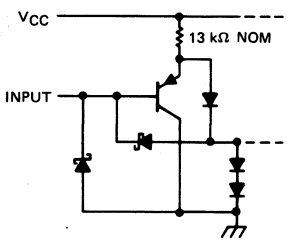
Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

schematics of inputs and outputs

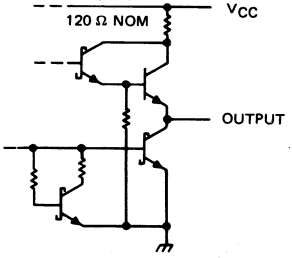
EQUIVALENT OF SERIAL INPUT



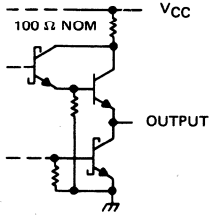
EQUIVALENT OF ALL OTHER INPUTS



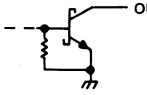
TYPICAL OF Q_H' OUTPUTS



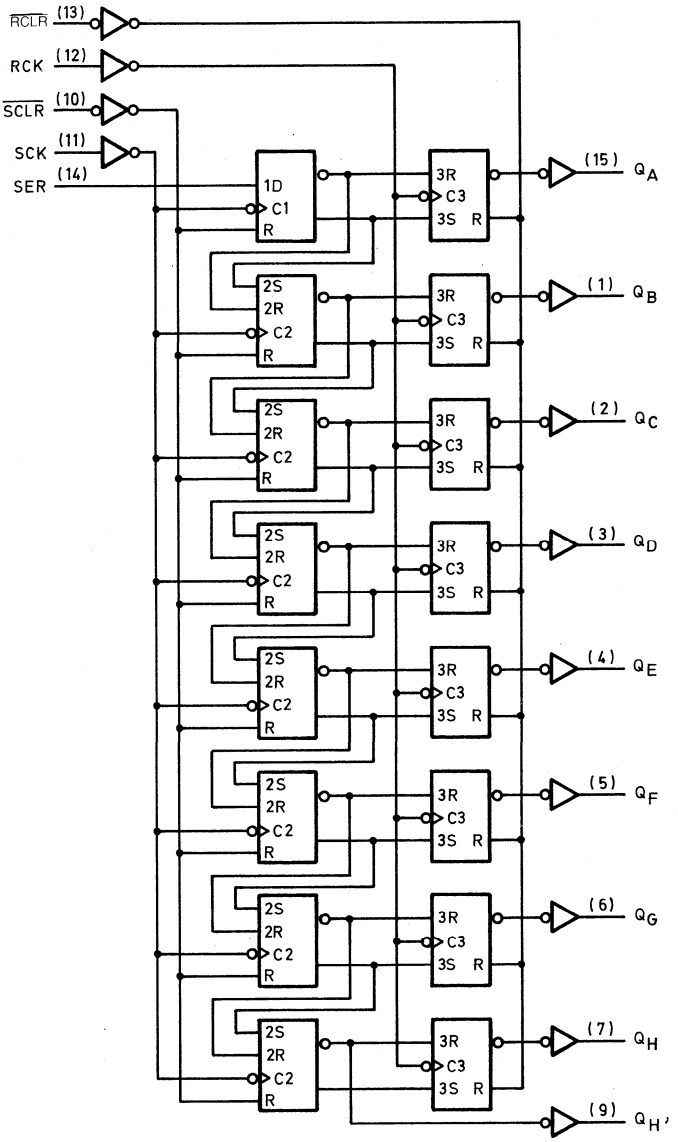
TYPICAL OF ALL OTHER OUTPUTS ('LS594)



TYPICAL OF ALL OTHER OUTPUTS ('LS599)

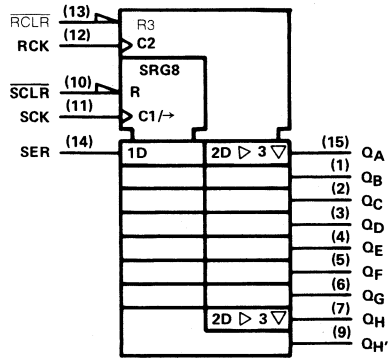


functional block diagram (positive logic)

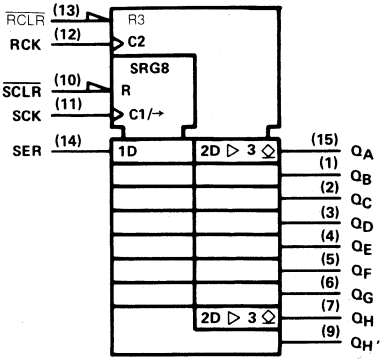


logic symbols

'LS594



'LS599



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS594, SN54LS599 . . . . . −55°C to 125°C
SN74LS594, SN74LS599 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q_A thru Q_H, 'LS599 only			5.5			5.5	V
High-level output current, I_{OH}	$Q_{H'}$			−0.4			−1	mA
	Q_A thru Q_H			−1			−2.6	
Low-level output current, I_{OL}	$Q_{H'}$			8			16	mA
	Q			12			24	
Shift clock frequency, $f_{(SCK)}$		0		20	0		20	MHz
Width of shift clock pulse, $t_{w(SCK)}$		25			25			ns
Width of register clock pulse, $t_{w(RCK)}$		20			20			ns
Setup time t_{su}	$\overline{SCLR}$↑ to SCK↑	20			20			ns
	SER to SCK↑	20			20			
	SCK to RCK (note 2)	40			40			
	$\overline{SCLR}$ to RCK↑	40			40			
	$\overline{RCLR}$ to RCK↑	20			20			
Hold time, t_h	SER from SCK↑	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I =–18mA				–1.5			–1.5	V
V_{OH}	High-level output voltage	'LS594 Q	V_{CC} = MIN,	I_{OH} = –1 mA	2.4	3.2					V
		$Q_{H'}$	V_{IH} = 2 V,	I_{OH} = –2.6 mA				2.4	3.1		
			V_{IL} = V_{IL}max	I_{OH} = –1 mA				2.4	3.2		
I_{OH}	High-level output current	'LS599 Q	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5	
		$Q_{H'}$	V_{IL} = V_{IL}max,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	SER	V_{CC} = MAX,	V_I = 0.4 V			–0.4			–0.4	mA
		All others					–0.2			–0.2	
I_{OS}	Short-circuit output current§	'LS594 Q	V_{CC} = MAX,	V_O = 0	–30		–130	–30		–130	mA
		$Q_{H'}$			–20		–100	–20		–100	
I_{CCH}	Supply current, outputs high	'LS594	V_{CC} = MAX, All possible inputs grounded, All outputs open			34	50		34	50	mA
		'LS599				30	45		30	45	
I_{CCL}	Supply current, outputs low	'LS594				42	65		42	65	mA
		'LS599				38	55		38	55	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS594			'LS599			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SCK↑	$Q_{H'}$	R_L = 1 kΩ,	C_L = 30 pF		12	18		12	18	ns
t_{PHL}						15	23		17	25	
t_{PLH}	RCK↑	Q_A thru Q_H	R_L = 667 Ω,	C_L = 45 pF		12	18		28	42	ns
t_{PHL}						20	30		24	35	
t_{PHL}	$\overline{SCLR}$↓	$Q_{H'}$	R_L = 1 kΩ,	C_L = 30 pF		22	33		24	35	ns
t_{PHL}	$\overline{RCLR}$↓	Q_A thru Q_H	R_L = 667 Ω,	C_L = 45 pF		38	57		40	60	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

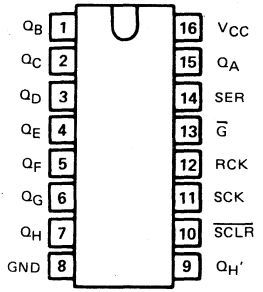
t_{PLH} = propagation delay time, low-to-high-level out
t_{PZH} = output enable time to high level
t_{PHZ} = output disable time from high level
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZL} = output enable time to low level
t_{PLZ} = output disable time from low level

TYPES SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

D2634, JANUARY 1981

- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 20 MHz

SN54LS595, SN54LS596 . . J OR W PACKAGE
SN74LS595, SN74LS596 . . J OR N PACKAGE
(TOP VIEW)

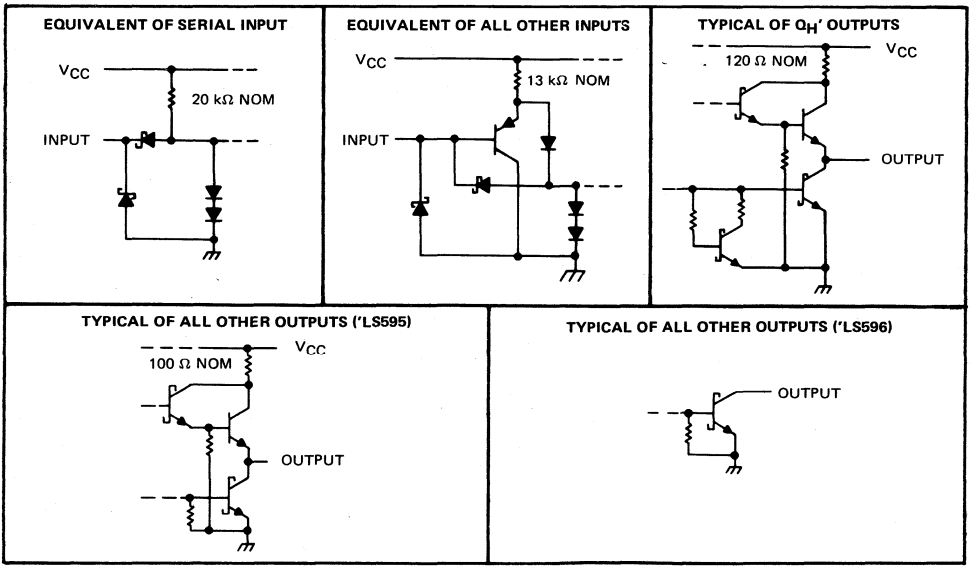


description

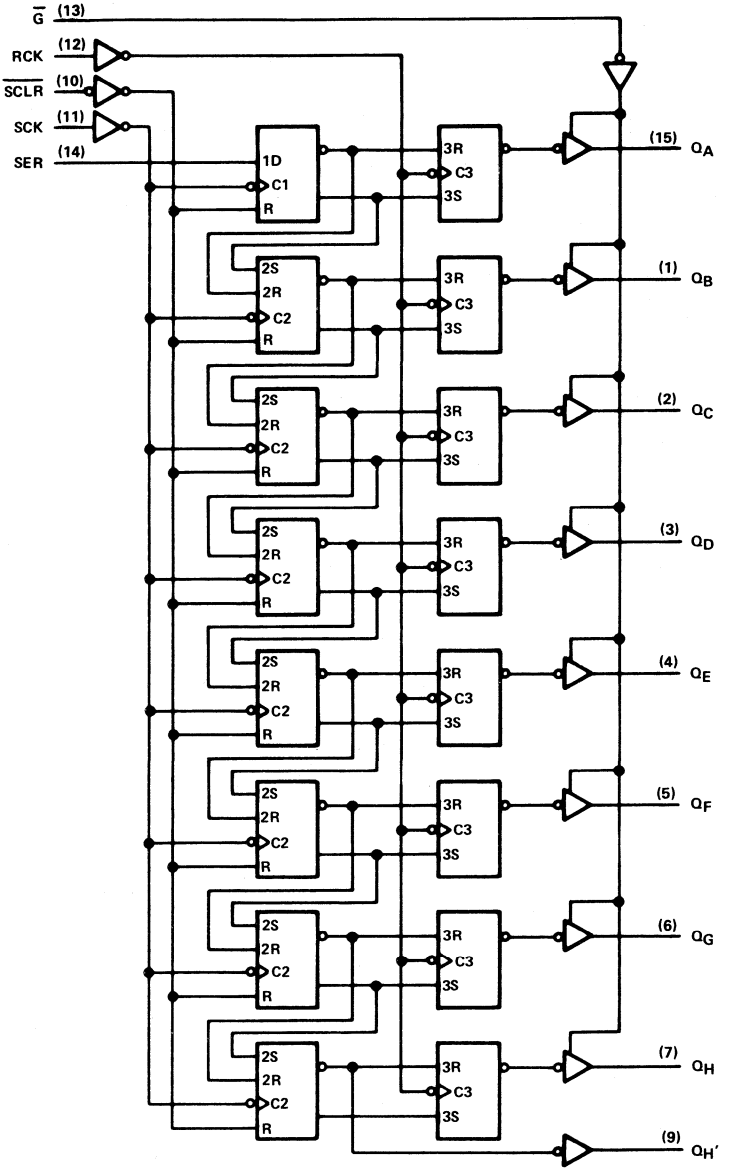
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

schematics of inputs and outputs

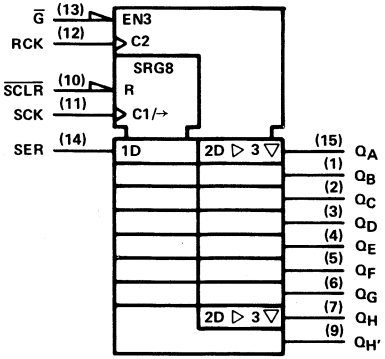


functional block diagram (positive logic)

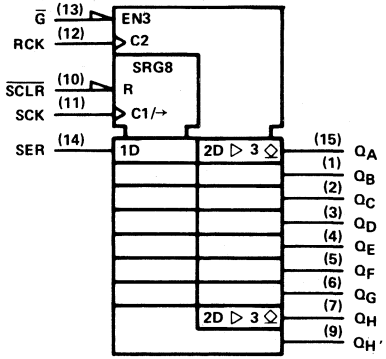


logic symbols

'LS595



'LS596



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596 . . . . . −55°C to 125°C
SN74LS595, SN74LS596 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

7

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	Q_A thru Q_H, 'LS596 only			5.5			5.5	V
High-level output current, I_{OH}	$Q_{H'}$			−0.4			−1	mA
	Q_A thru Q_H			−1			−2.6	
Low-level output current, I_{OL}	$Q_{H'}$			8			16	mA
	Q			12			24	
Shift clock frequency, $f_{(SCK)}$		0		20	0		20	MHz
Width of shift clock pulse, $t_{w(SCK)}$		25			25			ns
Width of register clock pulse, $t_{w(RCK)}$		20			20			ns
Setup time t_{su}	$\overline{SCLR}\uparrow$ to SCK↑	20			20			ns
	SER to SCK↑	20			20			
	$\overline{SCLR}\downarrow$ to RCK↑	40			40			
	SCK↑ to RCK↑ (see note 2)	40			40			
Hold time, t_h	SER from SCK↑	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I =−18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	'LS595 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −1 mA	2.4	3.2					V
		Q_H'		I_{OH} = −2.6 mA				2.4	3.1		
				I_{OH} = −1 mA	2.4	3.2		2.4	3.2		
I_{OH}	High-level output current	'LS596 Q	V_{CC} = MIN, V_{IL} = V_{IL}max	V_{IH} = 2V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Q_H'		I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS595 Q	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	'LS595 Q	V_{CC} MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	SER	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	'LS595 Q	V_{CC} = MAX,	V_O = 0	−30		−130	−30		−130	mA
		Q_H'			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high	'LS595	V_{CC} = MAX, All possible inputs grounded, All outputs open			33	50		33	50	mA
		'LS596				30	45		30	45	
I_{CCL}	Supply current, outputs low	'LS595				42	65		42	65	mA
		'LS596				36	55		36	55	
I_{CCZ}	Supply current, outputs off	'LS595				44	65		44	65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

* All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS595			'LS596			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SCK↑	Q_H'	R_L = 1 kΩ,	C_L = 30 pF		12	18		14	21	ns
t_{PHL}						17	25		20	30	
t_{PHL}	$\overline{SCLR}$↓	Q_M'	R_L = 1 kΩ	C_L = 30 pF		24	35		24	35	ns
t_{PLH}	RCK↑	Q_A thru Q_H	R_L = 667 Ω,	C_L = 45 pF		12	18		28	42	ns
t_{PHL}						24	35		24	35	
t_{PZH}	$\overline{G}$↓	Q_A thru Q_H				20	30				ns
t_{PZL}						25	38				
t_{PHZ}	G↑	Q_A thru Q_H	R_L = 667 Ω,	C_L = 5 pF		20	30				ns
t_{PLZ}						25	38				
t_{PLH}	$\overline{G}$↑	Q_A thru Q_H	R_L = 667 Ω,	C_L = 45 pF					40	60	ns
t_{PHL}	$\overline{G}$↓	Q_A thru Q_H							25	38	

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

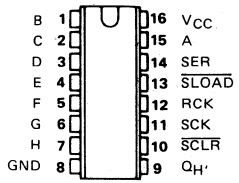
t_{PLH} = propagation delay time, low-to-high-level out
t_{PZH} = output enable time to high level
t_{PHZ} = output disable time from high level
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZL} = output enable time to low level
t_{PLZ} = output disable time from low level

TYPES SN54LS597, SN54LS598, SN74LS597, SN74LS598
8-BIT SHIFT REGISTERS WITH INPUT REGISTERS

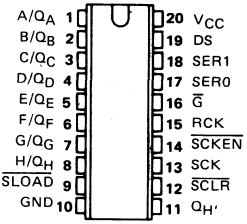
D2635, JANUARY 1981

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Guaranteed Shift Frequency . . . DC to 20 MHz

SN54LS597 . . J OR W PACKAGE
SN74LS597 . . J OR N PACKAGE
(TOP VIEW)



SN54LS598 . . J PACKAGE
SN74LS598 . . J OR N PACKAGE
(TOP VIEW)



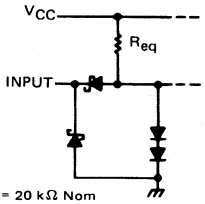
description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

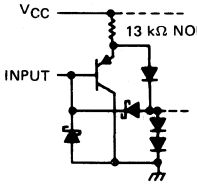
schematics of inputs and outputs

EQUIVALENT OF ALL DATA INPUTS

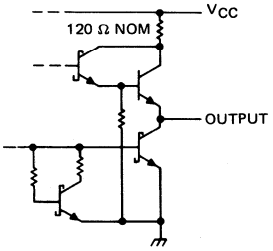


Serial A,B: R_{eq} = 20 kΩ Nom
A thru H: R_{eq} = 25 kΩ Nom

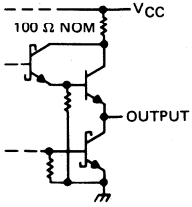
EQUIVALENT OF ALL OTHER INPUTS



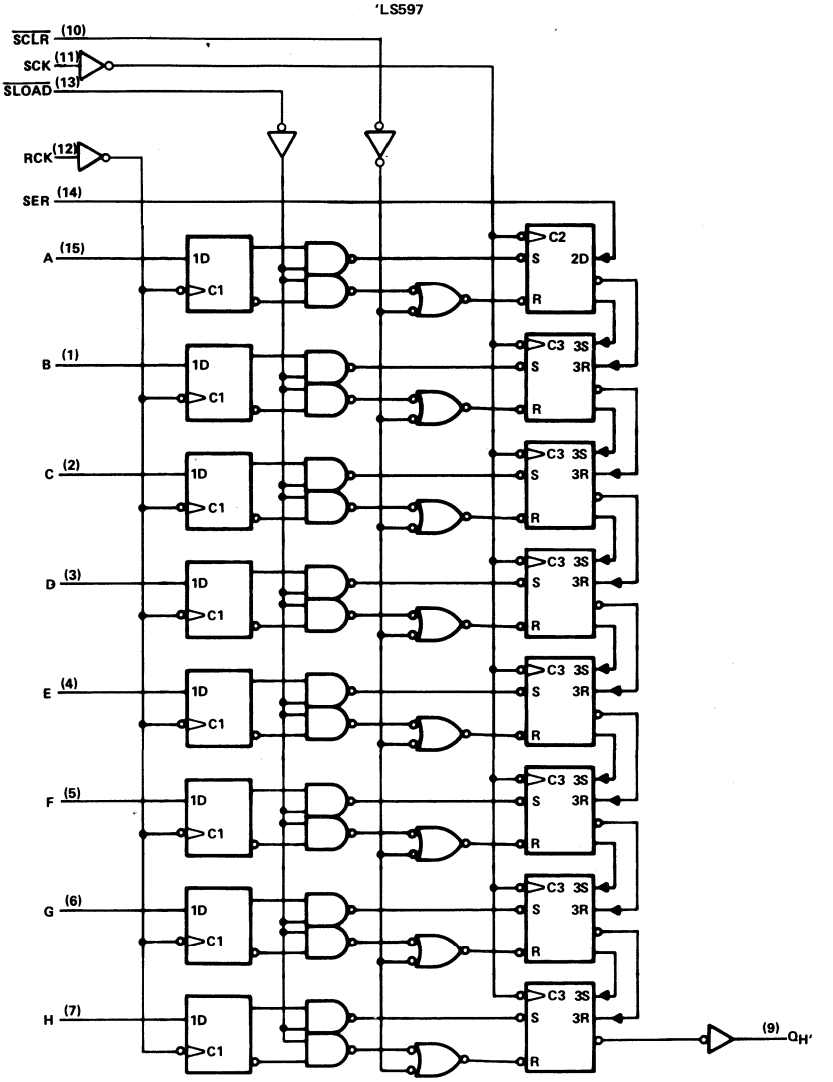
$Q_{H'}$ OUTPUT



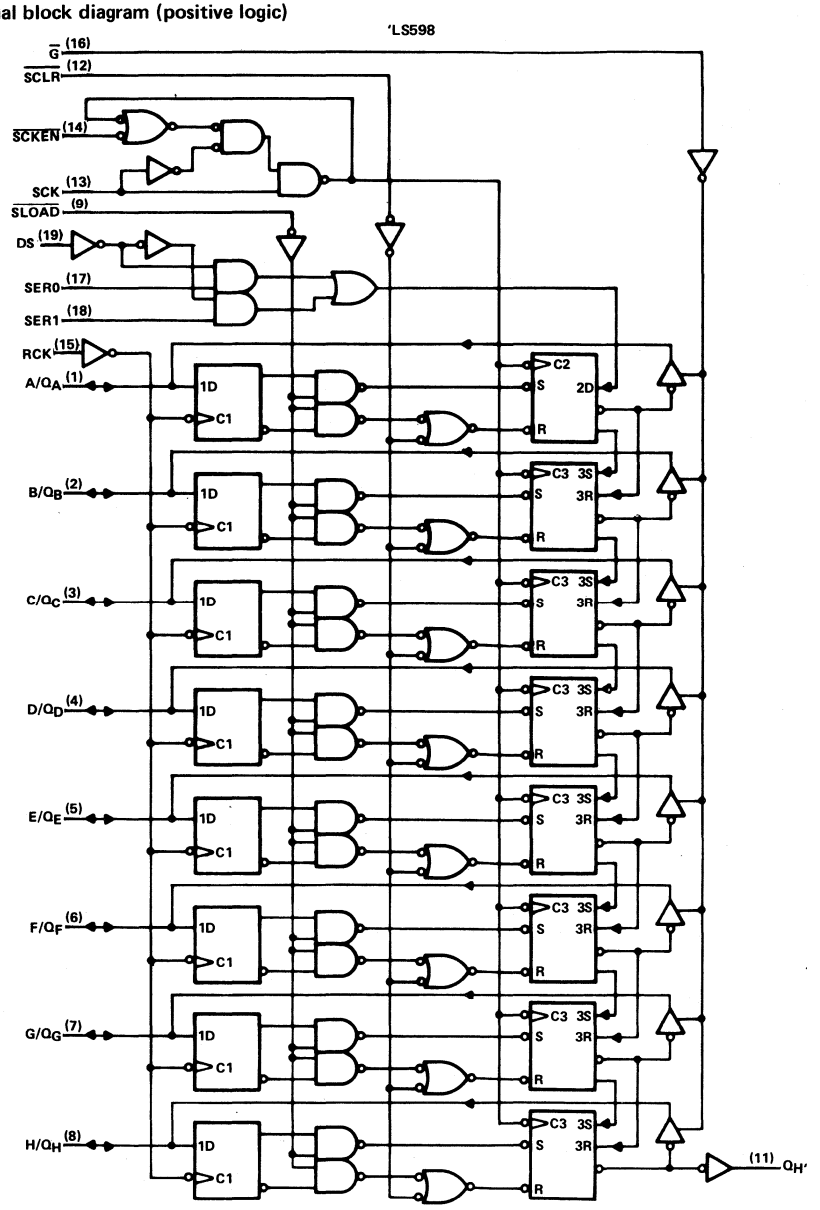
TYPICAL OF Q_A THRU Q_H OUTPUTS ('LS598 ONLY)



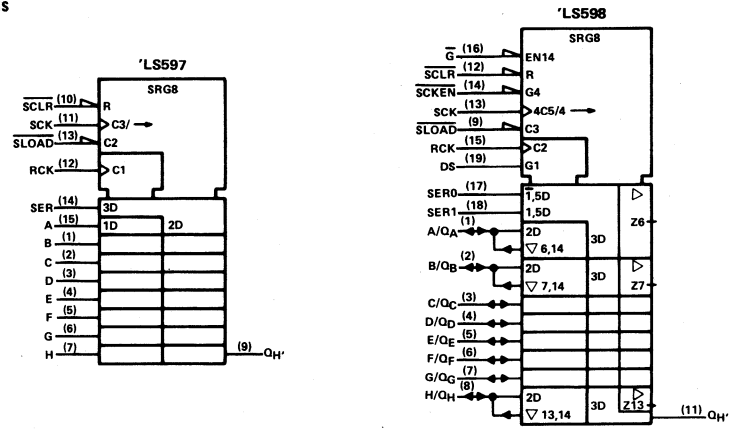
functional block diagram (positive logic)



functional block diagram (positive logic)



logic symbols



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (excluding I/O ports) . . . . . 7 V
Off-state output voltage (including I/O ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS597, SN54LS598 . . . . . −55°C to 125°C
SN74LS597, SN74LS598 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	$Q_{H'}$			−0.4			−1	μA
	Q_A thru Q_H			−1			−2.6	mA
Low-level output current, I_{OL}	$Q_{H'}$			8			16	mA
	Q_A thru Q_H ('LS598 only)			12			24	
Shift clock frequency, $f_{(SCK)}$		0		20	0		20	MHz
Pulse width, t_w	SCK	25			25			ns
	RCK	20			20			
	$\overline{SCLR}$	20			20			
	$\overline{SLOAD}$	20			20			
Shift enable time, t_{enable} ('LS598 only)	SCKEN↓ to SCK↑	20			20			ns
Setup time, t_{su} (see note 2)	$\overline{SCLR}$↑ to SCK↑ 597	25			25			ns
	$\overline{SCLR}$↑ to SCK↑ 598	20			20			
	RCK↑ to $\overline{SLOAD}$↑	40			40			
	$\overline{SLOAD}$↑ to SCK↑	30			30			
	SER to SCK↑	20			20			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: The RCK↑ to SCK↑ setup time ensures that the shift register will see stable data coming from the input register.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I =–18mA				–1.5			–1.5	V
V_{OH}	High-level output voltage	'LS598 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = –1 mA	2.4	3.2					V
		Q_H'		I_{OH} = –2.6 mA				2.4	3.1		
				I_{OH} = –1 mA	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	'LS598 Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Q_H'		I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	'LS598 Q	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 2.7 V			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	'LS598 Q	V_{CC} MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 0.4 V			–200			–200	µA
I_I	Input current at maximum input voltage	'LS598 Q	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V	SCK			–0.8			–0.8	mA
				SER, A thru H,			–0.4			–0.4	
				Others			–0.2			–0.2	
I_{OS}	Short-circuit output current§	'LS598 Q	V_{CC} = MAX,	V_O = 0	–30		–130	–30		–130	mA
		Q_H'			–20		–100	–20		–100	
I_{CC}	Supply current	'LS597	ICCH	V_{CC} = MAX, All possible inputs grounded, All outputs open		35	53		35	53	mA
			ICCL			35	53		35	53	
		'LS598	ICCH			45	68		45	68	
			ICCL			54	80		54	80	
			ICCZ			56	85		56	80	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS597			'LS598			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	SCK		R_L = 1 kΩ C_L = 30 pF	20	35		20	35		MHz
t_{PLH}	SCK↑	Q_H'			15	23		11	17	ns
t_{PHL}	SCK↑	Q_H'			20	30		15	23	ns
t_{PLH}	$\overline{SLOAD}$↑	Q_H'			38	57		28	42	ns
t_{PHL}	$\overline{SLOAD}$↓	Q_H'			29	44		20	30	ns
t_{PHL}	$\overline{SCLR}$↓	Q_H'			24	36		18	27	ns
t_{PLH}	RCK↑	Q_H'	R_L = 1 kΩ, C_L = 30 pF, $\overline{SLOAD}$ = L		41	60		32	48	ns
t_{PHL}	RCK↑	Q_H'			32	48		24	36	ns
t_{PLH}	SCK↑	Q	R_L = 667 Ω, C_L = 45 pF					12	18	ns
t_{PHL}	SCK↑	Q						19	28	ns
t_{PLH}	$\overline{SLOAD}$↓	Q						32	48	ns
t_{PHL}	$\overline{SLOAD}$↓	Q						27	40	ns
t_{PHL}	$\overline{SCLR}$↓	Q						25	38	ns
t_{PZH}	$\overline{G}$↓	Q						26	31	ns
t_{PZL}	$\overline{G}$↓	Q						29	43	ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF					25	38	ns
t_{PLZ}	G↑	Q						20	30	ns

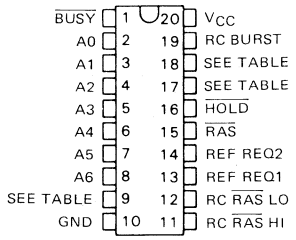
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

TYPES SN54LS600A THRU SN54LS603A, SN74LS600A THRU SN74LS603A MEMORY REFRESH CONTROLLERS

D2547, JANUARY 1981 – REVISED JANUARY 1983

- Controls Refresh Cycle of 4K, 16K, and 64K Dynamic RAMs
- Creates Static RAM Appearance
- Choice of Transparent, Cycle Steal, or Burst Refresh Modes
- 3-State Outputs Drive Bus Lines Directly
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



SELECTION TABLE

DEVICE	REFRESH MODES	MEMORY SIZE	PIN ASSIGNMENTS		
			PIN 9	PIN 17	PIN 18
'LS600A	Transparent, Burst	4K or 16K	4K/16K	LATCHED RCO	RESET LATCHED RCO
'LS601A	Transparent, Burst	64K	A7	LATCHED RCO	RESET LATCHED RCO
'LS602A	Cycle Steal, Burst	4K or 16K	4K/16K	READY	RC CYCLE STEAL
'LS603A	Cycle Steal, Burst	64K	A7	READY	RC CYCLE STEAL

description

The 'LS600A thru 'LS603A memory refresh controllers contain one 8-bit synchronous counter, nine 3-state buffer drivers, four RC-controlled multivibrators, and other control circuitry on a single monolithic chip. These devices are designed to provide RAS-only refresh on 4K, 16K, and 64K dynamic RAMs. The 'LS600A and 'LS601A provide transparent refresh while the 'LS602A and 'LS603A provide cycle-steal refresh. In addition, a burst-mode timer is provided to warn the CPU that the maximum allowable refresh time is about to be violated.

operating modes

In the transparent refresh mode ('LS600A or 'LS601A), row-refresh cycles occur only during inactive CPU-memory times. In most cases the entire memory refresh sequence can be completed "transparently" without interrupting CPU operations. During idle CPU-memory periods, the REF REQ pins should be taken high so as many rows as possible can be refreshed. A low from BUSY will signal the CPU to wait until the end of that current row refresh before reinstating operations. If all row addresses have been refreshed before the burst-mode timer expires, the burst-mode timer will reset.

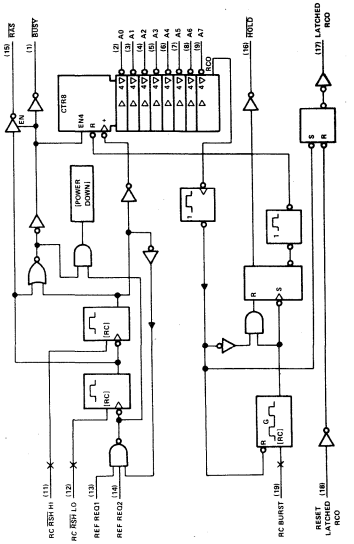
If the maximum allowable refresh time of the dynamic RAM is about to be exceeded, the burst mode timer will expire causing the HOLD pin to go low. This signals the CPU that a burst-mode refresh is manadatory and the burst-mode refresh will be accomplished when the CPU takes the REF REQ pins high. To ensure that all rows are refreshed, the address counter is reset to zero whenever the burst-mode timer expires. After the last row has been refreshed, the HOLD pin will return high, and the burst-mode timer will reset. The CPU can then return to normal transparent operation.

A LATCHED RCO output pin is also provided on the 'LS600A and 'LS601A to detect when the last row has been refreshed. Upon seeing a RCO from the address counter, the LATCHED RCO output will be set high. This latch is reset by providing a high-going pulse on the RESET LATCHED RCO input.

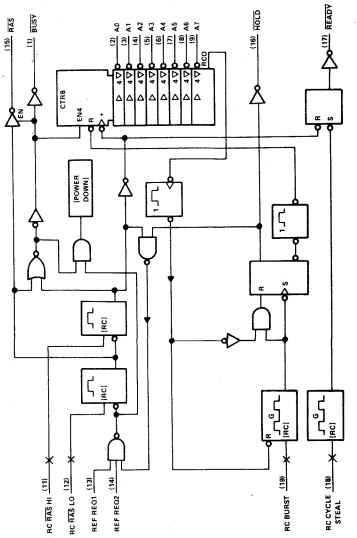
In the cycle-steal refresh mode ('LS602A or 'LS603A), refreshing is accomplished by dividing the safe refresh time into equal segments and refreshing one row in each segment. The segment time is programmed via the RC CYCLE STEAL input and will produce a low level on the READY output at the end of each segment period. This indicates to the CPU to suspend operations for one memory cycle for a row refresh. In effect it "steals" one memory cycle from the CPU. After the CPU recognizes the cycle-steal signal from the READY output, it must take both REF REQ pins high. These devices will then refresh one row and return control back to the CPU by taking READY high. The burst-mode timer is also provided to prevent exceeding the maximum allowable refresh time, and operates in the same manner as in the 'LS600A and 'LS601A.

TEXAS INSTRUMENTS

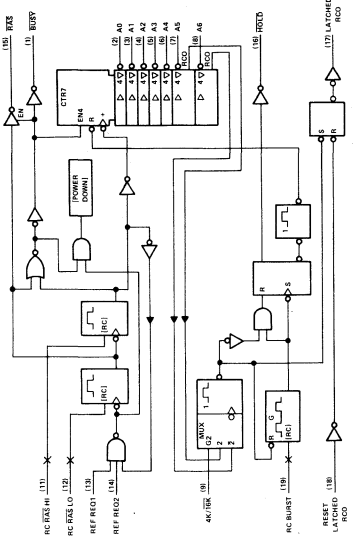
'LS601A



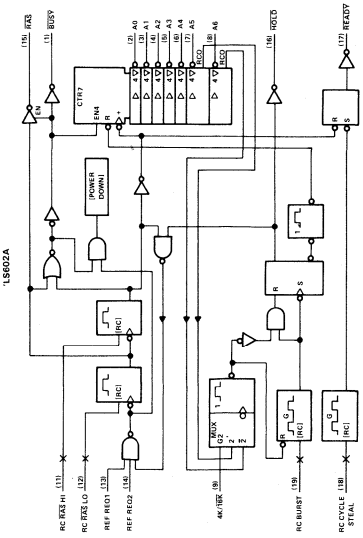
'LS603A



'LS600A



'LS602A



7

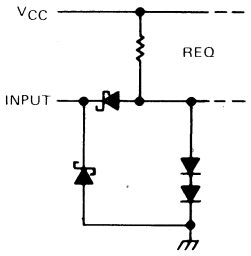
PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	$\overline{\text{BUSY}}$	Active output indicates to the CPU that a refresh cycle is in progress.
16	$\overline{\text{HOLD}}$	Active output should be a priority interrupt to the CPU for emergency burst refresh.
15	$\overline{\text{RAS}}$	3-state output row address strobe.
11	RC $\overline{\text{RAS}}$ HI	Timing node for high-level portion of $\overline{\text{RAS}}$. See Note 1.
12	RC $\overline{\text{RAS}}$ LO	Timing node for low-level portion of $\overline{\text{RAS}}$. See Note 1.
2-8	A0 thru A6	3-state output row address lines.
9	A7	MSB row address line for 'LS601A and 'LS603A (64K-bit memory controllers).
9	4K/$\overline{\text{16K}}$	A high input level disables the A5 row address line for 'LS600A and 'LS602A. (The high-level input makes the count chain 5 bits long while the low-level makes the count chain 6 bits long.)
17	$\overline{\text{READY}}$	Interrupt to CPU for cycle steal refresh ('LS602A and 'LS603A).
17	LATCHED RCO	Normally high-level, will latch low upon RCO of counter ('LS600A or 'LS601A).
18	RC CYCLE STEAL	Timing node that controls the $\overline{\text{READY}}$ output ('LS602A and 'LS603A). See Note 1.
18	RESET LATCHED RCO	Normally high-level, when pulsed low the LATCHED RCO output will be reset ('LS600A and 'LS601A).
19	RC BURST	Timing node for burst refresh. See Note 1.
13, 14	REF REQ1, REF REQ2	High level on both pins starts and continues row refresh. Low on either pin inhibits refresh.
20, 10	V_{CC}, GND	5-V power supply and network ground pins.

NOTE 1: All timing nodes require a resistor to V_{CC} and a capacitor to GND.

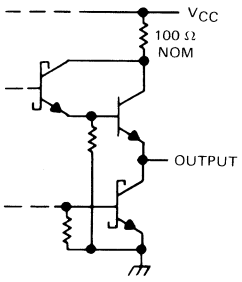
schematics of inputs and outputs

EQUIVALENT OF REF REQ, 4K/$\overline{\text{16K}}$, AND RESET LATCHED RCO INPUTS

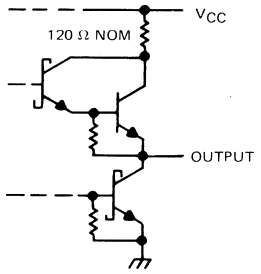


REF REQ: Req 20 kΩ NOM
4K/$\overline{\text{16K}}$: Req 30 kΩ NOM

TYPICAL OF $\overline{\text{RAS}}$ AND A OUTPUTS



TYPICAL OF $\overline{\text{BUSY}}$, $\overline{\text{HOLD}}$, $\overline{\text{READY}}$ AND LATCHED RCO OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS600A thru SN54LS603A . . . . . −55°C to 125°C
SN74LS600A thru SN74LS603A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 2: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	A, $\overline{RAS}$			−1			−2.6	mA
	All others			−400			−400	μA
Low-level output current, I_{OL}	A, $\overline{RAS}$			12			24	mA
	All others			4			8	
Duration of $\overline{RAS}$ output pulse†	High, t_{SHSL}	75			75			ns
	Low, t_{SLSH}	75			75			
Duration of RESET LATCHED RCO pulse, t_{RHRL}		35			35			ns
Duration of REF REQ pulse during CYCLE STEAL operation, t_{QHQL}								ns
External timing resistor, R_{ext}	RC $\overline{RAS}$ LO, RC $\overline{RAS}$ HI	1		6	1		6	kΩ
	RC BURST, RC CYCLE STEAL	1		1000	1		1000	
Operating free-air temperature, T_A		−55		125	0		70	°C

† *Maximum operating frequency for the address counter corresponds to its minimum period, which is the sum of $t_{w(RAS\text{-}HI)}$ min and $t_{w(RAS\text{-}LI)}$ min.*

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −1.8 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	A, $\overline{RAS}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −1 mA	2.4	2.9					V
				I_{OH} = −2.6 mA				2.4	2.9		
		All Others		I_{OH} = −400 μA	2.5	3.1		2.7	3.1		
V_{OL}	Low-level output voltage	A, $\overline{RAS}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		All others		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	A, $\overline{RAS}$	V_{CC} = MAX, REF REQ at V_{IL} max	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	A, $\overline{RAS}$	V_{CC} = MAX		−30		−130	−30		−130	mA
		All others			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, RC $\overline{RAS}$ LO and REF REQ at 0 V			50	85		50	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 3

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{QHBL}	REF REQ↑	$\overline{BUSY}$	C_L = 15 pF, R_L = 2 kΩ		30	45	ns
t_{SLBH}†	$\overline{RAS}$↑	$\overline{BUSY}$			245	300	ns
t_{QHSV}	REF REQ↑	$\overline{RAS}$	C_L = 320 pF, R_L = 667Ω		47	70	ns
t_{SHSZ}†	$\overline{RAS}$↑	$\overline{RAS}$	C_L = 5 pF, R_L = 667Ω		245	300	ns
t_{QHAV}	REF REQ↑	ADDRESS	C_L = 160 pF, R_L = 667Ω		38	65	ns
t_{SHAZ}†	$\overline{RAS}$↑	ADDRESS	C_L = 5 pF, R_L = 667Ω		245	300	ns
t_{RHCL}	RESET LATCHED RCO↑	LATCHED RCO	C_L = 15 pF, R_L = 2 kΩ		37	55	ns
t_{SHYH}	$\overline{RAS}$↑	$\overline{READY}$					ns
t_{SLSH}‡	$\overline{RAS}$↓	$\overline{RAS}$	C_L = 320 pF, R_L = 667Ω		210		ns
t_{SHSL}†	$\overline{RAS}$↑	$\overline{RAS}$			245		ns
t_{DHDL}§	$\overline{HOLD}$↑	$\overline{HOLD}$	C_L = 15 pF, R_L = 2 kΩ		3.56		ms
t_{YLYL}‖	$\overline{READY}$↓	$\overline{READY}$					μs

† Depends on RC network at pin 11 (4 kΩ, 200 pF used for testing).
‡ Depends on RC network at pin 12 (4 kΩ, 200 pF used for testing).
§ Depends on RC network at pin 19 (680 kΩ, 0.022 μF used for testing).
‖ Depends on RC network at pin 18.
NOTE 3: Load circuit and voltage waveforms are shown on page 3-11 of *The TTL Data Book for Design Engineers,* Second Edition, LCC4112.

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or ''don't care'' level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	A or C SUBSCRIPT
$\overline{BUSY}$	B
$\overline{HOLD}$	D
$\overline{RAS}$	S
A0 – A7	A
$\overline{READY}$	Y
LATCHED RCO	C
RESET LATCHED RCO	R
REF REQ	Q

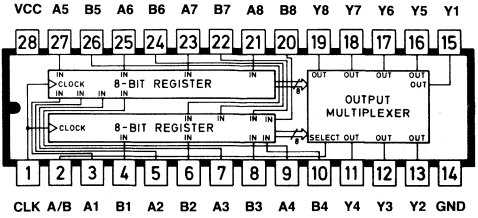
TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607 OCTAL 2-INPUT MULTIPLEXED REGISTERS

REVISED OCTOBER 1983

(TIM99604 THRU TIM99607)

- Choice of Outputs:
  - Three-State ('LS604, 'LS606)
  - Open-Collector ('LS605, 'LS607)
- 16 D-Type Registers, One for each Data Input
- Multiplexer Selects Stored Data from Either A Bus or B Bus
- Application Oriented:
  - Maximum Speed ('LS604, 'LS605)
  - Glitch-Free Operation ('LS606, 'LS607)

SN54LS604 thru SN54LS607 . . . J PACKAGE
SN74LS604 thru SN74LS607 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS604 through 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 and 'LS605 are optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

The SN54LS604 through SN54LS607 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS604 through SN74LS607 are characterized for operation from 0°C to 70°C.

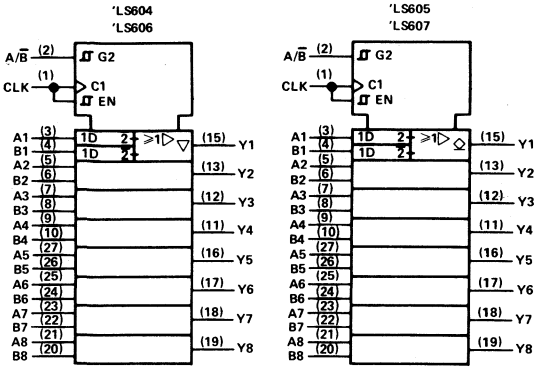
FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/$\overline{B}$	CLOCK	Y1-Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

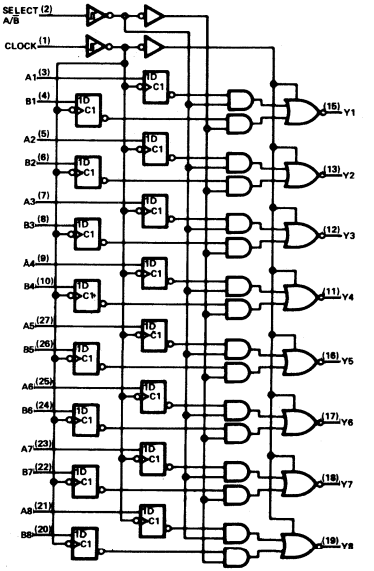
H = high level (steady state)
L = low level (steady state)
X = irrelevant
Z = high-impedance state
Off = H if pull-up resistor is connected to open-collector output
↑ = transistion from low to high level

TYPES SN54LS604 THRU SN54LS607, SN74LS604 THRU SN74LS607
OCTAL 2-INPUT MULTIPLEXED LATCHES

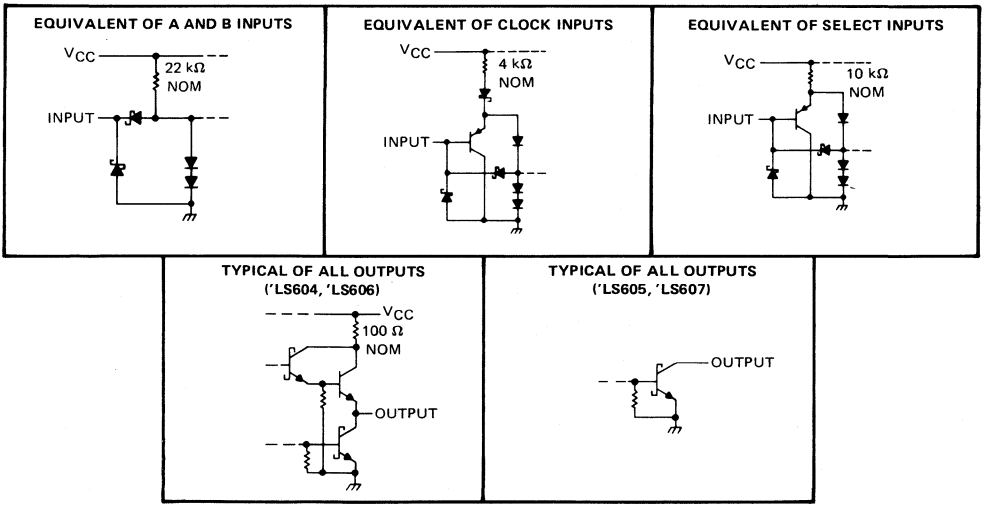
logic symbols



functional block diagram (positive logic)



schematics of inputs and outputs



recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			55	70		55	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select $A/\overline{B}$ (Data: A = H, B = L)	C_L = 45 pF, R_L = 667 Ω, See Note 3		15	25		36	50	ns
t_{PHL}				23	35		16	30	
t_{PLH}	Select $A/\overline{B}$ (Data: A = L, B = H)			31	45		22	35	ns
t_{PHL}				19	30		22	35	
t_{PZH}	Clock			19	30		27	40	ns
t_{PZL}				28	40		35	50	
t_{PHZ}	Clock	C_L = 5 pF, R_L = 667 Ω, See Note 3		20	30		20	30	ns
t_{PLZ}				15	25		15	25	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3: Load circuits and voltage waveforms are shown on page 3-11

recommended operating conditions

	SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS605 SN54LS607			SN74LS605 SN74LS607			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V	A, B			0.1			0.1	mA
				CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V	A, B			20			20	μA
				CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V	A, B			−0.4			−0.4	mA
				CLK, SELECT			−0.2			−0.2	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			40	60		40	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS605			'LS607			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select A/$\overline{B}$	C_L = 45 pF, R_L = 667 Ω, See Note 3		28	40		51	70	ns
t_{PHL}	(Data: A = H, B = L)			28	40		21	30	
t_{PLH}	Select A/$\overline{B}$			39	60		28	40	ns
t_{PHL}	(Data: A = L, B = H)			25	40		28	40	
t_{PLH}	Clock			27	40		30	45	ns
t_{PHL}				25	40		32	45	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
NOTE 3: Load circuits and voltage waveforms are shown on page 3-11

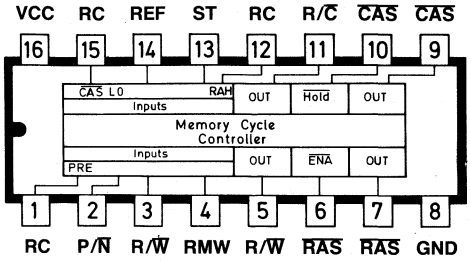
TYPES SN54LS608, SN74LS608
MEMORY CYCLE CONTROLLERS

D2548, JANUARY 1981

(TIM99608)

- Provides Correct Timing for Memory Cycles
  - Read Cycle
  - Write Cycle
  - Read-Modify-Write Cycle
  - RAS-Only Refresh Cycle
- Page or Normal Modes
- Stand-Alone Controller for CPU-to-Memory Interface
- Also Designed to be Part of a Three-Chip Set Consisting of 'LS600 thru 'LS603, 'LS604 thru 'LS607, and 'LS608
- $\overline{RAS}$ Output is 3-State to Share Bus With 'LS600 thru 'LS603
- Critical Times Are User RC-Programmable to Optimize System Performance

SN54LS608 . . . J PACKAGE
SN74LS608 . . . J OR N PACKAGE
(TOP VIEW)



description

The 'LS608 memory cycle controller is designed to interface between a microprocessor and dynamic RAM memories. It contains six RS latches, five D-type flip-flops, and more than 50 miscellaneous gates on a single chip. The 'LS608 combines maximum flexibility and ease of programming via RC nodes to allow optimum memory cycle performance.

The 'LS608 can operate as a stand-alone interface but is also designed to be part of a three-chip memory controller set. The user must select one of the 'LS600 thru 'LS603 refresh controllers and one of the 'LS604 thru 'LS607 multiplexers to use along with the 'LS608 memory cycle controller for complete dynamic RAM control.

After the user has selected and attached RC networks to pins 1, 12, and 15, the 'LS608 will deliver proper $\overline{RAS}$, $\overline{CAS}$, and READ/$\overline{WRITE}$ output signals to execute one memory cycle as the start input is switched from low to high. The actual cycle executed will depend upon steady-state input conditions of the 'LS608 as indicated in the table below.

MEMORY CYCLE	MODE	INPUT CONDITIONS						
		P/$\overline{N}$ IN	R/$\overline{W}$ IN	$\overline{RMW}$ IN	$\overline{RAS}$ $\overline{ENABLE}$ IN	$\overline{CAS}$ $\overline{HOLD}$ IN	START IN	REFRESH IN
READ	PAGE	H	H	H	L	H	↑	L
WRITE		H	L	H	L	H	↑	L
READ-MODIFY-WRITE		H	H	L	L	H	↑	L
READ	NORMAL	L	H	H	L	H	↑	L
WRITE		L	L	H	L	H	↑	L
READ-MODIFY-WRITE		L	H	L	L	H	↑	L
REFRESH	REFRESH	x	x	x	L	H	↑	H
EXTERNAL REFRESH		x	x	x	H	H	x	L

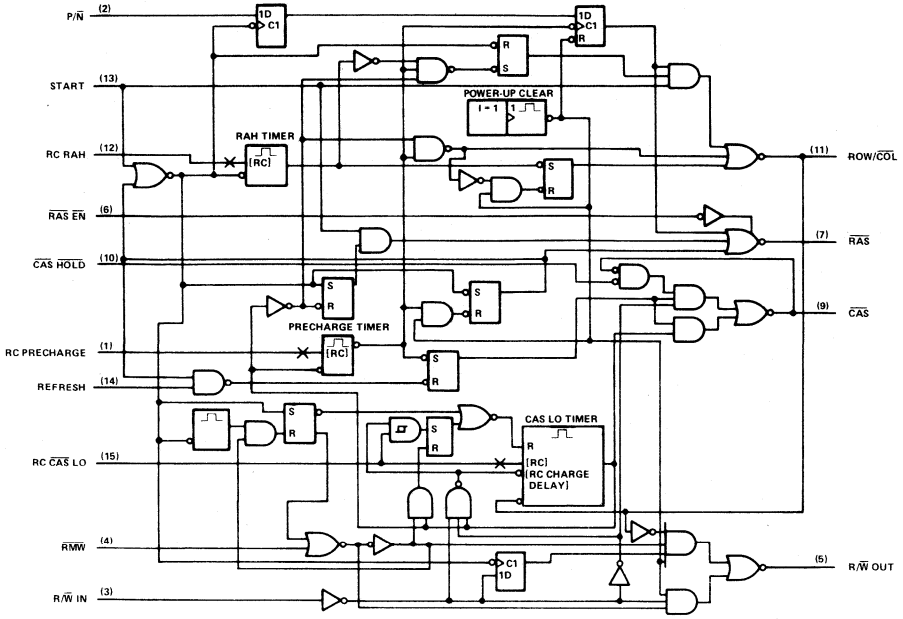
H = High, L = Low, x = irrelevant, ↑ = low-to-high transition

PIN FUNCTION TABLE

PIN	PIN NAME	FUNCTIONAL DESCRIPTION
1	RC PRECHARGE	User-programmable timing node* for precharge ($\overline{CAS}$ high and $\overline{RAS}$ high).
2	P/$\overline{N}$ IN	When high, initiates a ready cycle (holds R/W OUT high) and, when low, page mode read or write cycle holds $\overline{RAS}$ continuously low while $\overline{CAS}$ and column addresses are sequenced.
3	R/$\overline{W}$ IN	When high, initiates a ready cycle (holds R/$\overline{W}$ OUT high) and, when low, initiates a write cycle (holds R/$\overline{W}$ OUT low) if pin 4 is high and pin 14 is low.
4	$\overline{RMW}$ IN	When low, enables read-modify-write cycle. R/$\overline{W}$ IN must be high at the start of the RMW cycle.
5	R/$\overline{W}$ OUT	When high, indicates a read cycle is in progress. When low, indicates a write cycle is in progress. Normally ties to a $\overline{W}$ memory input in a system.
6	$\overline{RAS}$ $\overline{ENABLE}$ IN	When low, enables $\overline{RAS}$ output. When high, $\overline{RAS}$ is in the high-impedance or third state.
7	$\overline{RAS}$ OUT	3-state row-address-strobe output controlled by $\overline{RAS}$ $\overline{ENABLE}$ IN. In the three-chip controller set, the $\overline{RAS}$ output of the 'LS608 ties to the $\overline{RAS}$ output of the refresh controller ('LS600 thru 'LS603).
8	GND	Device and substrate ground.
9	$\overline{CAS}$ OUT	Column-address-strobe output.
10	$\overline{CAS}$ $\overline{HOLD}$ IN	When low, allows $\overline{CAS}$ to latch in low state. When high, latch is removed. Can be used to improve data retrieval during read cycle.
11	ROW/$\overline{COL}$ (or $\overline{MEMBSY}$) OUT	In a system where the 'LS608 is a stand-alone controller, this output indicates a memory-busy condition to the microprocessor. When the 'LS608 is used as a part of a three-chip controller set, this pin ties to the SELECT A/$\overline{B}$ input of the multiplexer ('LS604 thru 'LS607) for selecting row and column in addition to indicating a memory-busy condition to the microprocessor.
12	RC RAH	User-programmable timing node* for row address hold time. (high level at ROW/$\overline{COL}$ OUT).
13	START IN	When changed from low to high, initiates a memory cycle.
14	REFRESH IN	When high, enables $\overline{RAS}$-only refresh cycle.
15	RC $\overline{CAS}$ LO	User-programmable timing node* for column-address-strobe low time.
16	V_{CC}	5-volt power supply terminal.

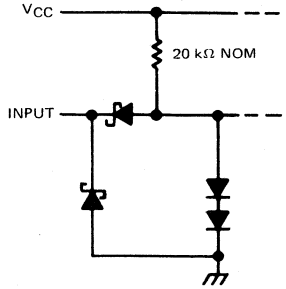
*All timing nodes require a resistor to V_{CC} and a capacitor to ground. Programmed time is approximately 0.29 RC.

functional block diagram (positive logic)

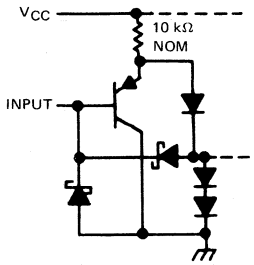


schematics of inputs and outputs

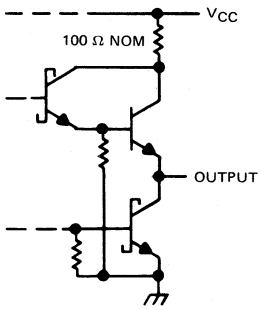
EQUIVALENT OF REFRESH, R/$\overline{W}$, AND $\overline{RMW}$ INPUTS



EQUIVALENT OF ALL OTHER INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS608 . . . . . −55°C to 125°C
SN74LS608 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS608			SN74LS608			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	ROW/$\overline{\text{COL}}$			−0.4			−0.4	mA
	$\overline{\text{RAS}}$			−1			−2.6	
	All others			−1.2			−1.2	
Low-level output current, I_{OL}	ROW/$\overline{\text{COL}}$			4			8	mA
	All others			12			24	
Setup time, t_{su}	R/$\overline{\text{W}}$, $\overline{\text{RMW}}$, P/$\overline{\text{N}}$, or REFRESH to START↑	20			20			ns
	$\overline{\text{CAS}}$ HOLD to $\overline{\text{CAS}}$↓	20			20			
Hold time, t_h		0			0			ns
External timing resistor, R_{ext}	RC RAH	0.1		2	0.1		2	kΩ
	RC $\overline{\text{CAS}}$ LO; RC PRECHARGE	1		6	1		6	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS608			SN74LS608			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	ROW/$\overline{\text{COL}}$	V_{CC} = MIN,	I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
		$\overline{\text{RAS}}$	V_{IH} = 2 V,	I_{OH} = MAX	2.4	3.2		2.4	3.1		
		Others	V_{IL} = V_{IL} max	I_{OH} = −1.2 mA	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	ROW/$\overline{\text{COL}}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
		Others		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	$\overline{\text{RAS}}$	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	REFRESH, R/$\overline{\text{W}}$, $\overline{\text{RMW}}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	ROW/$\overline{\text{COL}}$	V_{CC} = MAX,	V_O = 0 V	−10		−50	−10		−50	mA
		Others			−30		−130	−30		−130	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at GND	Outputs open,	38		65	38		65	mA

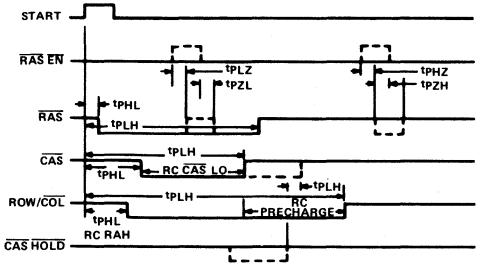
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND (see waveforms for more detail)

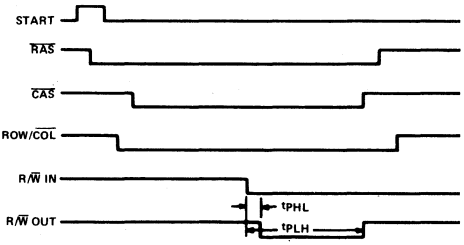
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MODE	MIN	TYP	MAX	UNIT
t_{PHL}	START ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}	NORMAL READ		8	15	ns
t_{PLH}†	START ↑	$\overline{RAS}$			290	363	435	ns
t_{PHL}‡	START ↑	$\overline{CAS}$			100	126	150	ns
t_{PLH}†	START ↑	$\overline{CAS}$			275	342	410	ns
t_{PHL}‡	START ↑	R/$\overline{W}$		NORMAL WRITE	90	113	135	ns
t_{PLH}†	START ↑	R/$\overline{W}$			303	383	460	ns
t_{PLH}	$\overline{CAS}$ HOLD ↑	$\overline{CAS}$		NORMAL READ		10	15	ns
t_{PHL}‡	START ↑	ROW/$\overline{COL}$	R_L = 2 kΩ to V_{CC}		75	100	125	ns
t_{PLH}§	START ↑	ROW/$\overline{COL}$			485	609	730	ns
t_{PHL}	R/$\overline{W}$ ↓	R/$\overline{W}$	R_L = 667 Ω to V_{CC}	NORMAL RMW		13	20	ns
t_{PLH}¶	R/$\overline{W}$ ↓	R/$\overline{W}$				10	15	ns
t_{PLH}	$\overline{RMW}$ ↑	$\overline{CAS}$				34	50	ns
t_{PLH}♦	$\overline{RMW}$ ↑	ROW/$\overline{COL}$			240	300	360	ns
t_{PZH}	$\overline{RAS}$ EN ↓	$\overline{RAS}$	R_L = 667 Ω to GND	NORMAL READ		13	20	ns
t_{PZL}	$\overline{RAS}$ EN ↓	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			14	25	ns
t_{PHZ}	$\overline{RAS}$ EN ↑	$\overline{RAS}$	R_L = 667 Ω to GND			7	15	ns
t_{PLZ}	$\overline{RAS}$ EN ↑	$\overline{RAS}$	R_L = 667 Ω to V_{CC}			16	25	ns

† Depends on RC network at pin 12 (2 kΩ, 180 pF used for testing) and the RC network at pin 15 (5 kΩ, 180 pF).
‡ Depends on RC network at pin 12 (2 kΩ, 180 pF).
§ Depends on RC networks at pin 12 (2 kΩ, 180 pF), pin 15 (5 kΩ, 180 pF), and pin 1 (5 kΩ, 180 pF).
¶ Depends on RC network at pin 15 (5 kΩ, 180 pF).
♦ Depends on RC network at pin 1 (5 kΩ, 180 pF).
NOTE 2: Measurement point for all t_{PHZ} output pulses is 2.9 V. Measurement point for all t_{PLZ} output pulses is 0.8 V. All other measurement points are 1.3 V.

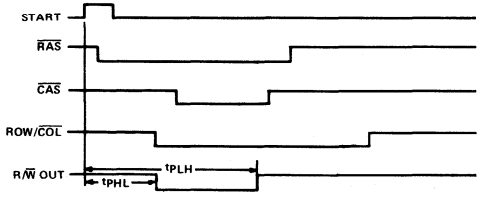
PARAMETER MEASUREMENT INFORMATION



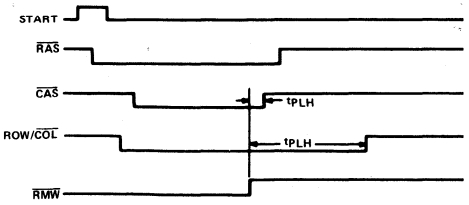
NORMAL READ MODE (R/$\overline{W}$ IN = H)



NORMAL READ-MODIFY-WRITE MODE ($\overline{RMW}$ = L)



NORMAL WRITE MODE (R/$\overline{W}$ IN = L)



NORMAL READ-MODIFY-WRITE ABORT AFTER READ (R/$\overline{W}$ = H)

TYPES SN54LS610 THRU SN54LS613, SN74LS610 THRU SN74LS613 MEMORY MAPPERS

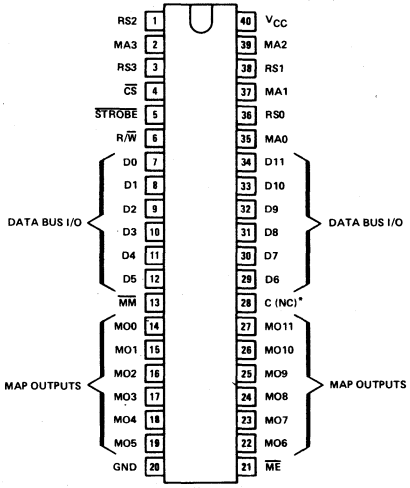
D2549, JANUARY 1981

(TIM99610 THRU TIM99613)

- Expands 4 Address Lines to 12 Address Lines
- Designed for Paged Memory Mapping
- Output Latches Provided on 'LS610 and 'LS611
- Choice of 3-State or Open-Collector Map Outputs
- Compatible with TMS 9900 and Other Microprocessors

DEVICE	OUTPUTS LATCHED	MAP OUTPUT TYPE
'LS610	Yes	3-State
'LS611	Yes	Open-Collector
'LS612	No	3-State
'LS613	No	Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



*NOTE: Pin 28 has no internal connection on 'LS612 and 'LS613

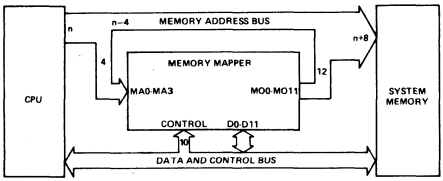
description

These memory-mapper integrated circuits contain a 4-line to 16-line decoder, a 16-word by 12-bit RAM, 16 channels of 2-line to 1-line multiplexers, and other miscellaneous circuitry on a monolithic chip. The 'LS610 and 'LS611 also contain 12 latches with an enable control.

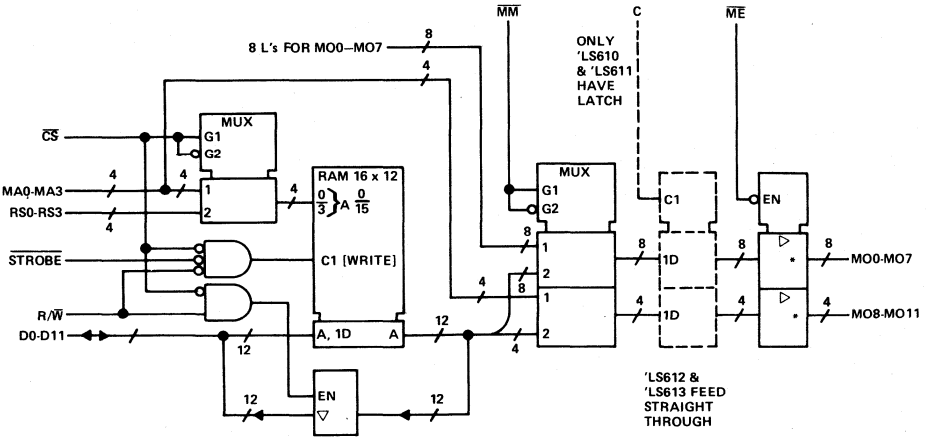
The memory mappers are designed to expand a microprocessor's memory address capability by eight bits. Four bits of the memory address bus (see the figure below) can be used to select one of 16 map registers that contain 12 bits each. These 12 bits are presented to the system memory address bus through the map output buffers along with the unused memory address bits from the CPU. However, addressable memory space without reloading the map registers is the same as would be available with the memory mapper left out. The addressable memory space is increased only by periodically reloading the map registers from the data bus.

This configuration lends itself to memory utilization of 16 pages of $2^{(n-4)}$ registers each without reloading (n = number of address bits available from CPU).

These devices have four modes of operation (read, write, map, and pass). Data may be read from or loaded into the map register selected by the register select inputs (RS0 thru RS3) under control of R/$\overline{W}$ whenever chip select ($\overline{CS}$) is low. The data I/O takes place on the data bus D0 thru D7. The map operation will output the contents of the map register selected by the map address inputs (MA0 thru MA3) when $\overline{CS}$ is high and $\overline{MM}$ (map mode control) is low. The 'LS612 and 'LS613 output stages are transparent in this mode, while the 'LS610 and 'LS611 outputs may be transparent or latched. When $\overline{CS}$ and $\overline{MM}$ are both high (pass mode), the address bits on MA0 thru MA3 appear at MO8–MO11, respectively, (assuming appropriate latch control) with low levels in the other bit positions of the map outputs.



functional block diagram (positive logic)



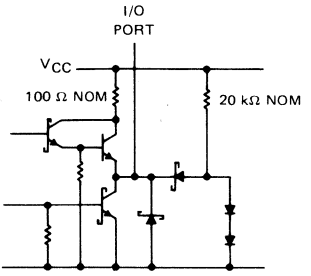
*'LS610 and 'LS612 have 3-state (▽) map outputs.
'LS611 and 'LS613 have open-collector (◇) map outputs.

PIN FUNCTION TABLE

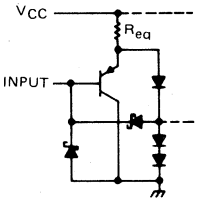
PIN	PIN NAME	FUNCTIONAL DESCRIPTION
7–12, 29–34	D0 thru D11	I/O connections to data and control bus used for reading from and writing to the map register selected by RS0–RS3 when $\overline{CS}$ is low. Mode controlled by R/$\overline{W}$.
36, 38, 1, 3	RS0 thru RS3	Register select inputs for I/O operations.
6	R/$\overline{W}$	Read or write control used in I/O operations to select the condition of the data bus. When high, the data bus outputs are active for reading the map register. When low, the data bus is used to write into the register.
5	$\overline{STROBE}$	Strobe input used to enter data into the selected map register during I/O operations.
4	$\overline{CS}$	Chip select input. A low input level selects the memory mapper (assuming more than one used) for an I/O operation.
35, 37, 39, 2	MA0 thru MA3	Map address inputs to select one of 16 map registers when in map mode ($\overline{MM}$ low and $\overline{CS}$ high).
14–19, 22–27	MO0 thru MO11	Map outputs. Present the map register contents to the system memory address bus in the map mode. In the pass mode, these outputs provide the map address data on MO8–MO11 and low levels on MO0–MO7.
13	$\overline{MM}$	Map mode input. When low, 12 bits of data are transferred from the selected map register to the map outputs. When high (pass mode), the 4 bits present on the map address inputs MA0-MA3 are passed to the map outputs MO8-MO11, respectively, while MO0-MO7 are set low.
21	$\overline{ME}$	Map enable for the map outputs. A low level allows the outputs to be active while a high input level puts the outputs at high impedance.
28	C	Latch enable input for the 'LS610 and 'LS611 (no internal connection for 'LS612 and 'LS613). A high level will transparently pass data to the map outputs. A low level will latch the outputs.
40, 20	V_{CC}, GND	5-V power supply and network ground (substrate) pins.

schematics of inputs and outputs

INPUT/OUTPUT PORTS, D0-D11

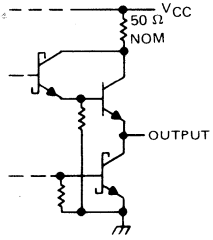


EQUIVALENT OF OTHER INPUTS

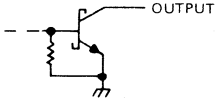


$\overline{MM}$: R_{eq} = 7 kΩ NOM
RS, $\overline{STROBE}$: R_{eq} = 9 kΩ NOM
$\overline{CS}$, R/$\overline{W}$, MA: R_{eq} = 6 kΩ nom

TYPICAL OF MAP OUTPUTS ('LS610, 'LS612)



TYPICAL OF MAP OUTPUTS ('LS611, 'LS613)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage:	Data Bus I/O	5.5 V
	All other inputs	7 V
Operating free-air temperature range:	SN54LS610 through SN54LS613	−55°C to 125°C
	SN74LS610 through SN74LS613	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	MO			−12			−15	mA
	D			−1			−2.6	
Low-level output current, I_{OL}	MO			12			24	mA
	D			4			8	
Width of strobe input pulse, t_{SLSH}	See Figure 1	75			75			ns
$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low), t_{CSLSL}		20			20			ns
R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low), t_{WLSL}		20			20			ns
RS setup time (RS valid to strobe low), t_{RVSL}		20			20			ns
Data setup time (D0-D11 valid to strobe high), t_{DVSH}		75			75			ns
$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high), t_{SHCSH}		20			20			ns
R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high), t_{SHWH}		20			20			ns
RS hold time (Strobe high to RS invalid), t_{SHRX}		20			20			ns
Data hold time (Strobe high to D0-D11 invalid), t_{SHDX}		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS610 SN54LS612			SN74LS610 SN74LS612			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input calmp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4			2.4			V
				I_{OH} = MAX	2			2			
		D		I_{OH} = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		D		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	MO	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 0.4 V				−20			−20	μA
		D					−400			−400	
I_I	Input current at maximum input voltage	D	V_{CC} = MAX	V_I = 5.5 V			100			100	μA
		All others		V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	MO	V_{CC} = MAX		−40		−225	−40		−225	mA
		D			−30		−130	−30		−130	
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		112	180		112	180	mA
				Outputs low		112	180		112	180	
				Outputs at high impedance		150	230		180	230	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS610			'LS612			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}$↓	D 0-11			28	50		26	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}$↑	D 0-11	R_L = 2 kΩ		20	35		20	35	ns
t_{RVDV}	Access time	RS	D 0-11	See Figure 1,		49	75		39	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}$↓	D 0-11	See Note 2		32	50		30	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}$↑	D 0-11			42	65		38	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}$↓	MO 0-11			19	30		17	30	ns
t_{CSHQV}	Access time	$\overline{CS}$↑	MO 0-11			56	85		48	85	ns
t_{MLQV}	Access time	$\overline{MM}$↓	MO 0-11	R_L = 667 Ω,		25	40		22	40	ns
t_{CHQV}	Access time	C↑	MO 0-11	See Figure 2,		24	40				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO 0-11	See Note 2		46	70		39	70	ns
t_{MHQV}	Access time	$\overline{MM}$↑	MO 0-11			24	40		22	40	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO 8-11			19	30		13	30	ns
t_{EHQZ}	Disable time	$\overline{ME}$↑	MO 0-11			14	25		14	25	ns

NOTE 2 For load circuits and measurement points, see page 3-11

Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

explanation of letter symbols

This data sheet uses a new type of letter symbol to describe time intervals. The format is:

$$t_{AB\text{-}CD}$$

where: subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval.

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state.

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur. For these letter symbols on this data sheet, the signal names are further abbreviated as follows:

SIGNAL NAME	B or D SUBSCRIPT
C	C
$\overline{CS}$	CS
D0–11	D
MA0–MA3	A
MO0–MO11	Q
$\overline{ME}$	E
$\overline{MM}$	M
R/$\overline{W}$	W
RS0–RS3	R
$\overline{STROBE}$	S

recommended operating conditions

		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	MO			5.5			5.5	V
High-level output current, I_{OH}	D			−1			−2.6	mA
Low-level output current, I_{OL}	MO			12			24	mA
	D			4			8	
Width of strobe input pulse, t_{SLSH}	See Figure 1	75			75			ns
$\overline{CS}$ setup time ($\overline{CS}$ low to strobe low), t_{CSLSL}		20			20			ns
R/$\overline{W}$ setup time (R/$\overline{W}$ low to strobe low), t_{WLSL}		20			20			ns
RS setup time (RS valid to strobe low), t_{RVSL}		20			20			ns
Data setup time (D0-D11 valid to strobe high), t_{DVSH}		75			75			ns
$\overline{CS}$ hold time (Strobe high to $\overline{CS}$ high), t_{SHCSH}		20			20			ns
R/$\overline{W}$ hold time (Strobe high to R/$\overline{W}$ high), t_{SHWH}		20			20			ns
RS hold time (Strobe high to RS invalid), t_{SHRX}		20			20			ns
Data hold time (Strobe high to D0-D11 invalid), t_{SHDX}		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 2: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS611 SN54LS613			SN74LS611 SN74LS613			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	D	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4			2.4			
I_{OH}	High-level output current	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	MO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		D		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	D	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	D	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−400			−400	
I_I	Input current at maximum input voltage	D	V_{CC} = MAX	V_I = 5.5 V			100			100	
		All others		V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	D	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX	Outputs high		100	170		100	170	mA
				Outputs low		100	170		100	170	
				Outputs at high impedance		110	200		110	200	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF to GND

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS611			'LS613			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{CSLDV}	Access (enable) time	$\overline{CS}\downarrow$	D 0-11			31	50		28	50	ns
t_{WHDV}	Access (enable) time	R/$\overline{W}\uparrow$	D 0-11	R_L = 2 kΩ,		23	35		21	35	ns
t_{RVDV}	Access time	RS	D 0-11	See Figure 1,		51	75		47	75	ns
t_{WLDZ}	Disable time	R/$\overline{W}\downarrow$	D 0-11	See Note 2		32	50		31	50	ns
t_{CSHDZ}	Disable time	$\overline{CS}\uparrow$	D 0-11			41	65		40	65	ns
t_{ELQV}	Access (enable) time	$\overline{ME}\downarrow$	MO 0-11			21	30		19	30	ns
t_{CSHQV}	Access time	$\overline{CS}\uparrow$	MO 0-11			57	90		53	90	ns
t_{MLQV}	Access time	MM↓	MO 0-11	R_L = 667 Ω,		25	40		25	40	ns
t_{CHQV}	Access time	C↑	MO 0-11	See Figure 2,		30	45				ns
t_{AVQV1}	Access time ($\overline{MM}$ low)	MA	MO 0-11	See Note 2		47	70		44	70	ns
t_{MHQV}	Access time	MM↑	MO 0-11			31	50		31	50	ns
t_{AVQV2}	Propagation time ($\overline{MM}$ high)	MA	MO 8-11			21	30		20	30	ns
t_{EHQZ}	Disable time	$\overline{ME}\uparrow$	MO 0-11			15	25		15	25	ns

NOTE 2 For load circuits and measurement points, see page 3-11 of *The TTL Data Book* for *Design Engineers*, second edition, LCC 4112. Access times are tested as t_{PLH} and t_{PHL} or t_{PZH} or t_{PZL}. Disable times are tested as t_{PHZ} and t_{PLZ}.

TIMING DIAGRAMS

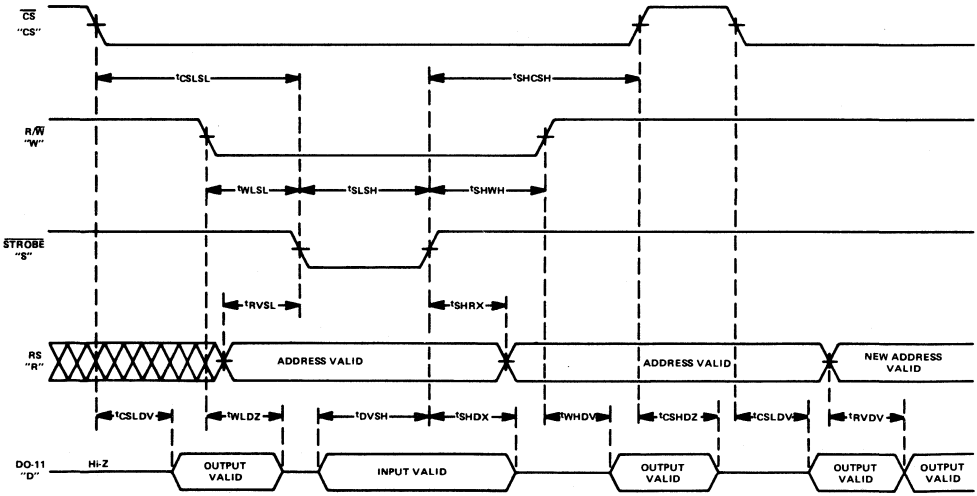


FIGURE 1–WRITE AND READ MODES

TIMING DIAGRAMS

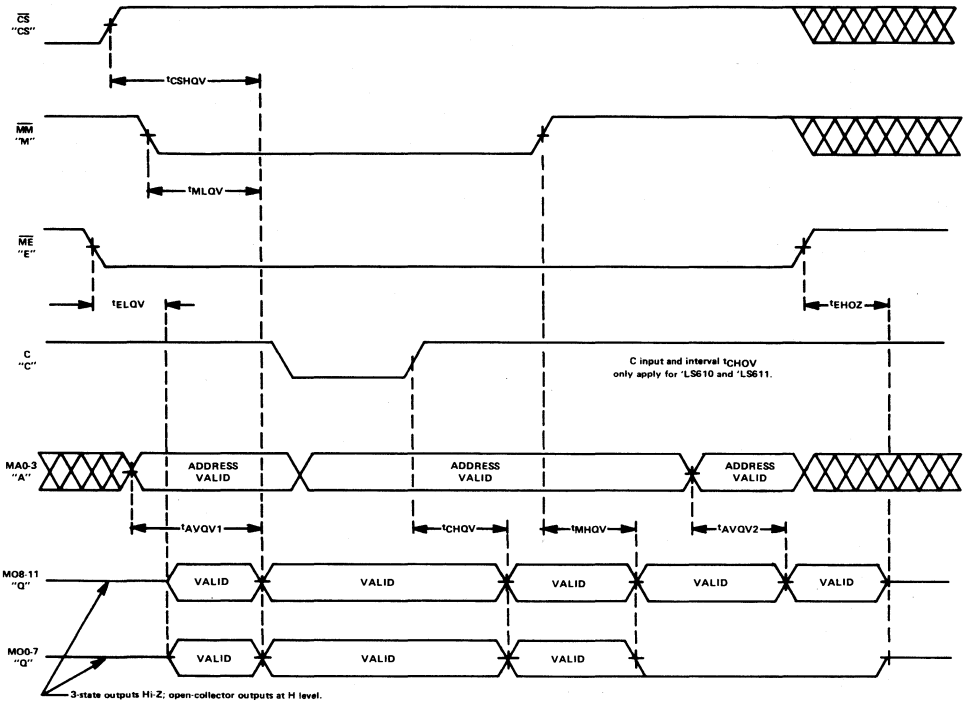


FIGURE 2–MAP AND PASS MODES

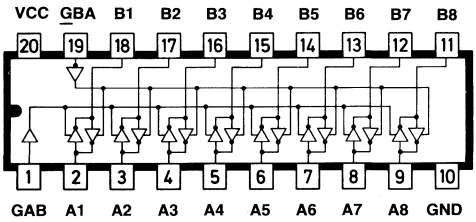
TYPES SN54LS620 THRU SN54LS623, SN74LS620 THRU SN74LS623 OCTAL BUS TRANSCEIVERS

D2537, AUGUST 1979

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Local Bus-Latch Capability
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

DEVICE	OUTPUT	LOGIC
'LS620	3-State	Inverting
'LS621	Open-Collector	True
'LS622	Open-Collector	Inverting
'LS623	3-State	True

SN54LS' . . . J PACKAGE
SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 'LS620 thru 'LS623 the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'LS621 and 'LS623 devices or complementary for the 'LS620 and 'LS622.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}$BA	GAB	'LS620, 'LS622	'LS621, 'LS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

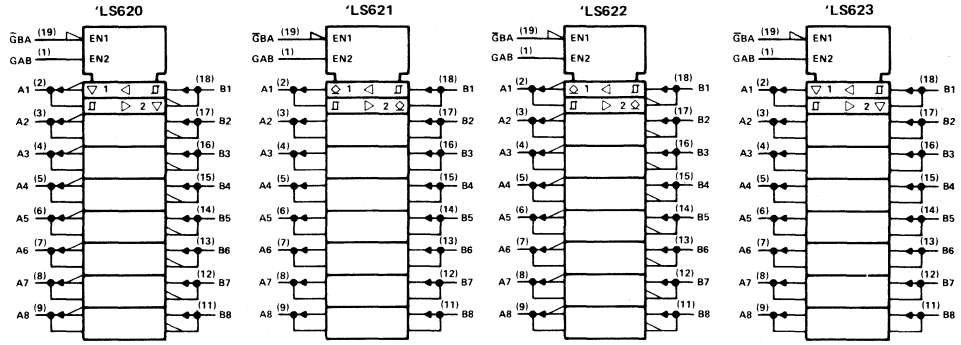
H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

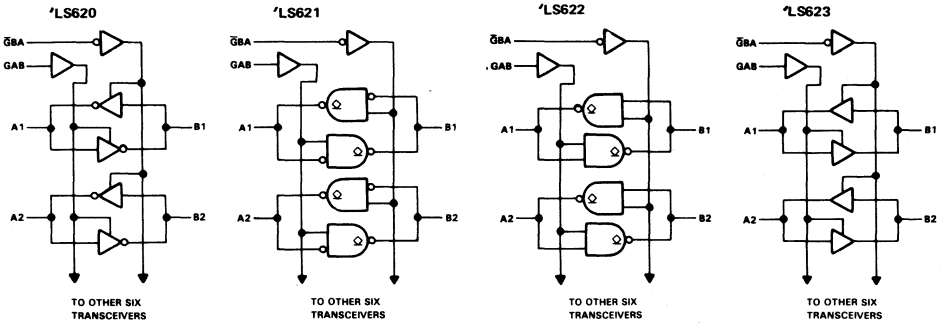
NOTE 1: Voltage values are with respect to network ground terminal.

logic symbols

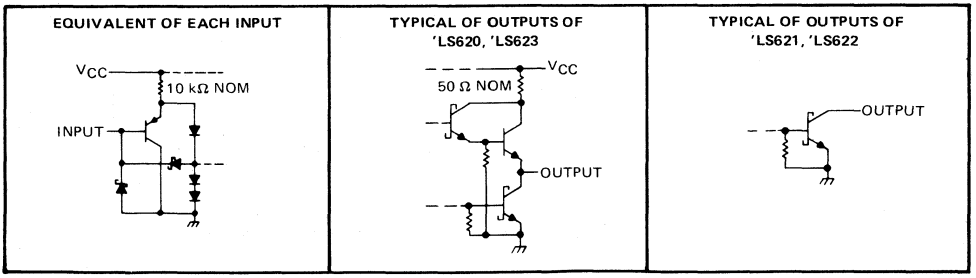


functional block diagrams (positive logic)

¼ 'LS620, ¼ 'LS622 ¼ 'LS621, ¼ 'LS623



schematics of inputs and outputs



recommended operating conditions

PARAMETER	SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS620 SN54LS623			SN74LS620 SN74LS623			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		$\overline{G}$BA or GAB		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS620			'LS623			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		8	15	ns
		B	A			6	10		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		11	15	ns
		B	A			8	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$BA	A			31	40		31	40	ns
		GAB	B			31	40		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$BA	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25	ns
		GAB	B			15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$BA	A			15	25		15	25	ns
		GAB	B			15	25		15	25	

NOTE 2: For load circuit and voltage waveforms see page 3-11.
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PZH} = Output enable time to high level
t_{PZL} = Output enable time to low level
t_{PHZ} = Output disable time from high level
t_{PLZ} = Output disable time from low level

recommended operating conditions

PARAMETER	SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS621 SN54LS622			SN74LS621 SN74LS622			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Outputs low				62	90		62	90	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS621			'LS622			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25	ns
		B	A			17	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25	ns
		B	A			16	25		14	25	
t_{PLH}	Output disable time from low level	$\overline{G}$BA	A			23	40		26	40	ns
		GAB	B			25	40		28	40	
t_{PHL}	Output disable time from high level	$\overline{G}$BA	A			34	50		43	60	ns
		GAB	B			37	50		39	60	

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11
t_{PLH} ≡ Propagation delay time, low-to-high-level input.
t_{PHL} ≡ Propagation delay time, high-to-low-level input.

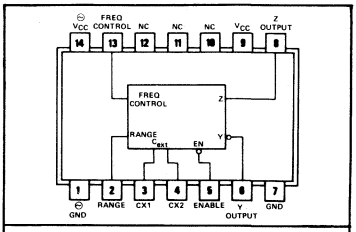
TYPES SN54LS624 THRU SN54LS629, SN74LS624 THRU SN74LS629 VOLTAGE-CONTROLLED OSCILLATORS

D2501, JANUARY 1980 – REVISED OCTOBER 1980

- **Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Output Circuitry**
- **Highly Stable Operation over Specified Temperature and/or Supply Voltage Ranges**

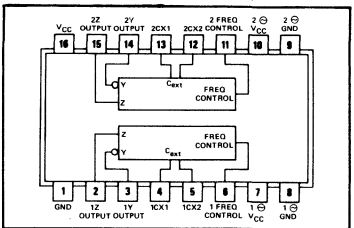
DEVICE TYPE	SIMILAR TO	NUMBER VCO's	COMP'L Z OUT	ENABLE	RANGE INPUT†	R_{ext}
'LS624	'LS324	single	yes	yes	yes	no
'LS625	'LS325	dual	yes	no	no	no
'LS626	'LS326	dual	yes	yes	no	no
'LS627	'LS327	dual	no	no	no	no
'LS628	'LS324	single	yes	yes	yes	yes
'LS629	'LS124	dual	no	yes	yes	no

SN54LS' . . . J OR W PACKAGE
SN74LS' . . . J OR N PACKAGE
'LS624 (TOP VIEW)



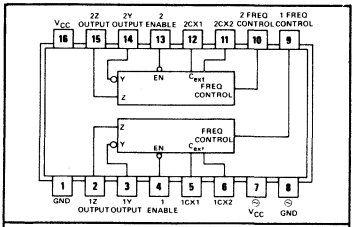
logic: see description

'LS625 (TOP VIEW)



logic: see description

'LS626 (TOP VIEW)



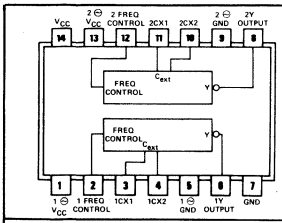
logic: see description

description

These voltage-controlled oscillators (VCO's) are improved versions of the original VCO family: SN54LS124, SN54LS324 thru SN54LS327, SN74LS124, and SN74LS324 thru SN74LS327. These new devices feature improved voltage-to-frequency linearity, range, and compensation. With the exception of the 'LS624 and 'LS628, all of these devices feature two independent VCO's in a single monolithic chip. The 'LS624, 'LS625, 'LS626 and 'LS628 have complementary Z outputs. The output frequency for each VCO is established by a single external capacitor in combination with voltage-sensitive inputs used for frequency control and frequency range. Each device has a voltage-sensitive input for frequency control; however, the 'LS624, 'LS628, and 'LS629 devices also have one for frequency range. (See Figures 1 thru 6).

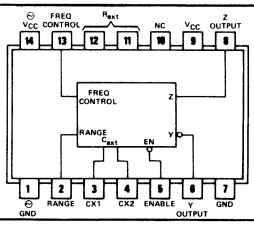
The 'LS628 features two $R_{external}$ pins that can offer more precise temperature compensation than its 'LS624 counterpart.

'LS627 (TOP VIEW)



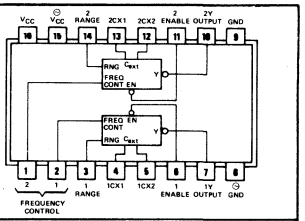
logic: see description

'LS628 (TOP VIEW)



logic: see description

'LS629 (TOP VIEW)



logic: see description

NC—No internal connection

Figure 3 and Figure 6 contain the necessary information to choose the proper capacitor value to obtain the desired operating frequency.

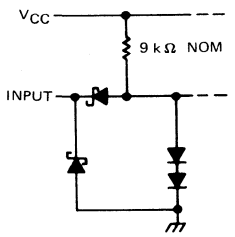
A single 5-volt supply can be used; however, one set of supply voltage and ground pins (V_{CC} and Gnd) is provided for the enable, synchronization-gating, and output sections, and a separate set ($\ominus V_{CC}$ and $\ominus$Gnd) is provided for the oscillator and associated frequency-control circuits so that effective isolation can be accomplished in the system. For operation of frequencies greater than 10 MHz, it is recommended that two independent supplies be used. Disabling either VCO of the 'LS625 and 'LS627 can be achieved by removing the appropriate $\ominus V_{CC}$. An enable input is provided on the 'LS624, 'LS626, 'LS628 and 'LS629. When the enable input is low the output is enabled: when the enable input is high, the internal oscillator is disabled, Y is high, and Z is low. Caution! Crosstalk may occur in the dual devices ('LS625, 'LS626, 'LS627, and 'LS629) when both VCO's are operated simultaneously.

The pulse-synchronization-gating section ensures that the first output pulse is neither clipped nor extended. The duty cycle of the square-wave output is fixed at approximately 50 percent.

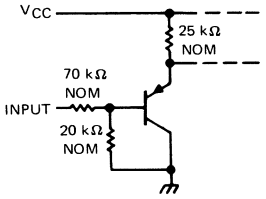
The SN54LS624 thru SN54LS629 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS624 thru SN74LS629 are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

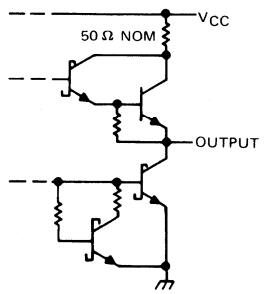
EQUIVALENT OF EACH ENABLE INPUT ('LS624, 'LS626, 'LS628, AND 'LS629)



EQUIVALENT OF EACH FREQUENCY CONTROL OR ('LS624, 'LS628, AND 'LS629) RANGE INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 2)	7 V
Input voltage: Enable input♦	7 V
Frequency control or range input▲	V_{CC}
Operating free-air temperature range: SN54LS' Circuits	−55°C to 125°C
SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

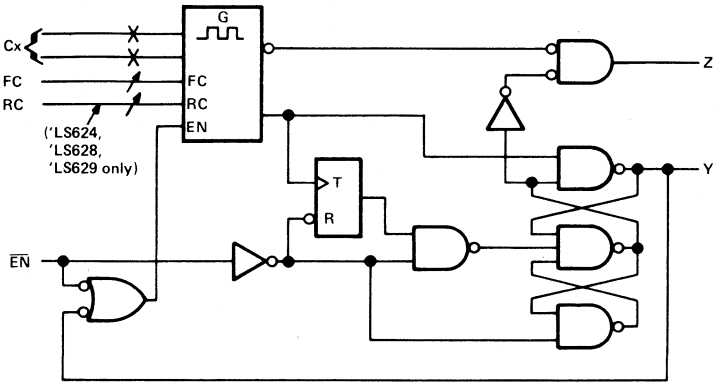
♦The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

▲The range input is provided only on 'LS624, 'LS628, and 'LS629.

NOTES: 1. Voltage values are with respect to the appropriate ground terminal.

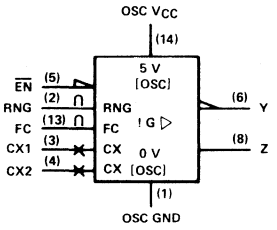
2. Throughout this data sheet, the symbol V_{CC} is used for the voltage applied to both the V_{CC} and $\ominus$ V_{CC} terminals, unless otherwise noted.

functional block diagram (positive logic)

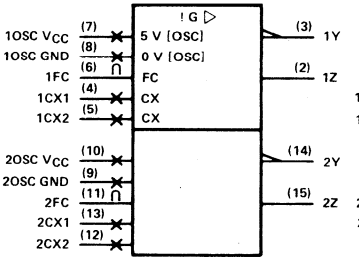


logic symbols¶

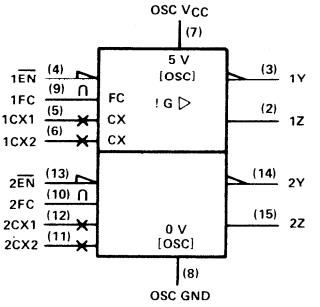
'LS624



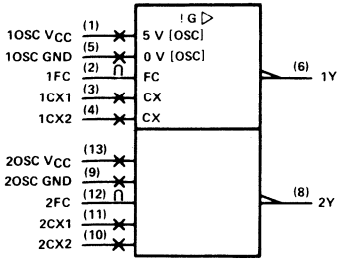
'LS625



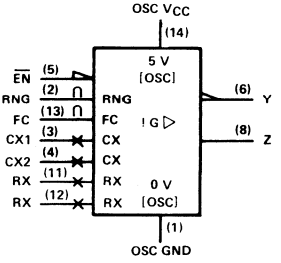
'LS626



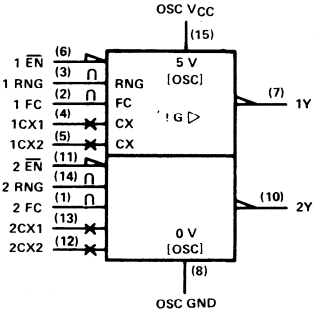
'LS627



'LS628



'LS629



recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input voltage at frequency control or range input, $V_{I(freq)}$ or $V_{I(rng)}$▲	0		5	0		5	V
High-level output current, I_{OH}			−1.2			−1.2	mA
Low-level output current, I_{OL}			12			24	mA
Output frequency, f_o	1			1			Hz
			20			20	MHz
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage at enable◆				2			2			V
V_{IL}	Low-level input voltage at enable◆						0.7			0.8	V
V_{IK}	Input clamp voltage at enable◆		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −1.2 mA, $\overline{EN}$ at V_{IL} max, See Note 3		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, $\overline{EN}$ at V_{IL} max, See Note 3	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current	Freq control or range ▲	V_{CC} = MAX	V_I = 5 V		50	250		50	250	μA
				V_I = 1 V		10	50		10	50	
I_I	Input current at maximum input voltage	Enable◆	V_{CC} = MAX, V_I = 7 V				0.2			0.2	mA
I_{IH}	High-level input current	Enable◆	V_{CC} = MAX, V_I = 2.7 V				40			40	μA
I_{IL}	Low-level input current	Enable◆	V_{CC} = MAX, V_I = 0.4 V				−0.8			−0.8	mA
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current, total into V_{CC} and ⏦ V_{CC} pins		V_{CC} = MAX, Enable◆ = 4.5 V, See Note 4	'LS624		20	35		20	35	mA
				'LS625		35	55		35	55	
				'LS626		35	55		35	55	
				'LS627		35	55		35	55	
				'LS628		20	35		20	35	
				'LS629		35	55		35	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

▲The range input is provided only on the 'LS624, 'LS628, and 'LS629.

◆The enable input is provided only on the 'LS624, 'LS626, 'LS628, and 'LS629.

NOTES: 3. V_{OH} for Y outputs and V_{OL} for Z outputs are measured while enable inputs are connected to ground, with individual 1-kΩ resistors connected from CX1 to V_{CC} and from CX2 to ground. The resistor connections are reversed for testing V_{OH} for Z outputs and V_{OL} for Y inputs.

4. For 'LS624, 'LS626, 'LS628, and 'LS629, I_{CC} is measured with the outputs disabled and open. For 'LS625 and 'LS627, I_{CC} is measured with one ⏦ V_{CC} = MAX, and with the other ⏦ V_{CC} and outputs open.

switching characteristics, V_{CC} = 5 V (unless otherwise noted), R_L = 667 Ω, C_L = 45 pF, T_A = 25 °C

PARAMETER		TEST CONDITIONS		'LS624, 'LS628, 'LS629			'LS625, 'LS626, 'LS627			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_O	Output frequency	C_{ext} = 50 pF	$V_{I(freq)}$ = 5 V, $V_{I(rng)}$ = 0 V	15	20	25				MHz
			$V_{I(freq)}$ = 0 V, $V_{I(rng)}$ = 5 V	0.7	1	1.3				
			$V_{I(freq)}$ = 5 V				7	9.5	12	
			$V_{I(freq)}$ = 0 V				0.9	1.2	1.5	

TYPICAL CHARACTERISTICS

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

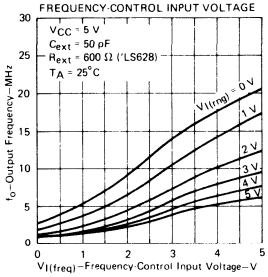


FIGURE 1

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

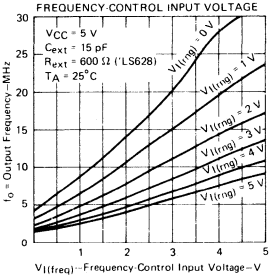


FIGURE 2

'LS624, 'LS628, 'LS629
OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

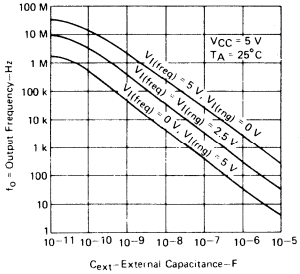


FIGURE 3

TYPICAL CHARACTERISTICS

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

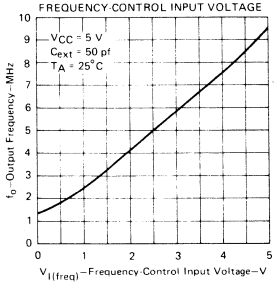


FIGURE 4

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
FREQUENCY-CONTROL INPUT VOLTAGE

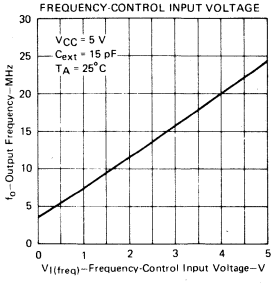


FIGURE 5

'LS625, 'LS626, 'LS627
OUTPUT FREQUENCY
vs
EXTERNAL CAPACITANCE

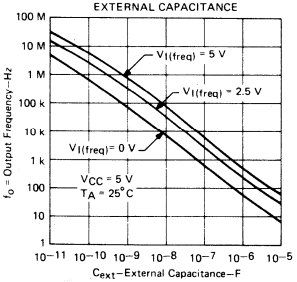


FIGURE 6

ENABLE TIME
vs
FREQUENCY

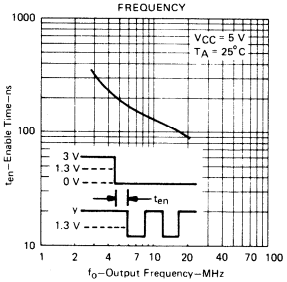


FIGURE 7

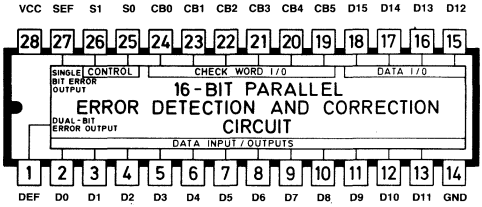
TYPES SN54LS630, SN54LS631, SN74LS630, SN74LS631
16-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

D2550, MARCH 1980

(TIM99630, TIM99631)

- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- Fast Processing Times:
  - Write Cycle: Generates Check Word in 45 ns Typical
  - Read Cycle: Flags Errors in 27 ns Typical
- Power Dissipation 600 mW Typical
- Choice of Output Configurations:
  - 'LS630 . . . 3-State
  - 'LS631 . . . Open-Collector

SN54LS' . . . J PACKAGE
SN74LS' . . . N PACKAGE
(TOP VIEW)



description

The 'LS630 and 'LS631 devices are 16-bit parallel error detection and correction circuits (EDACs) in 28-pin, 600-mil packages. They use a modified Hamming code to generate a 6-bit check word from a 16-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 22-bit words from memory are processed by the EDACs to determine if errors have occurred in memory.

Single-bit errors in the 16-bit data word are flagged and corrected.

Single-bit errors in the 6-bit check word are flagged, and the CPU sends the EDAC through the correction cycle even though the 16-bit word is not in error. The correction cycle will simply pass along the original 16-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

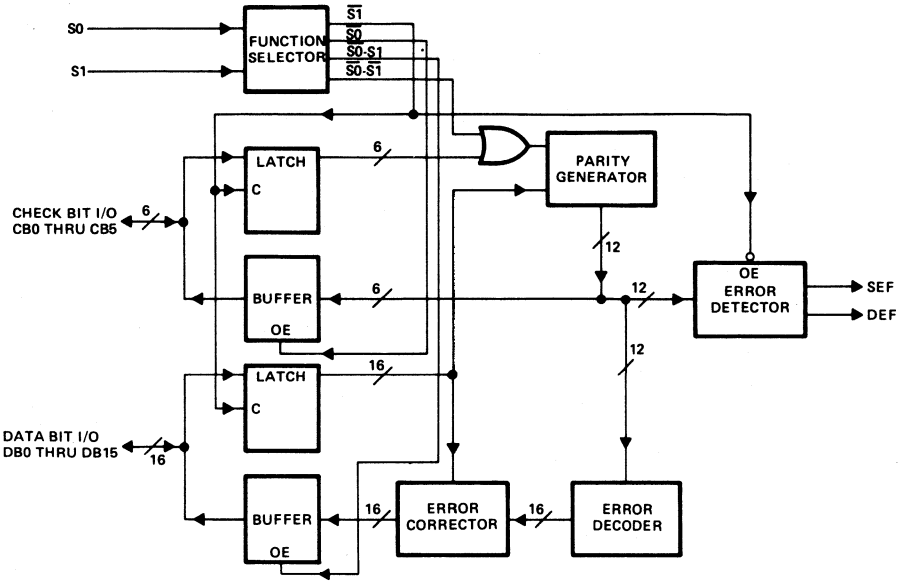
Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 22-bit word from memory (two errors in the 16-bit data word, two errors in the 6-bit check word, or one error in each word).

The gross-error condition of all lows or all highs from memory will be detected. Otherwise, errors in three or more bits of the 22-bit word are beyond the capabilities of these devices to detect.

CONTROL FUNCTION TABLE

Memory Cycle	Control S1	Control S0	EDAC Function	Data I/O	Check Word I/O	Error Flags SEF	Error Flags DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

functional block diagram



ERROR FUNCTION TABLE

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 16-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

error detection and correction details

During a memory write cycle, six check bits (CB0-CB5) are generated by eight-input parity generators using the data bits as defined below. During a memory read cycle, the 6-bit check word is retrieved along with the actual data.

CHECKWORD	16-BIT DATA WORD															
BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	x	x		x	x				x	x	x			x		
CB1	x		x	x		x	x		x			x			x	
CB2		x	x		x	x		x		x			x			x
CB3	x	x	x				x	x			x	x	x			
CB4				x	x	x	x	x						x	x	x
CB5									x	x	x	x	x	x	x	x

The six check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit.

Error detection is accomplished as the 6-bit check word and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16-bit data word will change the sense of exactly three bits of the 6-bit check word. Any single error in the 6-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, or an uncorrectable error has occurred and produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit data word and 6-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

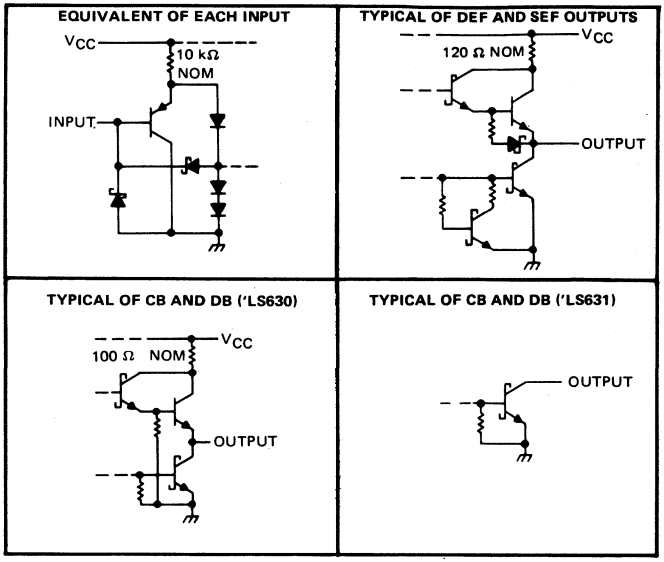
As the corrected word is made available on the data word I/O port, the check word I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the bad memory chip.

ERROR SYNDROME TABLE

	SYNDROME ERROR CODE					
ERROR LOCATION	CB0	CB1	CB2	CB3	CB4	CB5
DB0	L	L	H	L	H	H
DB1	L	H	L	L	H	H
DB2	H	L	L	L	H	H
DB3	L	L	H	H	L	H
DB4	L	H	L	H	L	H
DB5	H	L	L	H	L	H
DB6	H	L	H	L	L	H
DB7	H	H	L	L	L	H
DB8	L	L	H	H	H	L
DB9	L	H	L	H	H	L
DB10	L	H	H	L	H	L
DB11	H	L	H	L	H	L
DB12	H	H	L	L	H	L
DB13	L	H	H	H	L	L
DB14	H	L	H	H	L	L
DB15	H	H	L	H	L	L
CB0	L	H	H	H	H	H
CB1	H	L	H	H	H	H
CB2	H	H	L	H	H	H
CB3	H	H	H	L	H	H
CB4	H	H	H	H	L	H
CB5	H	H	H	H	H	L
NO ERROR	H	H	H	H	H	H

REVISED OCTOBER 1983

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: S0 and S1 . . . . . 7 V
CB and DB . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS630, SN54LS631 . . . . . −55°C to 125°C
SN74LS630, SN74LS631 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS630 SN54LS631			SN74LS630 SN74LS631			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	CB or DB, 'LS630 only			−1			−1	mA
	DEF or SEF			−0.4			−0.4	
High-level output voltage, V_{OH}	CB or DB, 'LS631 only			5.5			5.5	V
Low-level output current, I_{OL}	CB or DB			12			24	mA
	DEF or SEF			4			8	
Setup time, t_{su}	CB or DB to S1↑	30			30			ns
Hold time, t_h	CB or DB after S1↑	15			15			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The upward-pointing arrow indicates a transition from low to high.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS630 MIN	SN54LS630 TYP‡	SN54LS630 MAX	SN74LS630 MIN	SN74LS630 TYP‡	SN74LS630 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} min	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		DEF or SEF		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 0.4 V,			−20			−20	μA
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		S0 or S1	V_{IH} = 4.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶	CB or DB	V_{CC} = MAX,		−30		−130	−30		−130	mA
		DEF or SEF			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB pins grounded, DEF and SEF open			143	230		143	230	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS631 MIN	SN54LS631 TYP‡	SN54LS631 MAX	SN74LS631 MIN	SN74LS631 TYP‡	SN74LS631 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	DEF or SEF	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −400 μA, V_{IL} = V_{IL} max	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	CB or DB	V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL} max			100			100	μA
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX,	V_I = 5.5 V			100			100	μA
		S0 or S1	V_{IH} = 4.5 V	V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current¶	DEF or SEF	V_{CC} = MAX,		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB grounded, SEF and DEF open			113	180		113	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS630 MIN	'LS630 TYP	'LS630 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output◇	DB	CB	S0 at 0 V, S1 at 0 V, R_L = 667 Ω, See Figure 1		31	45	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output*	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ, See Figure 1		27	40	ns
		SEF			20	30	
t_{PZH} Output enable time to high level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		24	40	ns
t_{PZL} Output enable time to low level#	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		30	45	ns
t_{PHZ} Output disable time from high level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		43	65	ns
t_{PLZ} Output disable time from low level▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		31	45	ns

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF, see Figure 1

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS631 MIN	'LS631 TYP	'LS631 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high level output◇	DB	CB	S0 at 0 V, S1 at 0V, R_L = 667 Ω		38	55	ns
t_{PHL} Propagation delay time, high-to-low-level output◇					45	65	ns
t_{PLH} Propagation delay time, low-to-high-level output*	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ		27	40	ns
		SEF			20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output#	S0↓	CB, DB	S1 at 3 V, R_L = 667 kΩ		28	45	ns
t_{PLH} Propagation delay time, low-to-high-level output▲	S0↑	CB, DB	S1 at 3 V, R_L = 667 kΩ		33	50	ns

◇These parameters describe the time intervals taken to generate the check word during the memory write cycle.
*These parameters describe the time intervals taken to flag errors during the memory read cycle.
#These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
▲These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

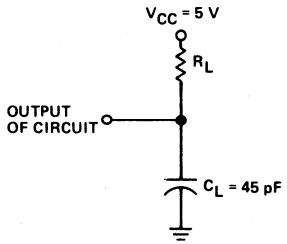


FIGURE 1–OUTPUT LOAD CIRCUIT

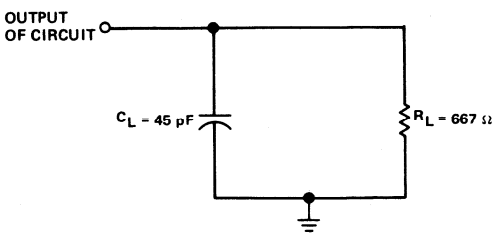
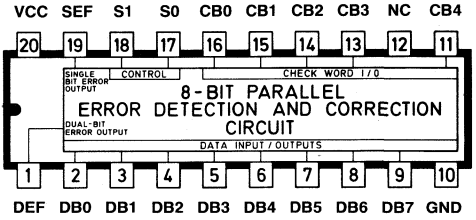


FIGURE 2–OUTPUT LOAD CIRCUIT

TYPES SN54LS636, SN54LS637, SN74LS636, SN74LS637
8-BIT PARALLEL ERROR DETECTION AND CORRECTION CIRCUITS

- **Detects and corrects Single-Bit Errors**
- **Detects and Flags Dual-Bit Errors**
- **Fast Processing Times:**
  Write Cycle: Generates Check word in 45 ns Typical
  Read Cycle: Flags Errors in 27 ns Typical
- **Power Dissipation 500 mW Typical**
- **Choice of Output Configurations:**
  'LS636 . . . 3-State
  'LS637 . . . Open-Collector

SN54LS'. . . J PACKAGE
SN74LS'. . . N PACKAGE
(TOP VIEW)



description

The 'LS636 and 'LS637 devices are 8-bit parallel error detection and correction circuits (EDACs) in 20-pin, 300-mil packages. They use a modified Hamming code to generate a 5-bit check word from an 8-bit data word. This check word is stored along with the data word during the memory write cycle. During the memory read cycle, the 13-bit words from memory are processed by the EDACs to determine if errors have occured in memory.

Single-bit errors in the 8-bit data word are flagged and corrected.

Single-bit errors in the 5-bit check word are flagged and the CPU sends the EDAC through the correction cycle even though the 8-bit data word is not in error. The correction cycle will simply pass along the original 8-bit word in this case and produce error syndrome bits to pinpoint the error-generating location.

Dual-bit errors are flagged but not corrected. These dual errors may occur in any two bits of the 13-bit word from memory (two errors in the 8-bit data word, two errors in the 5-bit check word, or one error in each word).

The gross-error condition of all highs from memory will be detected and flagged as a dual-bit error. Otherwise, errors in three or more bits of the 13-bit word are beyond the capabilities of these devices.

CONTROL FUNCTION TABLE

Memory Cycle	Control		EDAC Function	Data I/O	Check Word I/O	Error Flags	
	S1	S0				SEF	DEF
WRITE	L	L	Generate Check Word	Input Data	Output Check Word	L	L
READ	L	H	Read Data & Check Word	Input Data	Input Check Word	L	L
READ	H	H	Latch & Flag Errors	Latch Data	Latch Check Word	Enabled	
READ	H	L	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	

error detection and correction details

During a memory write cycle, five check bits (CB0-CB4) are generated by eight-input parity generators using the data bits as defined below. The five check bits are parity bits derived from the matrix of data bits as indicated by "x" for each bit.

CHECKWORD BIT	8-BIT DATA WORD							
	0	1	2	3	4	5	6	7
CB0	x	x		x	x			
CB1	x		x	x		x	x	
CB2		x	x		x	x		x
CB3	x	x	x				x	x
CB4				x	x	x	x	x

During a memory read cycle, the 5-bit check word is retrieved along with the actual data word and error detection is accomplished by applying the 13-bit word to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occured and both error flags will be low. (It should be noted that the sense of two of the check bits, bits CB0 and CB1, is inverted to ensure that the gross-error condition of all highs is detected.)

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 8-bit data word will change the sense of exactly three bits if the 5-bit check word. Any single error in the 5-bit check word changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify single-bit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors can fool the EDAC into believing that no error, a correctable error, on an uncorrectable error has occured and produce erroneous results in all three cases.

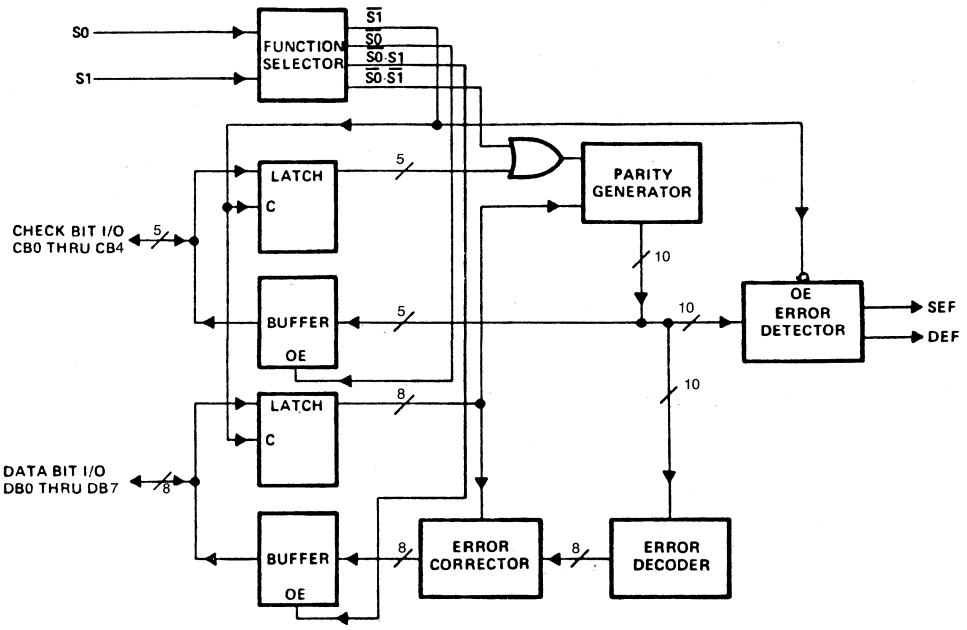
Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 8-bit data word and the 5-bit check word from memory with the new check word with one (check word error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the check word I/O port presents a 5-bit syndrom error code. This syndrome code can be used to identify the bad memory chip. (See the table below.)

ERROR SYNDROME TABLE

ERROR LOCATION	SYNDROME ERROR CODE				
	CB0	CB1	CB2	CB3	CB4
DB0	L	L	H	L	H
DB1	L	H	L	L	H
DB2	H	L	L	L	H
DB3	L	L	H	H	L
DB4	L	H	L	H	L
DB5	H	L	L	H	L
DB6	H	L	H	L	L
DB7	H	H	L	L	L
CB0	L	H	H	H	H
CB1	H	L	H	H	H
CB2	H	H	L	H	H
CB3	H	H	H	L	H
CB4	H	H	H	H	L
NO ERROR	H	H	H	H	H

functional block diagram



ERROR FUNCTION TABLE

Total Number of Errors		Error Rags		Data Correction
8-Bit Data	5-Bit Checkword	SEF	DEF	
0	0	L	L	Not Applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

In order to be able to determine whether the data from the memory is acceptable to use as presented to the bus, the EDAC must be strobed to enable the error flags and the flags will have to be tested for the zero condition.

The first case in the error function table represents the normal, no-error condition. The CPU sees lows on both flags. The next two cases of single-bit errors require data correction. Although the EDAC can discern the single check bit error and ignore it, the error flags are identical to the single error in the 8-bit data word. The CPU will ask for data correction in both cases. An interrupt condition to the CPU results in each of the last three cases, where dual errors occur.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS636			SN74LS636			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}min	I_{OH} = MAX	2.4	3.3		2.4	3.2		V
		DEF or SEF		I_{OH} = −400 μA	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	CB or DB	V_{CC} = MAX, S0 and S1 at 2 V	V_O = 0.4 V			−200			−200	μA
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		S0 or S1	V_{IH} = 4.5 V	V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	CB or DB	V_{CC} = MAX,		−30		−130	−30		−130	mA
		DEF or SEF			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB pins grounded, DEF and SEF open			100	160		100	160	mA

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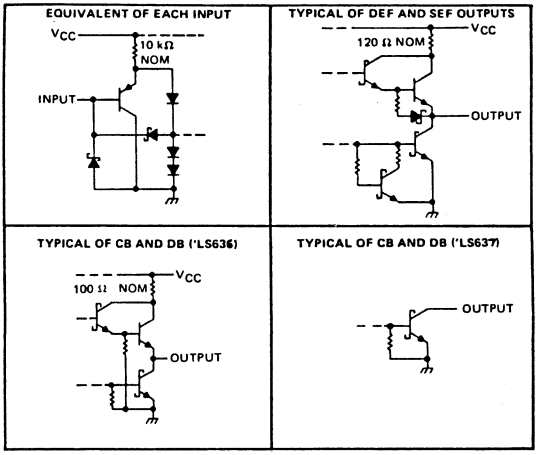
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS637			SN74LS637			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	DEF or SEF	V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −400 μA, V_{IL} = V_{IL}max	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current	CB or DB	V_{CC} = MIN, V_{IH} = 2 V,	V_{OH} = 5.5 V, V_{IL} = V_{IL}max			100			100	μA
V_{OL}	Low-level output voltage	CB or DB	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		DEF or SEF		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	CB or DB	V_{CC} = MAX,	V_I = 5.5 V			100			100	μA
		S0 or S1	V_{IH} = 4.5 V	V_I = 7 V			100			100	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current§	DEF or SEF	V_{CC} = MAX,		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, S0 and S1 at 4.5 V, All CB and DB pins grounded, DEF and SEF open			90	144		90	144	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: S0 and S1 . . . . . 7 V
CB and DB . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS636, SN54LS637 . . . . . −55°C to 125°C
SN74LS636, SN74LS637 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage Values are with respect to network ground terminal.

recommended operating conditions

		SN54LS636 SN54LS637			SN74LS636 SN74LS637			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	CB or DB, 'LS636 only			−1			−1	mA
	DEF or SEF			−0.4			−0.4	
High-level output voltage, V_{OH}	CB or DB, 'LS637 only			5.5			5.5	V
Low-level output current, I_{OL}	CB or DB			12			24	mA
	DEF or SEF			4			8	
Setup time, t_{su}	CB or DB to S1 ↑	10			10			ns
Hold timne, t_h	CB or DB after S1 ↑	15			15			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

† *The upward pointing arrow indicates a transition from low to high.*

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS636 MIN	'LS636 TYP	'LS636 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output*	DB	CB	S0 at 0 V, S1 at 0 V, R_L = 667 Ω, See Figure 1		31	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output*					45	65	ns
t_{PLH}	Propagation delay time, low-to-high-level output†	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ, See Figure 1		27	40	ns
			SEF			20	30	
t_{PZH}	Output enable time to high level§	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		24	40	ns
t_{PZL}	Output enable time to low level§	S0↓	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		30	45	ns
t_{PHZ}	Output disable time from high level●	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 2		43	65	ns
t_{PLZ}	Output disable time from low level●	S0↑	CB, DB	S1 at 3 V, R_L = 667 Ω, See Figure 1		31	45	ns

switching characteristics, V_{CC} = 5 V, T_A = 25°C, C_L = 45 pF, see Figure 1

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS637 MIN	'LS637 TYP	'LS637 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output*	DB	CB	S0 at 0 V, S1 at 0 V, R_L = 667 Ω,		38	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output*					45	65	ns
t_{PLH}	Propagation delay time, low-to-high-level output†	S1↑	DEF	S0 at 3 V, R_L = 2 kΩ,		27	40	ns
			SEF			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output§	S0↓	CB, DB	S1 at 3 V, R_L = 667 kΩ,		28	45	ns
t_{PLH}	Propagation delay time, low-to-high-level output●	S0↑	CB, DB	S1 at 3 V, R_L = 667 kΩ,		33	50	ns

* These parameters describe the time intervals taken to generate the check word during the memory write cycle.
† These parameters describe the time intervals taken to flag errors during the memory read cycle.
§ These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
● These parameters describe the time intervals taken to disable the CB and DB buses in preparation for a new data word during the memory read cycle.

PARAMETER MEASUREMENT INFORMATION

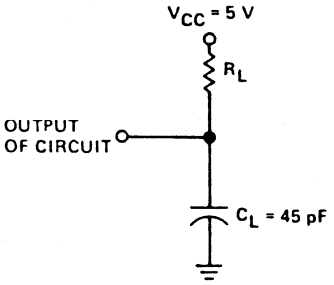


FIGURE 1-OUTPUT LOAD CIRCUIT

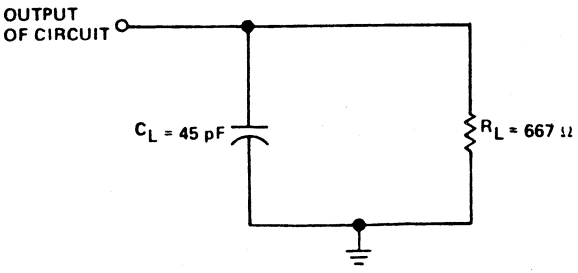


FIGURE 2-OUTPUT LOAD CIRCUIT

TYPES SN54LS638, SN54LS639, SN74LS638, SN74LS639
OCTAL BUS TRANSCEIVERS

D2636, JANUARY 1981

- Bidirectional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- A Bus Outputs are Open-Collector, B Bus Outputs are 3-State

description

These octal bus transceivers are designed for asynchronous two-way communication between open-collector and 3-state buses. The devices transmit data from the A bus (open-collector) to the B bus (3-state) or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so the buses are isolated.

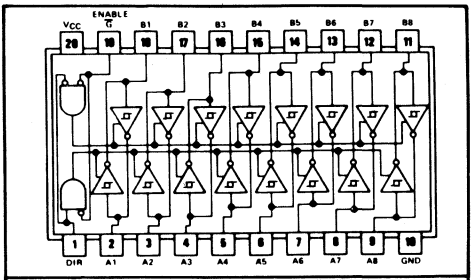
FUNCTION TABLE

CONTROL INPUTS		OPERATION	
$\overline{G}$	DIR	'LS638	'LS639
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

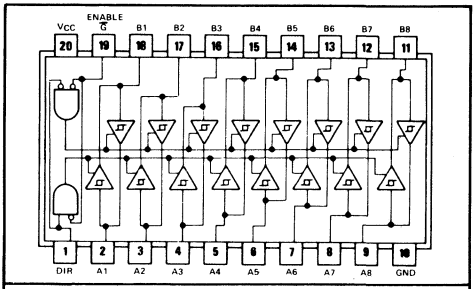
DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS638	Open-Collector	3-State	Inverting
'LS639	Open-Collector	3-State	True

SN54LS638 . . J PACKAGE
SN74LS638 . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

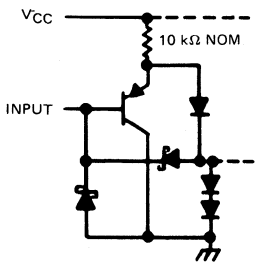
SN54LS639 . . J PACKAGE
SN74LS639 . . J OR N PACKAGE
(TOP VIEW)



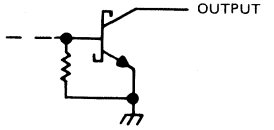
positive logic: see functional table

schematics of inputs and outputs

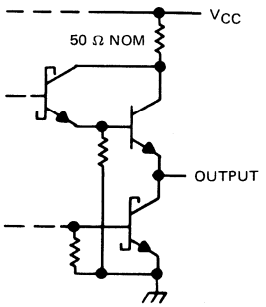
EQUIVALENT OF EACH INPUT



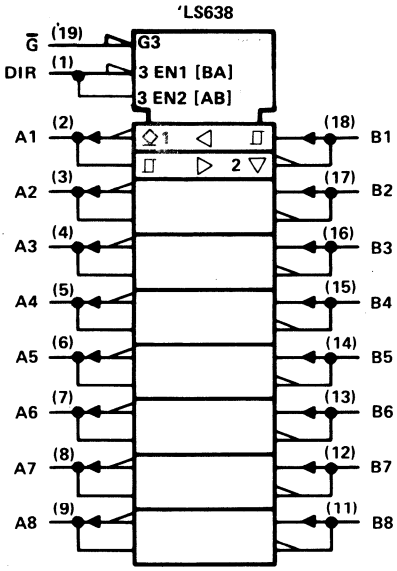
TYPICAL OF A OUTPUTS

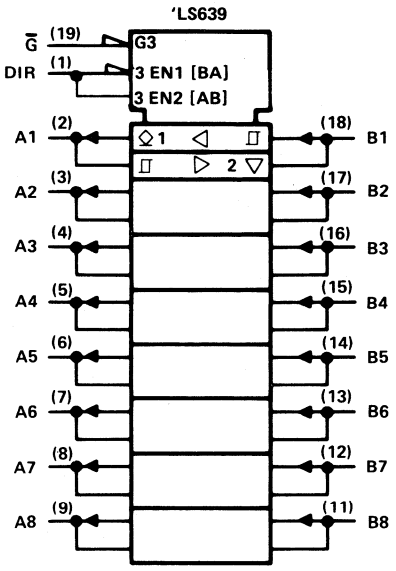


TYPICAL OF B OUTPUTS



logic symbols





7

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (DIR or $\overline{G}$) . . . . . 7 V
Off-state output voltage (A or B) . . . . . 5.5 V
Operating free-air temperature range: SN54LS638, SN54LS639 . . . . . −55°C to 125°C
SN74LS638, SN74LS639 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH} (A bus)			5.5			5.5	V
High-level output current, I_{OH} (B bus)			−12			−15	mA
Low-level output current, I_{OL} (A or B bus)			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+}-V_{T-}$)		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current	A	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL}=V_{IL}$ max, V_{OH} = 5.5 V				100			100	μA
V_{OH}	High-level output voltage	B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4			2.4			V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	A or B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	B	V_{CC} = MIN, $\overline{G}$ at 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current low-level voltage applied	A or B	V_{CC} = MIN, $\overline{G}$ at 2 V,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	B	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, Outputs open			48	70		48	70	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, Outputs open			62	90		62	90	mA
I_{CCZ}	Supply current, outputs off		V_{CC} = MAX, Outputs open			64	95		64	95	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS638			'LS639			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	B	C_L = 45 pF, R_L = 667 Ω		6	10		8	15	ns
	B	A			17	25		19	25	
t_{PHL}	A	B			8	15		11	15	ns
	B	A			14	25		16	25	
t_{PLH}	$\overline{G}$, DIR	A			26	40		23	40	ns
t_{PHL}	$\overline{G}$, DIR	A			43	60		34	50	ns
t_{PZH}	$\overline{G}$, DIR	B			23	40		26	40	ns
t_{PZL}	$\overline{G}$, DIR	B			31	40		31	40	ns
t_{PHZ}	$\overline{G}$, DIR	B	C_L = 5 pF, R_L = 667 Ω		15	25		15	25	ns
t_{PLZ}	$\overline{G}$, DIR	B			15	25		15	25	ns

NOTE 2: Load circuit and voltage waveforms are shown on page 3-11
t_{PLH} ≡ Propagation delay time, low-to-high-level input.
t_{PHL} ≡ Propagation delay time, high-to-low-level input.
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

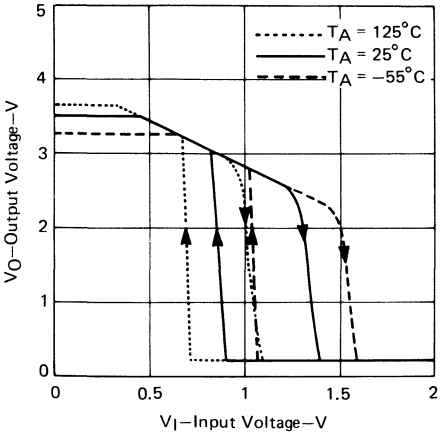


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

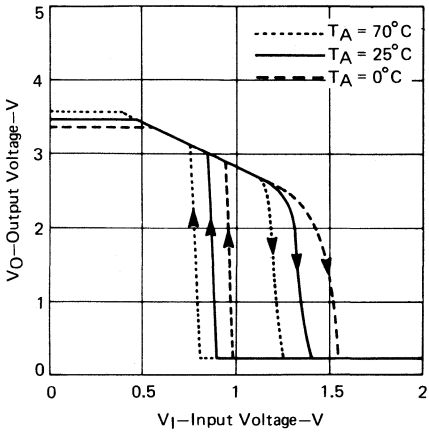


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

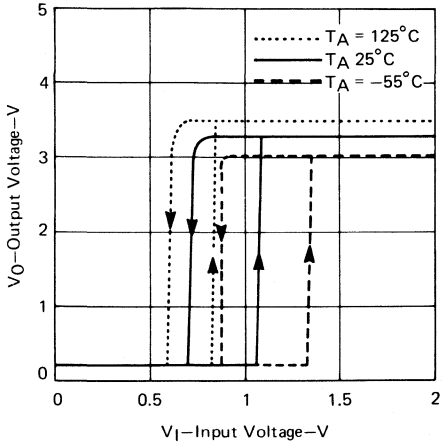


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

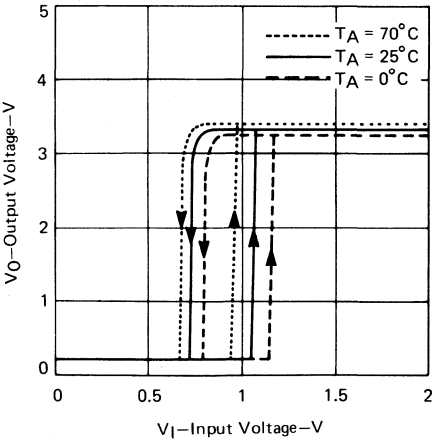


FIGURE 4

TYPES SN54LS640 THRU SN54LS645, SN74LS640 THRU SN74LS645 OCTAL BUS TRANSCEIVERS

D2420, APRIL 1979

- SN74LS64X-1 Versions Rated at I_{OL} of 48 mA
- Bi-directional Bus Transceivers in High-Density 20-Pin Packages
- Hysteresis at Bus Inputs Improves Noise Margins
- Choice of True or Inverting Logic
- Choice of 3-State or Open-Collector Outputs

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

DEVICE	OUTPUT	LOGIC
'LS640	3-State	Inverting
'LS641	Open-Collector	True
'LS642	Open-Collector	Inverting
'LS643	3-State	True and inverting
'LS644	Open-Collector	True and inverting
'LS645	3-State	True

FUNCTION TABLE

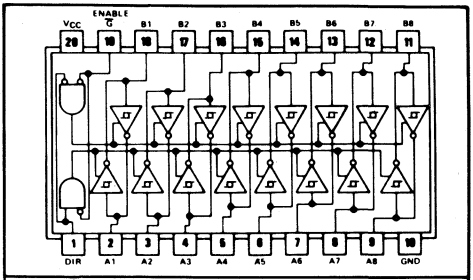
CONTROL INPUTS		OPERATION		
$\overline{G}$	DIR	'LS640 'LS642	'LS641 'LS645	'LS643 'LS644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

H = high level, L = low level, X = irrelevant

absolute maximum ratings

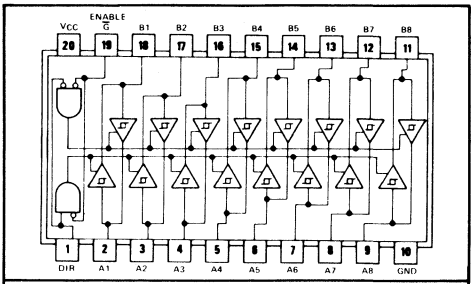
Same as SN54LS245 and SN74LS245 maximum ratings on page 7-359.

SN54LS640, SN54LS642 . . . J PACKAGE
SN74LS640, SN74LS642 . . . J OR N PACKAGE
(TOP VIEW)



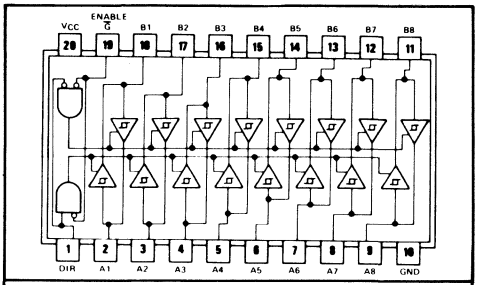
positive logic: see function table

SN54LS641, SN54LS645 . . . J PACKAGE
SN74LS641, SN74LS645 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

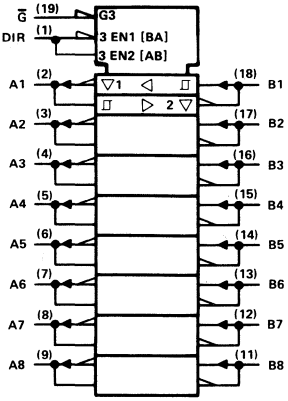
SN54LS643, SN54LS644 . . . J PACKAGE
SN74LS643, SN74LS644 . . . J OR N PACKAGE
(TOP VIEW)



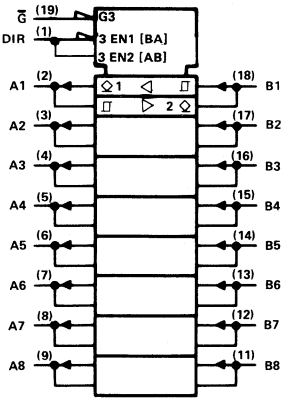
positive logic: see functional table

logic symbols

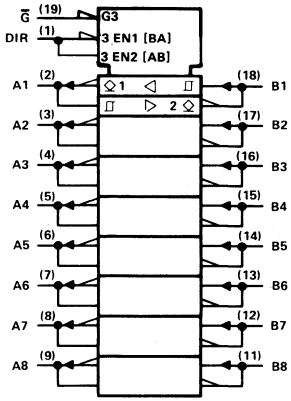
'LS640



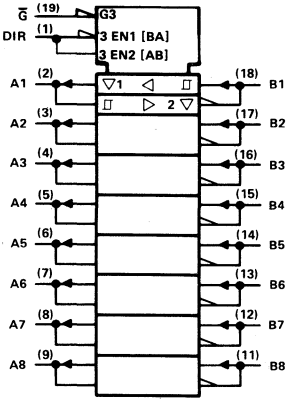
'LS641



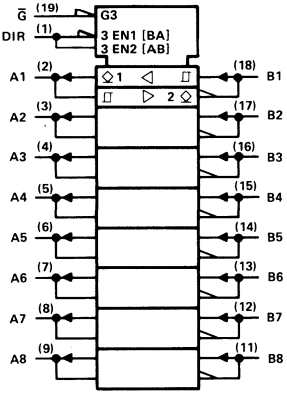
'LS642



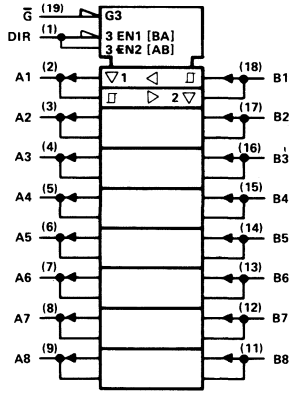
'LS643



'LS644



'LS645



7

recommended operating conditions

PARAMETER	SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15			−15	mA
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1: Voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS640 SN54LS643 SN54LS645			SN74LS640 SN74LS643 SN74LS645			SN74LS640–1 SN74LS643–1 SN74LS645–1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.5			0.6			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V,	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		2.4	3.4		V
			V_{IL} = V_{IL} max	I_{OH} = MAX	2			2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
			V_{IH} = 2 V,	I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
			V_{IL} = V_{IL} max	I_{OL} = 48 mA								0.4	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_O = 2.7 V	$\overline{G}$ at 2 V,			20			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX, V_O = 0.4 V	$\overline{G}$ at 2 V,			−400			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX		−40		−225	−40		−225	−40		−225	mA
I_{CC}	Total supply current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
		Outputs low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

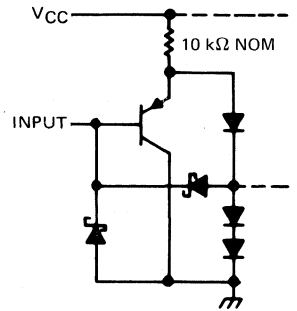
switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS640, 'LS640–1			'LS643, 'LS643–1			'LS645, 'LS645–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		6	10		6	10		8	15	ns
		B	A			6	10		8	15		8	15	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			8	15		9	15		11	15	ns
		B	A			8	15		11	15		11	15	
t_{PZL}	Output enable time to low level	$\overline{G}$, DIR	A			31	40		32	45		31	40	ns
		$\overline{G}$, DIR	B			31	40		32	45		31	40	
t_{PZH}	Output enable time to high level	$\overline{G}$, DIR	A			23	40		27	40		26	40	ns
		$\overline{G}$, DIR	B			23	40		23	40		26	40	
t_{PLZ}	Output disable time from low level	$\overline{G}$, DIR	A	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	
t_{PHZ}	Output disable time from high level	$\overline{G}$, DIR	A			15	25		15	25		15	25	ns
		$\overline{G}$, DIR	B			15	25		15	25		15	25	

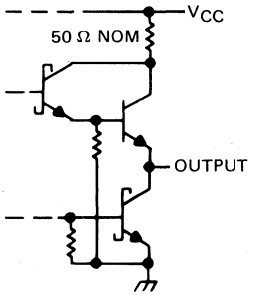
NOTE 2: For load circuits and voltage waveforms, see page 3-11

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS



TYPICAL CHARACTERISTICS

SN54LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

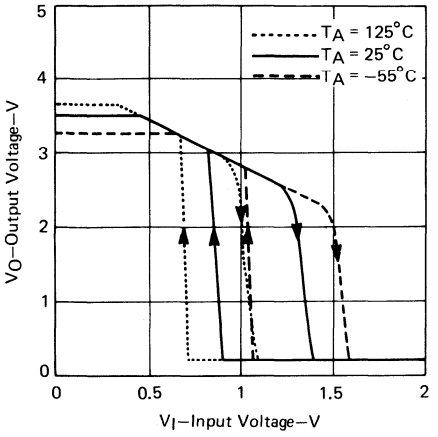


FIGURE 1

SN74LS'
INVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

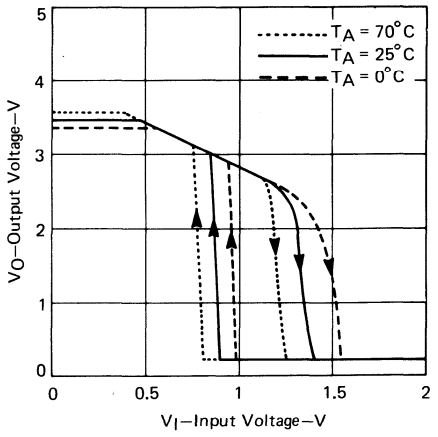


FIGURE 2

SN54LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

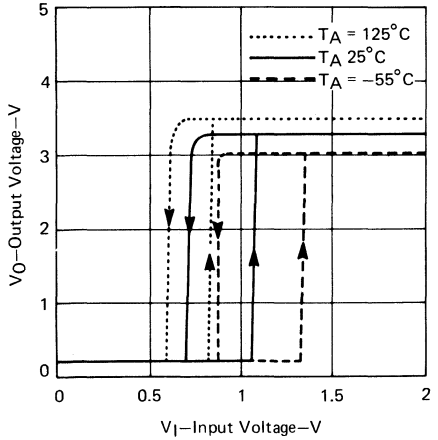


FIGURE 3

SN74LS'
NONINVERTING OUTPUT VOLTAGE
vs
INPUT VOLTAGE

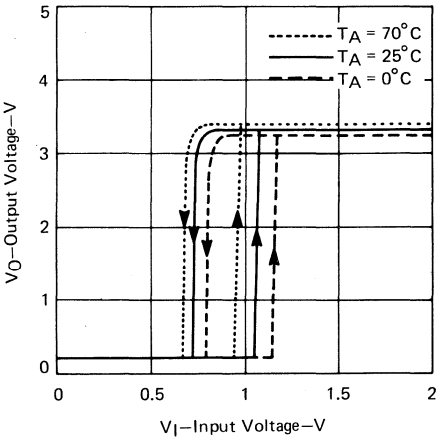


FIGURE 4

recommended operating conditions

PARAMETER	SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5			5.5	V
Low-level output current, I_{OL}			12			24			48	mA
Operating free-air temperature, T_A	−55		125	0		70	0		70	°C

NOTE 1 : Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS641 SN54LS642 SN54LS644			SN74LS641 SN74LS642 SN74LS644			SN74LS641–1 SN74LS642–1 SN74LS644–1			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.5			0.6			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5		0.35	0.5	
				I_{OL} = 48 mA								0.4	0.5	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1			0.1	mA
		DIR or $\overline{G}$		V_I = 7 V			0.1			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4			−0.4	mA
I_{CC}	Total Supply Current	Outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70		48	70	mA
		Outputs low				62	90		62	90		62	90	
		Outputs at Hi-Z				64	95		64	95		64	95	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All Typical values are at V_{CC} = 5 V, T_A = 25°C.

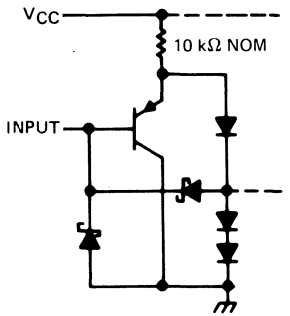
switching characteristics at V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS641, 'LS641–1			'LS642, 'LS642–1			'LS644, 'LS644–1			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	B	C_L = 45 pF, R_L = 667 Ω, See Note 2		17	25		19	25		17	25	ns
		B	A			17	25		19	25		19	25	
t_{PHL}	Propagation delay time, high-to-low-level output	A	B			16	25		14	25		14	25	ns
		B	A			16	25		14	25		16	25	
t_{PLH}	Output disable time from low level	$\overline{G}$, DIR	A			23	40		26	40		26	40	ns
		$\overline{G}$, DIR	B			25	40		28	40		25	40	
t_{PHL}	Output enable time from high level	$\overline{G}$, DIR	A			34	50		43	60		43	60	ns
		$\overline{G}$, DIR	B			37	50		39	60		37	50	

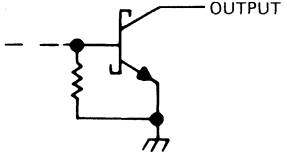
NOTE 2: For load circuits and voltage waveforms, see page 3-11.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF OUTPUTS

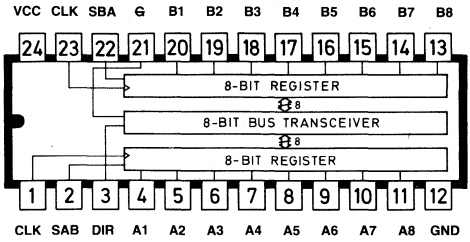


TYPES SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

D2581, JANUARY 1981

- Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs

SN54LS'. . . JT PACKAGE
SN74LS'. . . JT OR NT PACKAGE
(TOP VIEW)



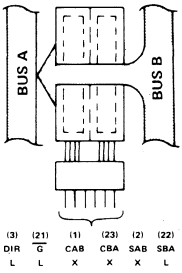
DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

description

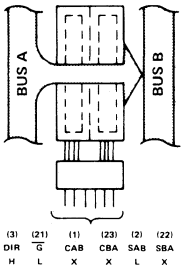
These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Control $\overline{G}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the A or the B register or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled, and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

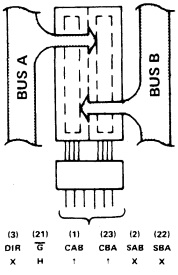
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS646, 'LS647, 'LS648, or 'LS649.



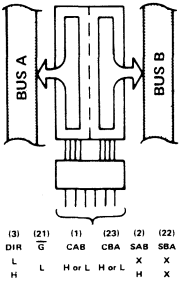
REAL-TIME TRANSFER
BUS B TO BUS A



REAL-TIME TRANSFER
BUS A TO BUS B



STORAGE



TRANSFER
STORED DATA
TO A OR B

FUNCTION TABLE

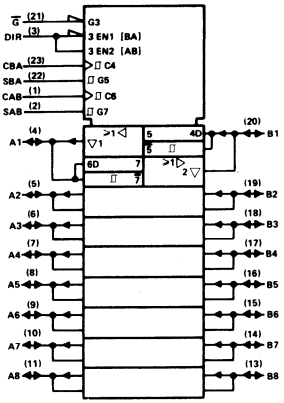
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS646, 'LS647	'LS648, 'LS649
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

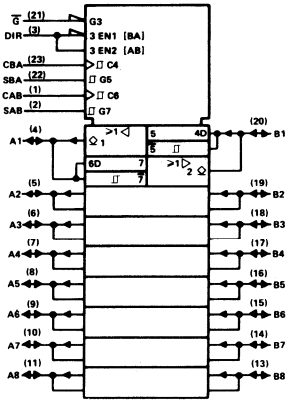
*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

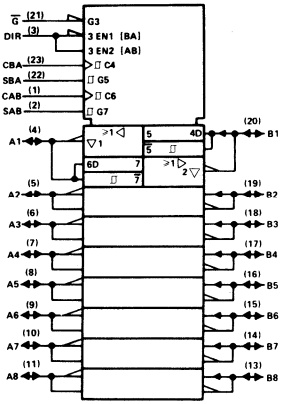
'LS646



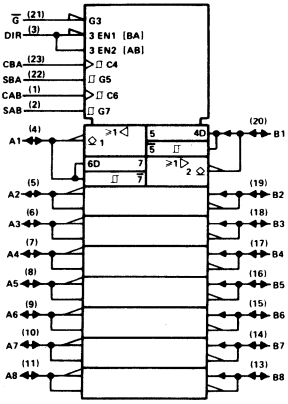
'LS647



'LS648

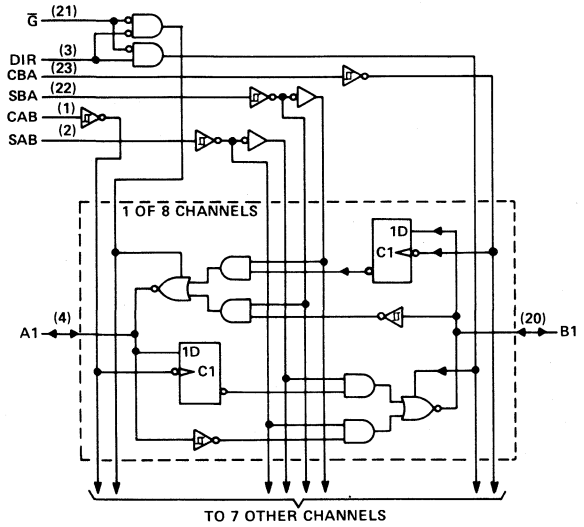


'LS649

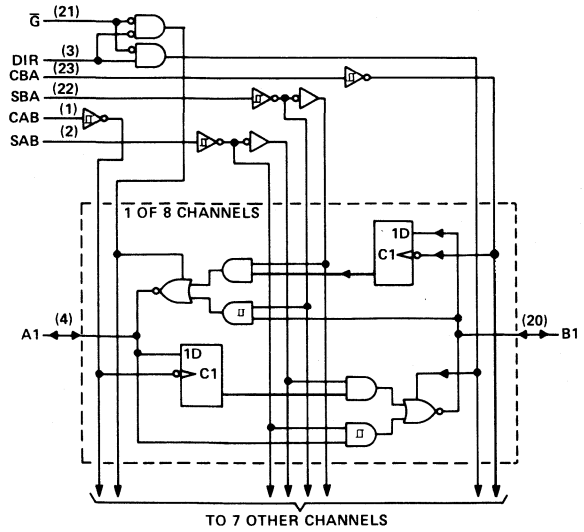


functional block diagram (positive logic)

'LS646, 'LS647

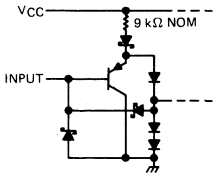


'LS648, 'LS649

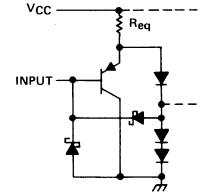


schematics of inputs and outputs

EQUIVALENT OF DIRECTION INPUTS

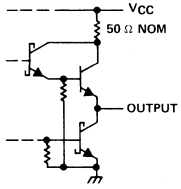


EQUIVALENT OF ALL OTHER INPUTS

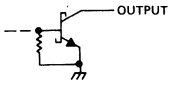


A and B: R_{eq} = 15 kΩ NOM
CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL 'LS646, 'LS648 OUTPUTS



TYPICAL OF ALL 'LS647, 'LS649 OUTPUTS



7

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS646, SN54LS648 . . . . . −55°C to 125°C
SN74LS646, SN74LS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−12			−15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646 SN54LS648			SN74LS646 SN74LS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.5			0.6	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input	V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage: A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
	All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶	V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	V_{CC} = MAX, Outputs open	Outputs high		91	145		91	145	mA
			Outputs low		103	165		103	165	
			Outputs at Hi-Z		103	165		103	165	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646			'LS648			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		15	25		15	25	ns
t_{PHL}					23	35		24	40	ns
t_{PLH}	Bus	Bus			12	18		12	18	ns
t_{PHL}					13	20		15	25	ns
t_{PLH}	Select, with bus input high†	Bus			33	50		37	55	ns
t_{PHL}					14	25		24	40	ns
t_{PLH}	Select, with bus input low†				26	40		26	40	ns
t_{PHL}					21	35		23	40	ns
t_{PZH}	Enable	Bus			33	55		30	50	ns
t_{PZL}					42	65		37	55	ns
t_{PZH}	Direction				28	45		23	40	ns
t_{PZL}					39	60		30	45	ns
t_{PHZ}	Enable	Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		23	35		28	45	ns
t_{PLZ}					22	35		22	35	ns
t_{PHZ}	Direction				20	30		24	35	ns
t_{PLZ}					19	30		19	30	ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11

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absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649 . . . . . −55°C to 125°C
SN74LS647, SN74LS649 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.5			0.6	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{t+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
I_{OH}	High-level output current		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.5 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{CC}	Total Supply Current		V_{CC} = MAX, Outputs open	Outputs high		79	130		79	130	mA
				Outputs low		94	150		94	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		22	35		17	30	ns
t_{PHL}					28	45		28	45	ns
t_{PLH}	Bus	Bus			17	26		15	25	ns
t_{PHL}					18	27		20	30	ns
t_{PLH}	Select, with bus input high†	Bus			39	60		37	55	ns
t_{PHL}					19	30		28	45	ns
t_{PLH}	Select, with bus input low†				33	50		30	45	ns
t_{PHL}					29	45		26	40	ns
t_{PLH}	Enable	Bus			25	40		21	40	ns
t_{PHL}					33	50		34	50	ns
t_{PLH}	Direction				23	35		19	30	ns
t_{PHL}					25	40		27	45	ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

†These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown on page 3-11

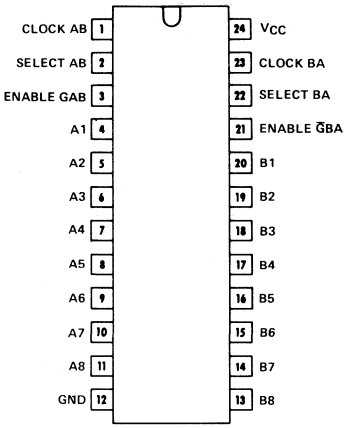
7

TYPES SN54LS651, THRU SN54LS654, SN74LS651, THRU SN74LS654
OCTAL BUS TRANSCEIVERS AND REGISTERS

- **Bidirectional Bus Transceivers/Registers in the New JT and NT 24-pin 300-mil Packages**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs Drive Bus Lines Directly**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
LS651	3-STATE	3-STATE	INVERTING
LS652	3-STATE	3-STATE	TRUE
LS653	OPEN COLLECTOR	3-STATE	INVERTING
LS654	OPEN COLLECTOR	3-STATE	TRUE

SN54LS'...JT PACKAGE
SN74LS'...JT OR NT PACKAGE
(TOP VIEW)



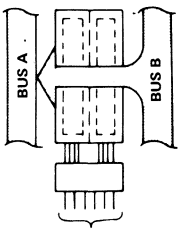
description

These devices consist of bus transceiver circuits with 3-state or open collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or internal storage registers. Enable GAB and $\overline{\text{G}}$BA are provided to control the transceiver functions.

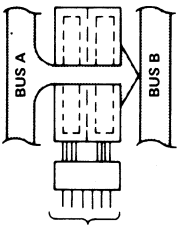
SAB and SBA control pins are provided to select whether real or stored data is transferred. A low selects real data and a high selects stored data.

Data on both the A and B data bus can be stored into the internal D flip-flops by a low to high transition on the appropriate clock pins (CBA and/or CAB) regardless of the select or enable control pins. When SAB and SBA are in the real time transfer mode it is possible to store data without using the internal D flip-flops by simultaneous enabling of GAB and $\overline{\text{G}}$BA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, both set of bus lines will remain at their last states.

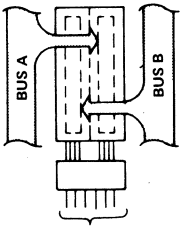
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, 'LS653, or 'LS654.



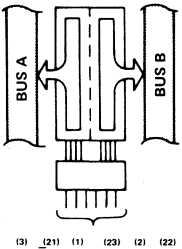
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE



TRANSFER STORED DATA TO A AND/OR B

PRODUCT PREVIEW

This product is under development Texas Instruments reserves the right to discontinue this product without notice.

FUNCTION TABLE

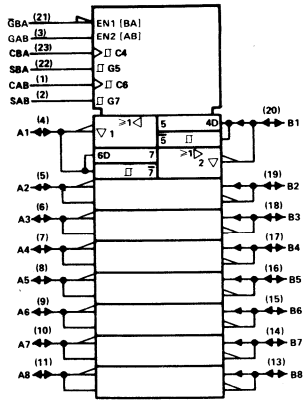
INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651	'LS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and	Stored A Data to B Bus and
								Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus

H = high level L = low level X = irrelevant ↑ = low-to-high-level transition

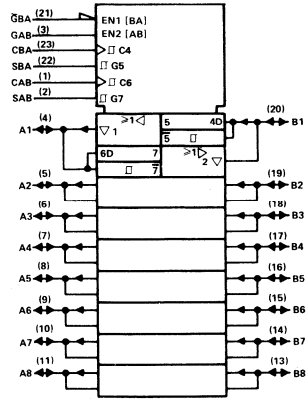
*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols

'LS651/'LS653

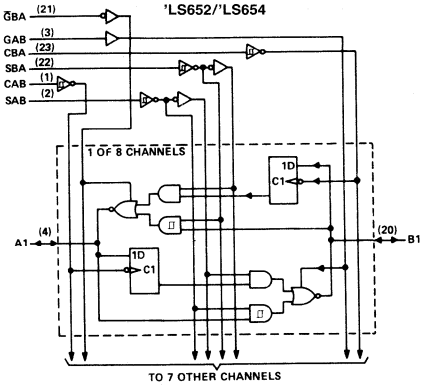


'LS651/'LS653

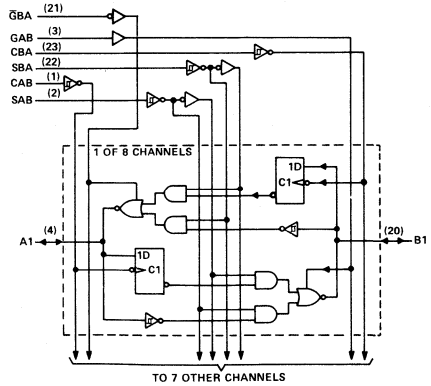


functional block diagram (positive logic)

'LS652/'LS654



'LS652/'LS654



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS651, SN54LS652 . . . . . −55°C to 125°C
SN74LS651, SN74LS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−12			−15	mA
Low-level output current, I_{OL}				12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$), A or B input		V_{CC} = MIN		0.1	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_{CC} = MAX,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current¶		V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS651	V_{CC} = MAX, Outputs open	Outputs high		78			78		mA
				Outputs low		86			86		
				Outputs at Hi-Z		88			88		
		'LS652	V_{CC} = MAX, Outputs open	Outputs high		91			91		
				Outputs low		103			103		
				Outputs at Hi-Z		103			103		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

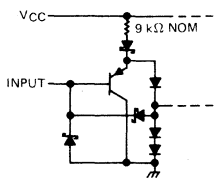
PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651			'LS652			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2		15			15		ns
t_{PHL}					26			23		ns
t_{PLH}	Bus	Bus			15			15		ns
t_{PHL}					23			15		ns
t_{PLH}	Select, with bus input high†	Bus			36			33		ns
t_{PHL}					36			15		ns
t_{PLH}	Select, with bus input low†				27			26		ns
t_{PHL}					27			21		ns
t_{PZH}	Enable $\overline{G}$BA	A Bus			24			28		ns
t_{PZL}					35			39		ns
t_{PZH}	Enable GAB	B Bus			30			33		ns
t_{PZL}					38			42		ns
t_{PHZ}	Enable $\overline{G}$BA	A Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2		23			23		ns
t_{PLZ}					19			19		ns
t_{PHZ}	Enable GAB	B Bus			23			23		ns
t_{PLZ}					22			22		ns

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

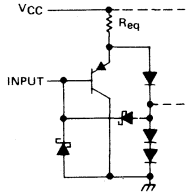
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 2: Load circuits and voltage waveforms are shown on page 3-11

schematics of inputs and outputs

EQUIVALENT OF GAB INPUTS

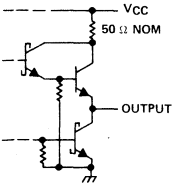


EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} = 15 kΩ NOM
$\overline{G}$BA, CAB and CBA: R_{eq} = 10 kΩ NOM
SAB and SBA: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (control inputs) . . . . . 7 V
Off-state output voltage (A and B ports) . . . . . 5.5 V
Operating free-air temperature: SN54LS653, SN54LS654 . . . . . −55°C to 125°C
SN74LS653, SN74LS654 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS653 SN54LS654			SN74LS653 SN74LS654			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}	A Bus			5.5			5.5	V
High-level output current, I_{OH}	B Bus			−12			−15	mA
Low-level output current, I_{OL}	A or B Bus			12			24	mA
Width of clock pulse, t_w		20			20			ns
Setup time, t_{su}	Bus to clock	20			20			ns
Hold time, t_h	Bus from clock	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 1: All voltage values are with respect to the network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETERS			TEST CONDITIONS†		SN54LS653 SN54LS654			SN74LS653 SN74LS654			UNIT
					MIN	TYP*	MAX	MIN	TYP*	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	A	V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			100			100	μA
V_{OH}	High-level output voltage	B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage	A or B	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	B	V_{CC} = MAX,	V_O = 2.7 V,			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	A or B	V_{CC} = MAX,	V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.4			−0.4	mA
I_{OS}	Output current§	B	V_{CC} = MAX,	V_O = 0	−40		−225	−40		−225	mA
I_{CC}	Total supply current	'LS653	V_{CC} = MAX, Outputs open	Outputs high		78			78		mA
				Outputs low		86			86		
				Outputs at Hi-Z		88			88		
		'LS654	V_{CC} = MAX, Outputs open	Outputs high		91			91		
				Outputs low		103			103		
				Outputs at Hi-Z		103			103		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
* All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS653			'LS654			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Clock	A Bus	R_L = 667 Ω, C_L = 45 pF, See Note 2							ns
t_{PHL}										
t_{PLH}		B Bus								ns
t_{PHL}										
t_{PLH}	A Bus	B Bus								ns
t_{PHL}										
t_{PLH}	B Bus	A Bus								ns
t_{PHL}										
t_{PLH}	Select, with bus input high†	A Bus								ns
t_{PHL}										
t_{PLH}	Select, with bus input low†									ns
t_{PHL}										
t_{PLH}	Select, with bus input high†	B Bus								ns
t_{PHL}										
t_{PLH}	Select, with bus input low†									ns
t_{PHL}										
t_{PLH}	Enable $\overline{G}$BA	A Bus								ns
t_{PHL}										
t_{PZH}	Enable GAB	B Bus	R_L = 667 Ω, C_L = 5 pF, See Note 2							ns
t_{PZL}										
t_{PHZ}										ns
t_{PLZ}										

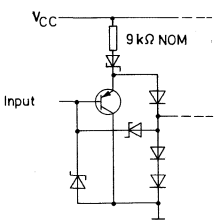
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

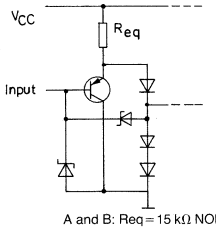
NOTE 2: Load circuits and voltage waveforms are shown on page 3-11.

schematics of inputs and outputs

EQUIVALENT OF GAS INPUTS

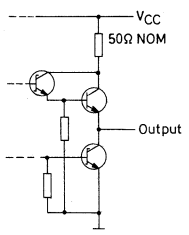


EQUIVALENT OF ALL OTHER INPUTS

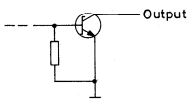


A and B: Req = 15 kΩ NOM
$\overline{G}$BA, CAB and CBA: Req = 10 kΩ NOM
SAB and SBA: Req = 6 kΩ NOM

TYPICAL OF ALL B OUTPUTS



TYPICAL OF ALL A OUTPUTS



TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

D2351, APRIL 1977 – REVISED JANUARY 1981

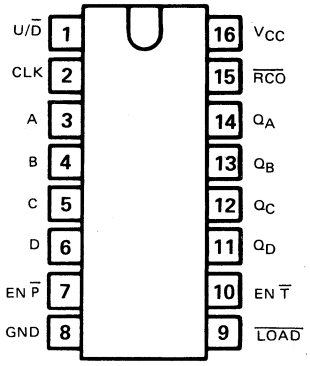
'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	35 MHz	35 MHz	100 mW

SERIES SN54LS' . . . J OR W PACKAGE
SERIES SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

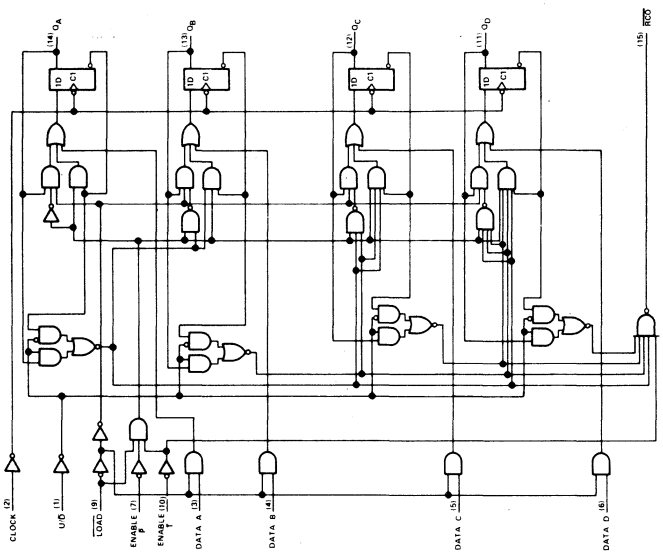
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

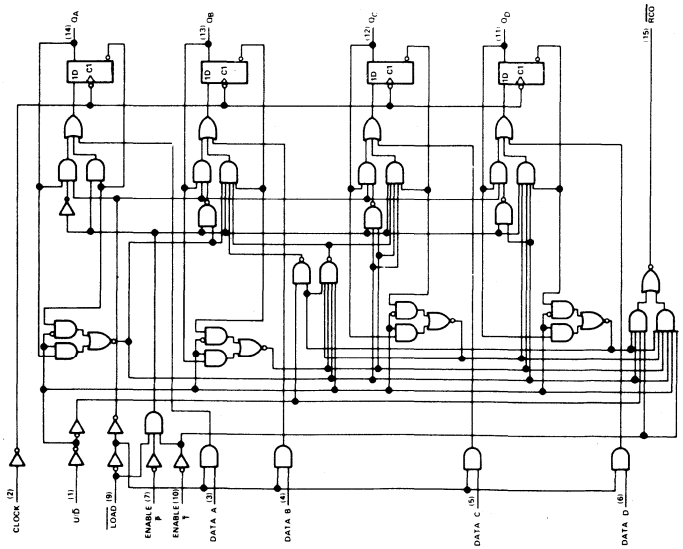
The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.

functional block diagrams

SN54LS669, SN74LS669, BINARY COUNTERS

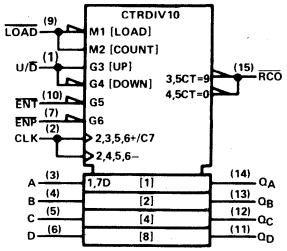


SN54LS668, SN74LS668, DECADE COUNTERS



'LS668 DECADE COUNTERS

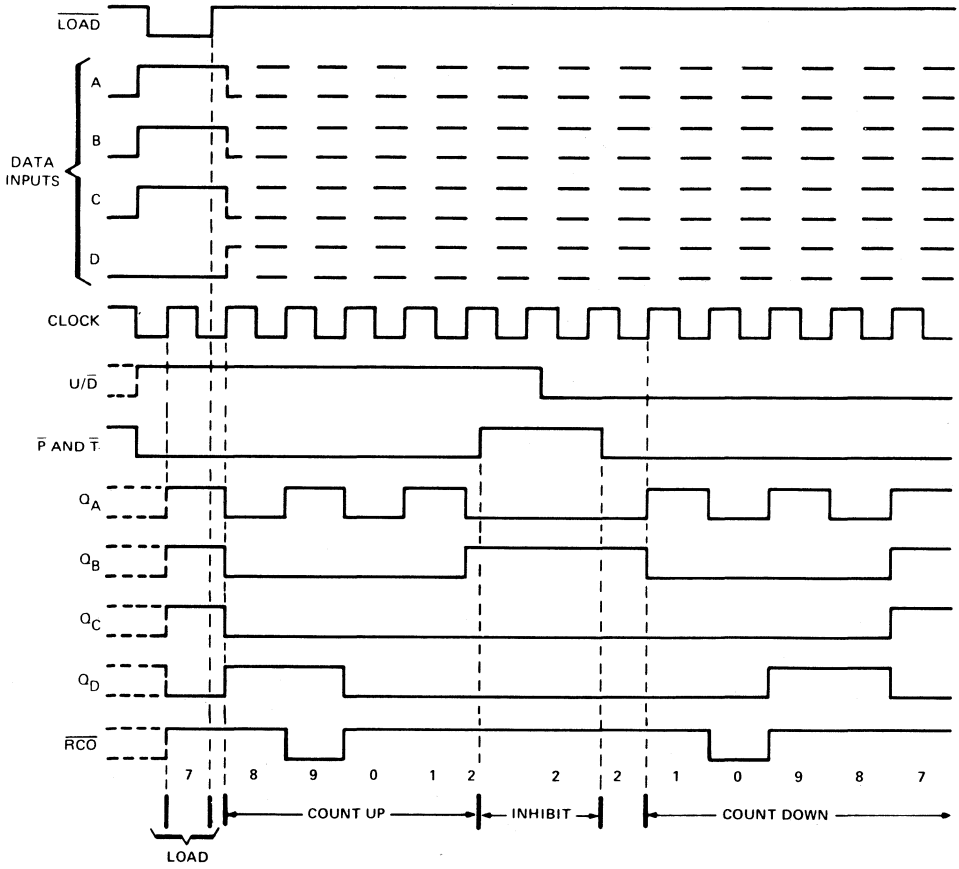
logic symbol



typical load, count, and inhibit sequences

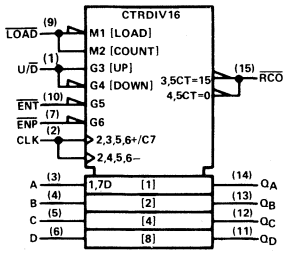
Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



'LS669 BINARY COUNTERS

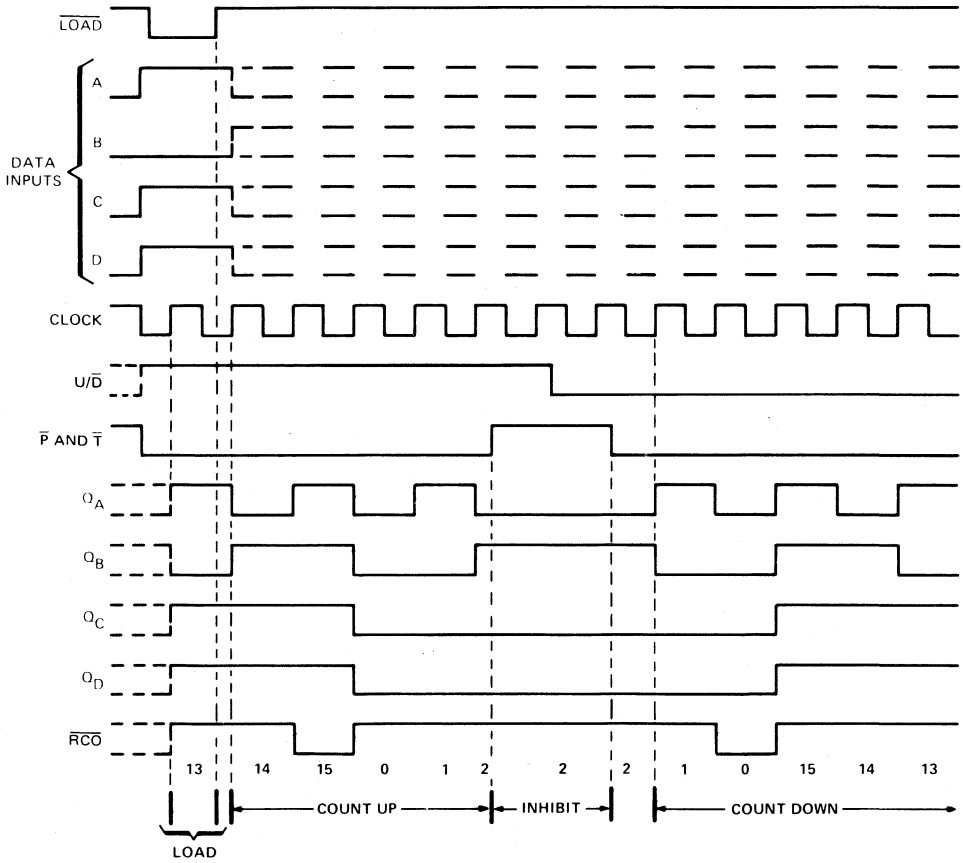
logic symbol



typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



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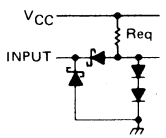
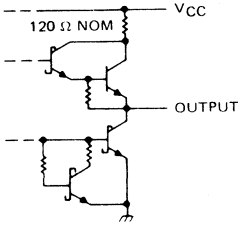
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Load: R_{eq} = 10 kΩ NOM
Data: R_{eq} = 25 kΩ NOM
Clock, Enable $\overline{P}$, $\overline{T}$, U/$\overline{D}$: R_{eq} = 20 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS668, SN54LS669 . . . . . −55°C to 125°C
SN74LS668, SN74LS669 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low) (see Figure 1)		20			20			ns
Setup time, t_{su} (see Figure 1)	Data inputs A, B, C, D	20			20			ns
	Enable $\overline{P}$ or $\overline{T}$	35			35			
	$\overline{LOAD}$	25			25			
	U/$\overline{D}$	30			30			
Hold time at any input with respect to clock, t_h (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Clock, $\overline{T}$					0.1			0.1	
		$\overline{LOAD}$					0.2			0.2	
I_{IH}	High-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Clock, $\overline{T}$					20			20	
		$\overline{LOAD}$					40			40	
I_{IL}	Low-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Clock, $\overline{T}$					−0.4			−0.4	
		$\overline{LOAD}$					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		20	34		20	34	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured after applying a momentary 4.5 V, then ground, to the clock input with all other inputs grounded and the outputs open.

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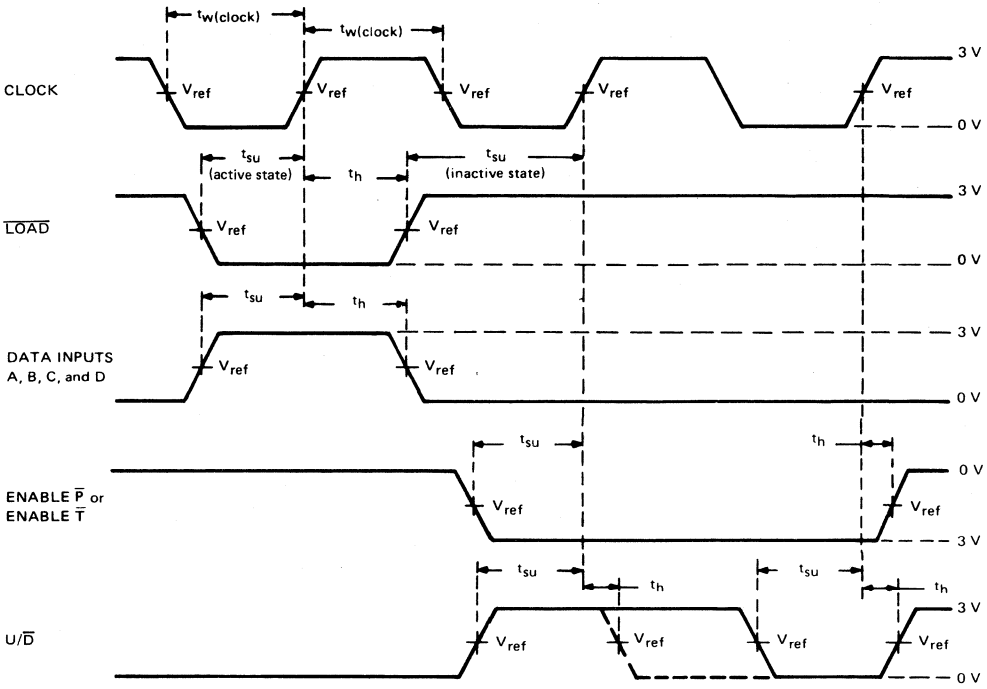
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 2 and 3	25	32		MHz
t_{PLH}	Clock	$\overline{RCO}$			26	40	ns
t_{PHL}					40	60	
t_{PLH}	Clock	Any Q			18	27	ns
t_{PHL}					18	27	
t_{PLH}	Enable $\overline{T}$	$\overline{RCO}$			11	17	ns
t_{PHL}					29	45	
t_{PLH}◇	U/$\overline{D}$	$\overline{RCO}$			22	35	ns
t_{PHL}◇					26	40	

¶ f_{max} = Maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.
◇ Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668 or 15 for 'LS669), the ripple carry output will be out of phase.

PARAMETER MEASUREMENT INFORMATION

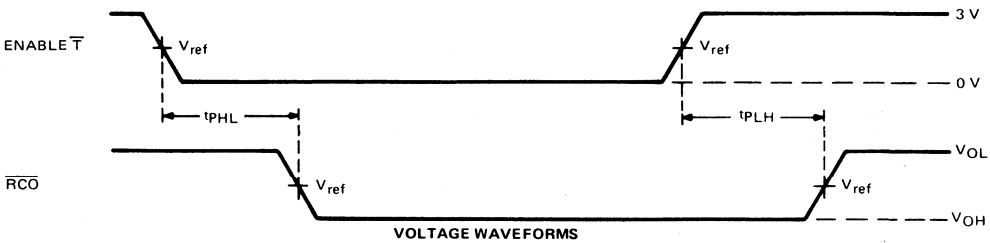


VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

B. $V_{ref} = 1.3$ V.

FIGURE 1–PULSE WIDTHS, SETUP TIMES, HOLD TIMES



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

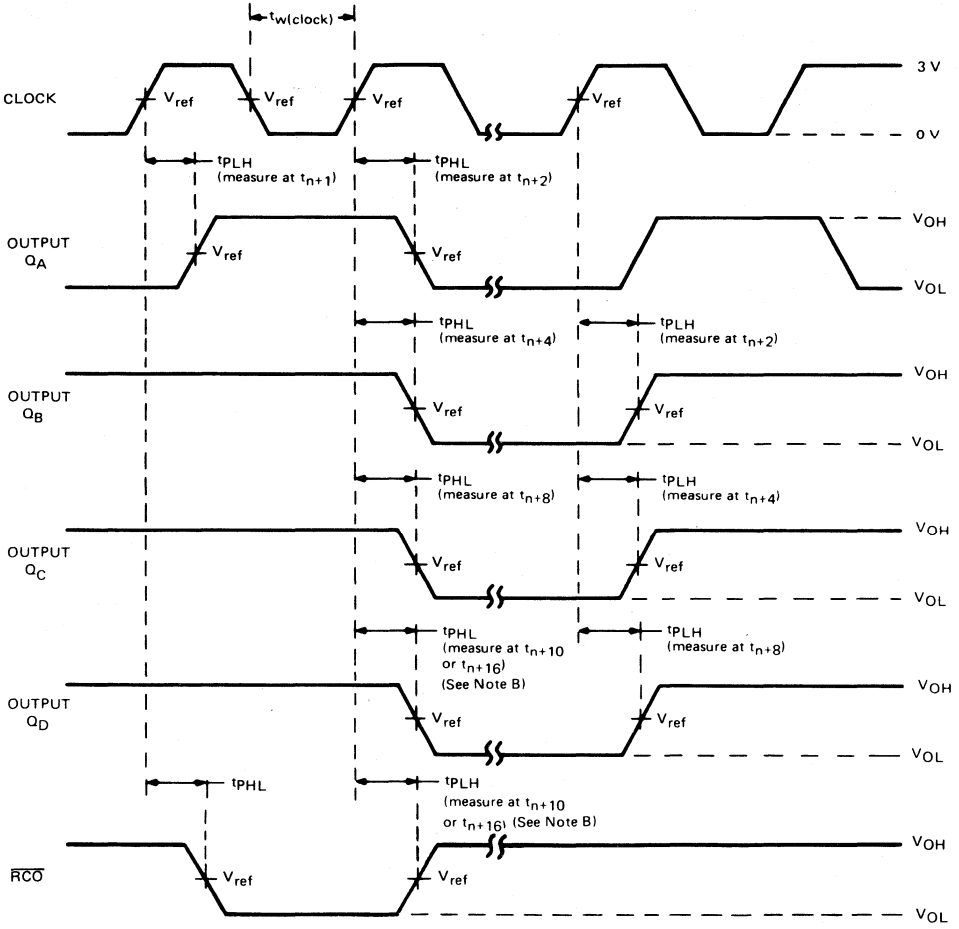
B. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A and Q_D high for 'LS668, all Q outputs high for 'LS669).

C. $V_{ref} = 1.3$ V.

D. Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0) the ripple carry output transition will be in phase. If the count is maximum (9 for 'LS668, or 15 for 'LS669) the ripple carry output will be out of phase.

FIGURE 2–PROPAGATION DELAY TIMES TO CARRY OUTPUT

PARAMETER MEASUREMENT INFORMATION



UP-COUNT VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the 'LS668, and at t_{n+16} for the 'LS669, where t_n is the bit-time when all outputs are low.

C. $V_{ref} = 1.3$ V.

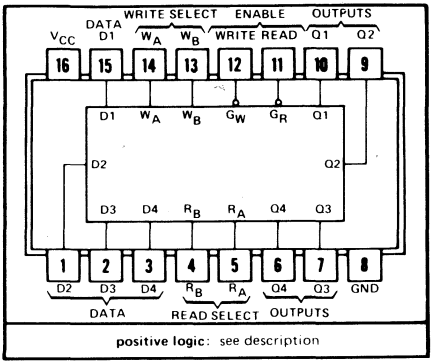
FIGURE 3–PROPAGATION DELAY TIMES FROM CLOCK

TYPES SN54LS670, SN74LS670
4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7612122, MARCH 1974—REVISED OCTOBER 1976

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
  - Scratch-Pad Memory
  - Buffer Storage between Processors
  - Bit Storage in Fast Multiplication Designs
- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs

SN54LS670 . . . J OR W PACKAGE
SN74LS670 . . . J OR N PACKAGE
(TOP VIEW)



description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS670 is characterized for operation from 0°C to 70°C.

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

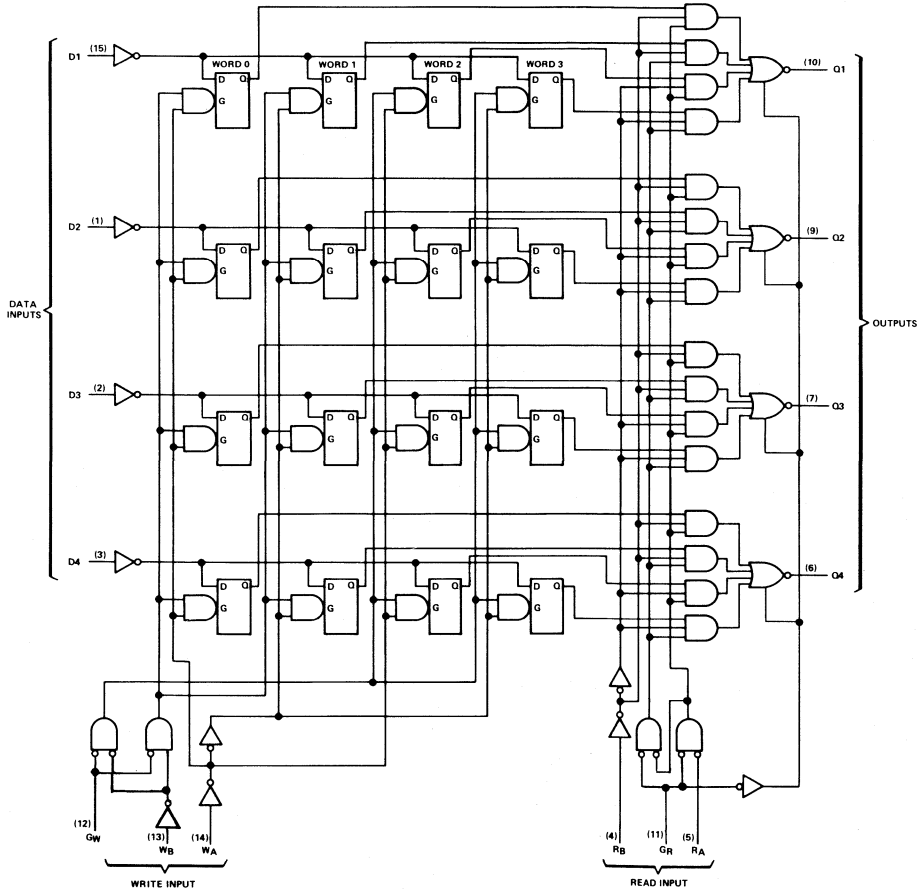
WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

functional block diagram



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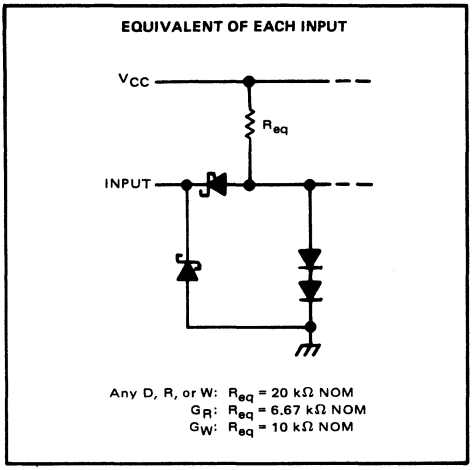
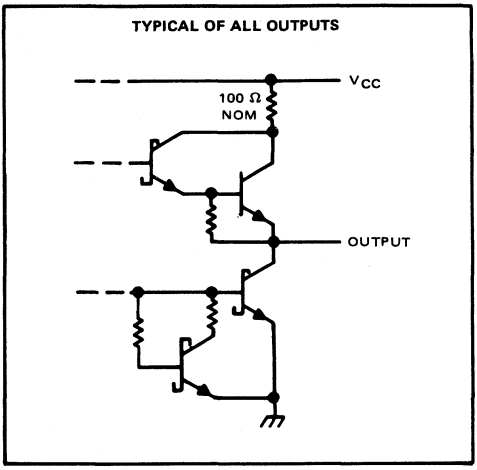
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS670 . . . . . −55°C to 125°C
SN74LS670 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54LS670			SN74LS670			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{su(D)}$	10			10			ns
	Write select with respect to write enable, $t_{h(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_{h(D)}$	15			15			ns
	Write select with respect to write enable, $t_{h(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{su(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{h(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS670			SN74LS670			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.7 V			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.4 V			−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V	Any D, R, or W				0.1			0.1	mA
			G_W				0.2			0.2	
			G_R				0.3			0.3	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	Any D, R, or W				20			20	μA
			G_W				40			40	
			G_R				60			60	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Any D, R, or W				−0.4			−0.4	mA
			G_W				−0.8			−0.8	
			G_R				−1.2			−1.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 4			30	50		30	50	mA

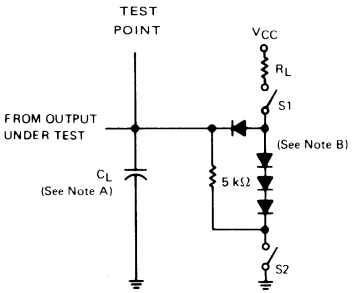
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read select	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2		23	40	ns
t_{PHL}					25	45	
t_{PLH}	Write enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 3		26	45	ns
t_{PHL}					28	50	
t_{PLH}	Data	Any Q			25	45	ns
t_{PHL}					23	40	
t_{PZH}	Read enable	Any Q	C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 4		15	35	ns
t_{PZL}					22	40	
t_{PHZ}			C_L = 5 pF, R_L = 2 kΩ, See Figures 1 and 4		30	50	ns
t_{PLZ}					16	35	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

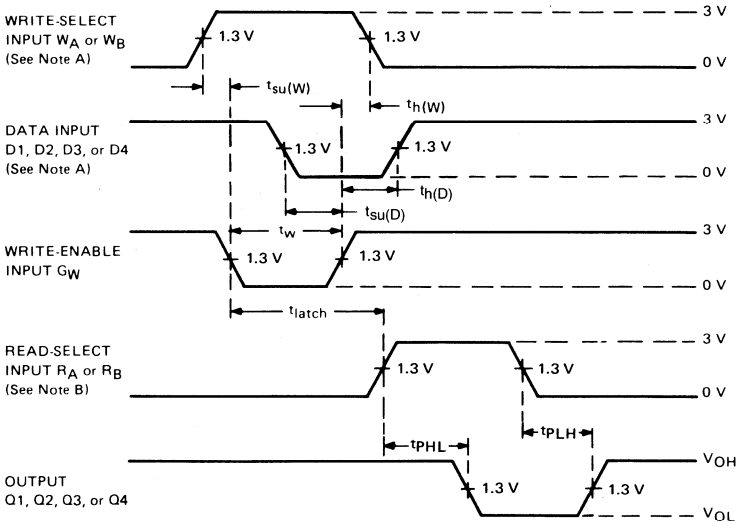
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.

LOAD CIRCUIT

FIGURE 1

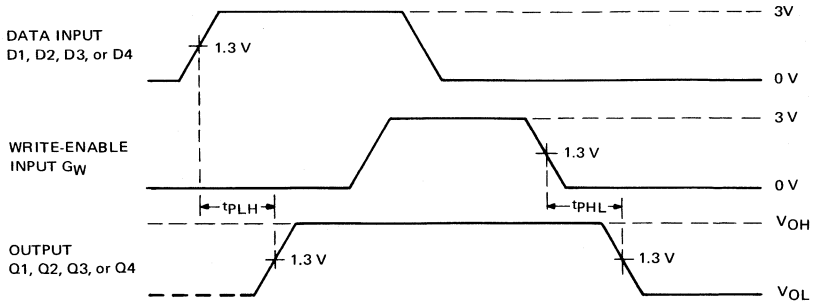


VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

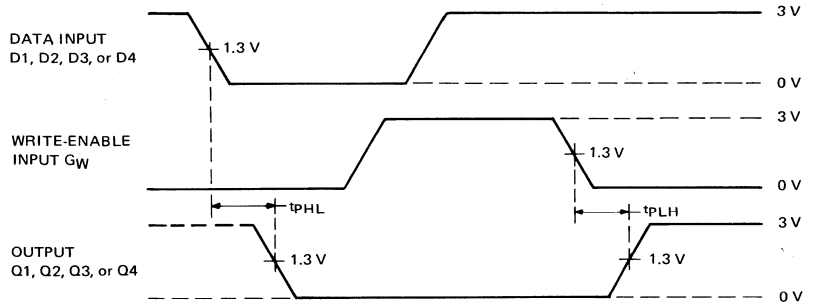
NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: PRR ⩽ 2 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ⩽ 50%, $t_r \leqslant 15$ ns, $t_f \leqslant 6$ ns.

FIGURE 2

PARAMETER MEASUREMENT INFORMATION



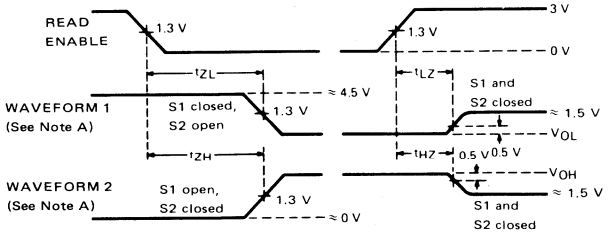
VOLTAGE WAVEFORM 1 (S1 AND S2 ARE CLOSED)



VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
B. Input waveforms are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ⩽ 50%, $t_r \leqslant 15$ ns, $t_r \leqslant 6$ ns.

FIGURE 3



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
C. Input waveforms are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle ⩽ 50%, $t_r \leqslant 15$ ns, $t_r \leqslant 6$ ns.

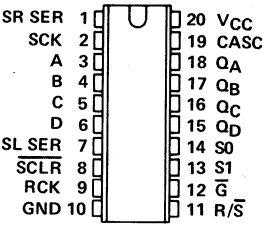
FIGURE 4

TYPES SN54LS671, SN54LS672, SN74LS671, SN74LS672
4-BIT UNIVERSAL SHIFT REGISTERS/REGISTERS WITH 3-STATE OUPUTS

D2638, JANUARY 1981

- 4-Bit Universal Shift Registers/Registers
- Multiplexed Outputs for Shift Register or Stored Data
- Choice of Direct SR Clear ('LS671) or Synchronous SR Clear ('LS672)
- 3-State Outputs Drive Bus Lines Directly
- Expandable to Any Word Length

SN54LS671, SN54LS672 . . J PACKAGE
SN74LS671, SN74LS672 . . J OR N PACKAGE



description

The 'LS671 and 'LS672 each contain a 4-bit universal shift register (similar to the 'LS194A) and a 4-bit storage register (similar to the 'LS175) multiplexed to a 3-state output stage (similar to the 'LS258). The user has the option of selecting the shift or storage register via the register/shift select input R/$\overline{S}$. The 'LS671 has a direct-overriding shift register clear while the 'LS672 features a synchronous shift register clear. The shift register has four distinct modes of operation, namely:

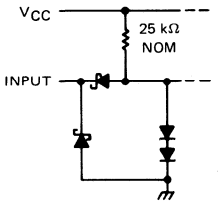
Inhibit clock (do nothing)
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Parallel (broadside) load

A cascade output for the shift register is provided so that full shift register functionality is provided even while the outputs are in the high-impedance mode. The cascade output presents Q_A data in the shift-left mode, Q_D data in the shift-right mode.

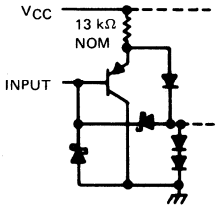
Both the shift register clock and the latch clock are triggered on the positive transition. The output control ($\overline{G}$) activates Q_A thru Q_D when low, it places Q_A thru Q_D into the high-impedance state when high.

schematics of inputs and outputs

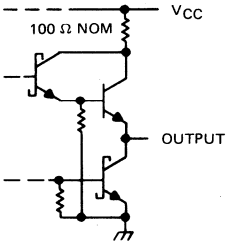
EQUIVALENT OF A THRU D, SL SER, AND SR SER INPUTS



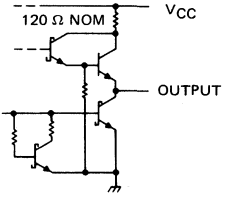
EQUIVALENT OF ALL OTHER INPUTS



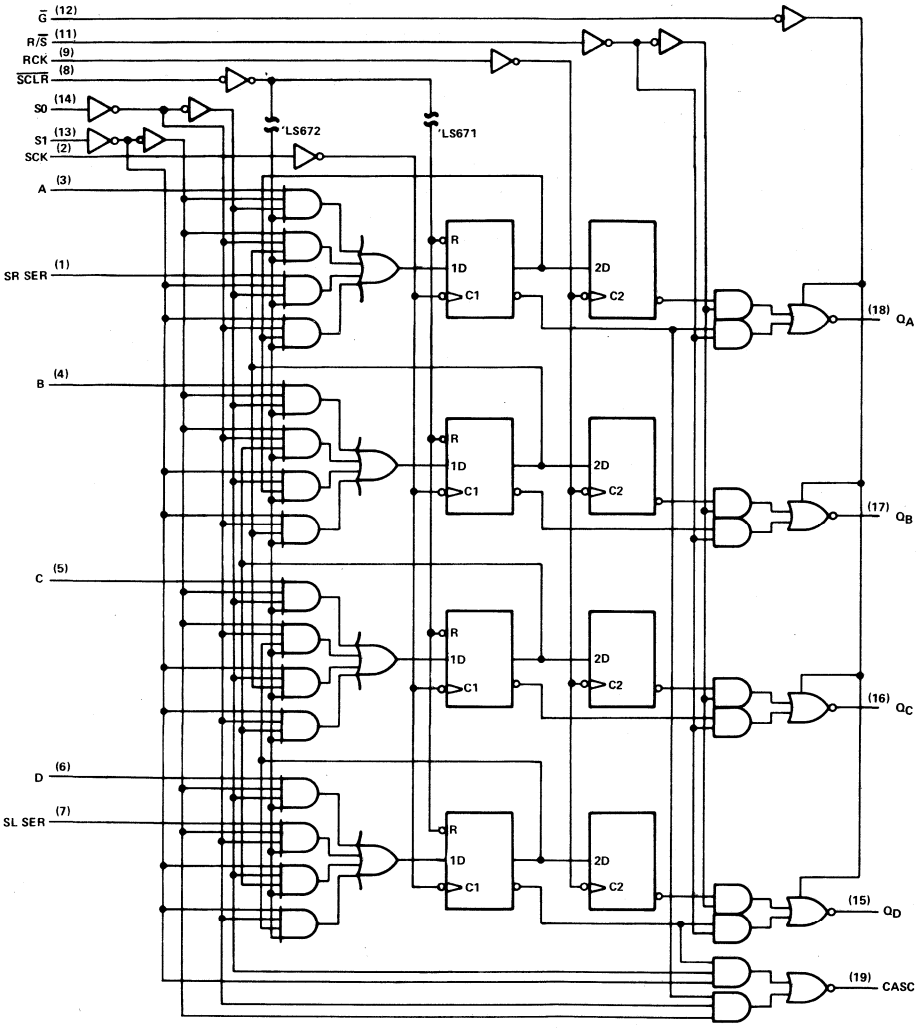
TYPICAL OF Q_A THRU Q_D OUTPUTS



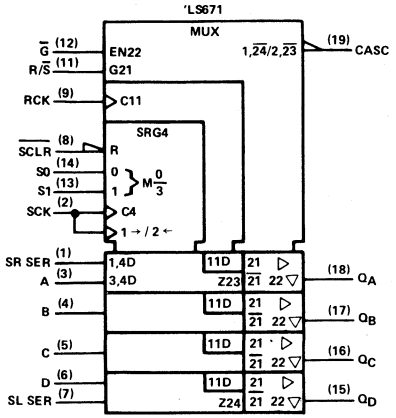
TYPICAL OF CASCADE OUTPUT

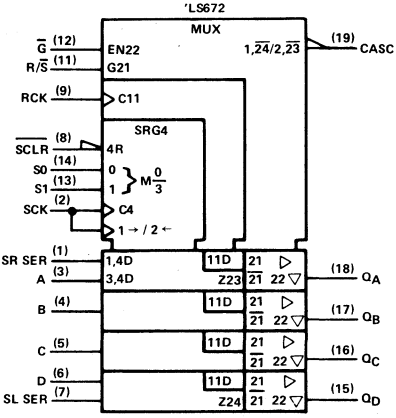


functional block diagram (positive logic)



logic symbols





FUNCTION TABLE

$\overline{G}$	R/$\overline{S}$	$\overline{SCLR}$	SR MODE S1	SR MODE S0	SCK '671	SCK '672	SERIAL INPUTS SL	SERIAL INPUTS SR	PARALLEL INPUTS A	B	C	D	PARALLEL OUTPUTS Q_A	Q_B	Q_C	Q_D	CASC*
L	L	L	X	X	X	↑	X	X	X	X	X	X	L	L	L	L	(*)
L	L	H	X	X	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	(*)
L	L	H	L	L	X	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	H
L	L	H	L	H	↑	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	L	H	↑	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
L	L	H	H	L	↑	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H	Q_{Bn}
L	L	H	H	L	↑	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L	Q_{Bn}
L	L	H	H	H	↑	↑	X	X	a	b	c	d	a	b	c	d	H
H	X	X	L	H	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Cn}
H	X	X	H	L	↑	↑	X	X	X	X	X	X	Z	Z	Z	Z	Q_{Bn}
L	H	X	X	X	X	X	X	X	X	X	X	X	Internal register contents				(*)

When the output control $\overline{G}$ is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the shift register and the output at CASC are not affected.

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock
Z = high-impedance state
*The cascade output displays the D bit of the shift register in mode 1 (S1, S0 = L, H), the A bit in mode 2 (S1, S0 = HL), and is inactive (H) in modes 0 and 3 (S1, S0 = LL and HH).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS671, SN54LS672 . . . . . −55°C to 125°C
SN74LS671, SN74LS672 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Cascade out			−0.4			−0.4	mA
	Q_A, Q_B, Q_C, Q_D			−1			−2.6	
Low-level output current, I_{OL}	Cascade out			4			8	mA
	Q_A, Q_B, Q_C, Q_D			12			24	
Width of SCK, RCK, or $\overline{SCLR}$ ('LS671 only) input pulse, t_w		30			30			ns
Setup time, t_{su}	S0 or S1 to SCK ↑	45			45			ns
	$\overline{SCLR}$ ↓ ('LS672 only) to SCK ↑	45			45			
	A, B, C, D to SCK ↑	30			30			
	SCK ↑ to RCK ↑	30			30			
	SER to SCK ↑	35			35			
Hold time, t_h	Any input from RCK ↑ or SCK ↑	0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	$Q_A - Q_D$	V_{CC} = MIN,	I_{OH} = −1 mA	2.4	3.1					V
		$Q_A - Q_D$	V_{IH} = 2 V,	I_{OH} = −2.6 mA				2.4	3.1		
		CASC	V_{IL} = V_{IL} max	I_{OH} = −400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	$Q_A - Q_D$	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		$Q_A - Q_D$		I_{OL} = 24 mA					0.35	0.5	
		CASC		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
		CASC		I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.7 V, V_{IL} = V_{IL} max			20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	$Q_A - Q_D$	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 0.4 V, V_{IL} = V_{IL} max			−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	A, B, C, D	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	$Q_A - Q_D$	V_{CC} = MAX,	V_O = 0 V	−30		−130	−30		−130	mA
		CASC			−20		−100	−20		−100	
I_{CC}	Supply current	All outputs low	V_{CC} = MAX,	See Note 2		35	70		35	70	mA
		All outputs high	All outputs	See Note 3		30	65		30	65	
		Q_A thru Q_D, at Hi-Z	open	See Note 4		37	70		37	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CCL} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SCK and RCK while S0 is at 4.5 V and all other inputs are grounded.

3. I_{CCH} is tested after two 4.5-V to 0-V to 4.5-V pulses have been applied to SCK and RCK while all other inputs are at 4.5 V.

4. I_{CCZ} is tested after two 0-V to 4.5-V to 0-V pulses have been applied to SCK and RCK while S0 and $\overline{G}$ are at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS671			'LS672			UNIT
			MODE	LOAD	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SCK ↑	CASCADE	SHIFT LEFT OR RIGHT	R_L = 2 kΩ, C_L = 15 pF		31	45		31	45	ns
t_{PHL}						14	25		14	25	
t_{PLH}	S0, S1					11	20		12	20	ns
t_{PHL}						11	20		12	20	
t_{PHL}	SCK ↑		SR CLEAR						19	30	ns
t_{PHL}	$\overline{SCLR}$ ↓					19	30				ns
t_{PLH}	SCK ↑	$Q_A - Q_D$	SHIFT LEFT OR RIGHT	R_L = 667 Ω, C_L = 45 pF		10	20		10	20	ns
t_{PHL}						16	25		16	25	
t_{PLH}			SR LOAD			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PHL}			SR CLEAR						17	30	ns
t_{PHL}	$\overline{SCLR}$ ↓					21	30				ns
t_{PLH}	RCK ↑		LATCH			10	20		10	20	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↑		MUX			12	25		13	25	ns
t_{PHL}						15	25		15	25	
t_{PLH}	R/$\overline{S}$ ↓					17	25		17	25	ns
t_{PHL}						16	25		16	25	
t_{PZH}	$\overline{G}$ ↓		3-STATE ENABLE			16	25		16	25	ns
t_{PZL}						19	30		19	30	
t_{PHZ}	$\overline{G}$ ↑		3-STATE DISABLE	R_L = 667 Ω, C_L = 5 pF		16	25		16	25	ns
t_{PLZ}						16	25		16	25	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-11

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

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TYPICAL APPLICATION DATA

The 'LS671 or 'LS672 can easily be expanded utilizing the cascade output and the SL SER and SR SER inputs. A typical expansion is shown below.

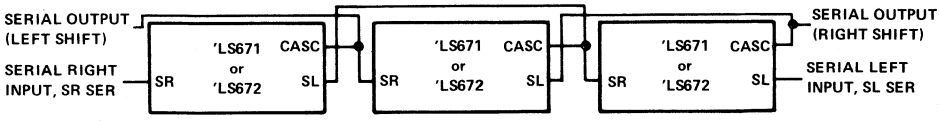


FIGURE 1 – 'LS671, 'LS672 EXPANDED TO 12 BITS, (3 PACKAGES)

Any desired word length may be obtained using the scheme shown. Corresponding control pins of all the packages are tied in common, i.e., all S0 pins are connected together, all S1 pins are connected together, etc.

TYPES SN54LS673, SN54LS674, SN74LS673, SN74LS674
16-BIT SHIFT REGISTERS

D2421, JUNE 1978

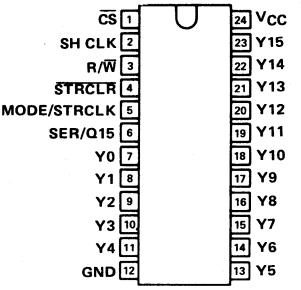
'LS673

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

'LS674

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

SN54LS673 . . . J OR W PACKAGE
SN74LS673 . . . J OR N PACKAGE
(TOP VIEW)



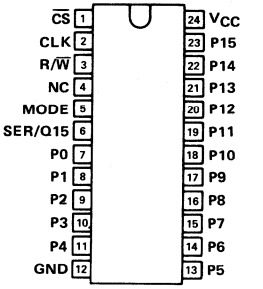
description

SN54LS673, SN74LS673

The 'LS673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (SER/Q15) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-select ($\overline{CS}$) input disables both the shift-register clock and the storage-register clock and places SER/Q15 in the high-impedance state. The store-clear function is not disabled by the chip select.

SN54LS674 . . . J OR W PACKAGE
SN74LS674 . . . J OR N PACKAGE
(TOP VIEW)



NC – No internal connection

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

SN54LS674, SN74LS674

The 'LS674 is a 16-bit parallel-in, serial-out shift register. A three-state input/output (SER/Q15) port provides access for entering serial data or reading the shift-register word in a recirculating loop.

The device has four basic modes of operation:

1) Hold (do nothing)
2) Write (serially via input/output)
3) Read (serially)
4) Load (parallel via data inputs)

Low-to-high-level changes at the chip select input should be made only when the clock input is low to prevent false clocking.

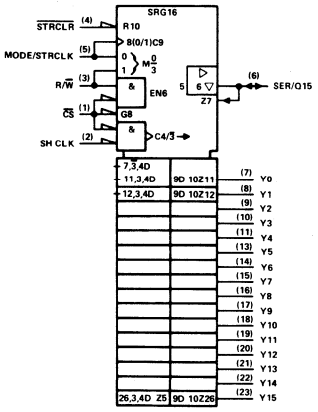
'LS673

FUNCTION TABLE

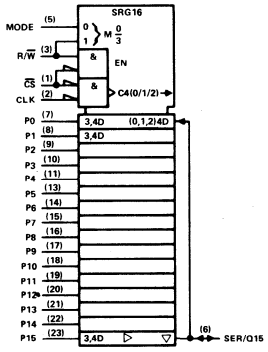
INPUTS					SER/ Q15	SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS	
$\overline{CS}$	R/$\overline{W}$	SH CLK	$\overline{STRCLR}$	MODE/ STRCLK		SHIFT	READ FROM SERIAL OUTPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		NO
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO			NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	H	L	NO	YES		YES	YES	NO
L	H	↓	H	H	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO		NO	NO	YES

logic symbols

'LS673



'LS674



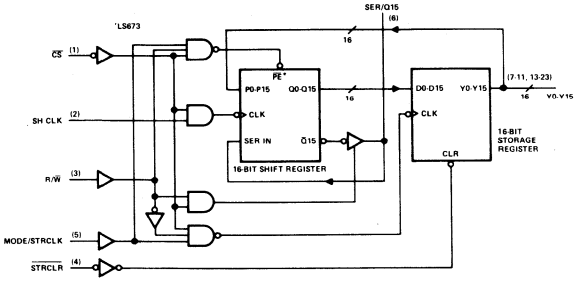
'LS674 FUNCTION TABLE

INPUTS				SER/	OPERATION
$\overline{CS}$	R/$\overline{W}$	MODE	CLK	Q15	
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	Parallel load

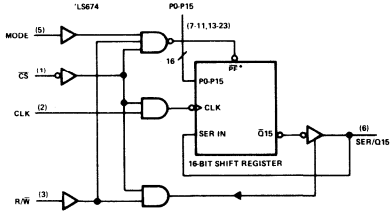
H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
X = irrelevant (any input including transitions)
Z = high impedance, input mode
Q14n = content of 14th bit of the shift register before the most recent ↓ transition of the clock.
Q15 = present content of 15th bit of the shift register
Y15n = content of the 15th bit of the storage register before the most recent ↓ transition of the clock.
P15 = level of input P15

functional block diagrams

SN54LS673, SN74LS673

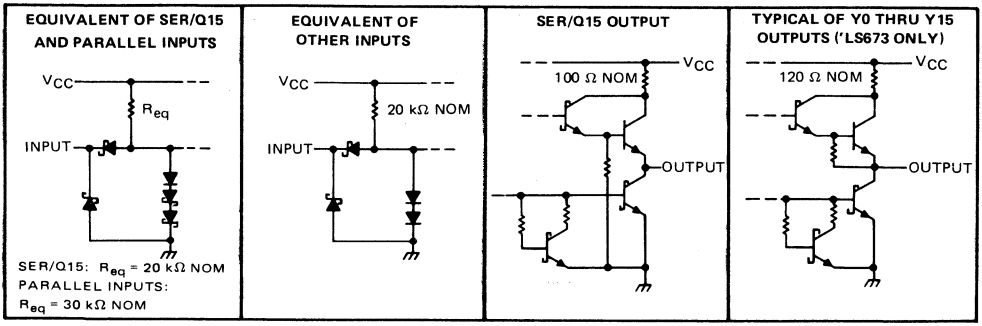


SN54LS674, SN74LS674



*When $\overline{PE}$ is low, data is synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: SER/Q15 . . . . . 5.5 V
All others . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS673, SN54LS674 . . . . . −55°C to 125°C
SN74LS673, SN74LS674 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	SER/Q15			−1			−2.6	mA
	Y0 thru Y15			−0.4			−0.4	
Low-level output current, I_{OL}	SER/Q15			12			24	mA
	Y0 thru Y15			4			8	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		20			20			ns
Width of clear input pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{su}	SER/Q15	20			20			ns
	P0 thru P15	20			20			
	Mode	35			35			
	$\overline{R/W}$, $\overline{CS}$	35			35			
Hold time, t_h	SER/Q15	0			0			ns
	P0 thru P15	0			0			
	Mode	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	SER/Q15	V_{CC} = MIN,	V_{IH} = 2 V,	2.4	3.2		2.4	3.1		V
		Y0 thru Y15¶	V_{IL} = V_{IL}max,	I_{OH} = MAX	2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	SER/Q15	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
		Y0 thru Y15¶		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 2.7 V			40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	SER/Q15	V_{CC} = MAX, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_O = 0.4 V			−400			−400	μA
I_I	Input current at maximum input voltage	SER/Q15	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		Others		V_I = 7 V			0.1			0.1	
I_{IH}	High-level input current	SER/Q15	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
		Others					20			20	
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	SER/Q15	V_{CC} = MAX		−30		−130	−30		−130	mA
		Y0 thru Y15¶			−20		−100	−20		−100	
I_{CC}	Supply current	'LS673	V_{CC} = MAX			50	80		52	80	mA
		'LS674				25	40		25	40	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
¶'LS673 only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 2

PARAMETER	'LS673 FROM	'LS673 TO	'LS674 FROM	'LS674 TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF	20	28		MHz
t_{PHL}	$\overline{STRCLR}$	Y0 thru Y15			R_L = 2 kΩ, C_L = 15 pF		25	40	ns
t_{PLH}	MODE/ STRCLK	Y0 thru Y15					28	45	
t_{PHL}							30	45	
t_{PLH}	SH CLK	SER/Q15	CLK	SER/Q15	R_L = 667 Ω, C_L = 45 pF		21	33	ns
t_{PHL}							26	40	
t_{PZH}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 45 pF		30	45	ns
t_{PZL}							30	45	
t_{PHZ}	$\overline{CS}$, R/$\overline{W}$	SER/Q15	$\overline{CS}$, R/$\overline{W}$	SER/Q15	R_L = 667 Ω, C_L = 5 pF		25	40	ns
t_{PLZ}							25	40	

NOTE 2: For load circuit and voltage waveforms see page 3-11

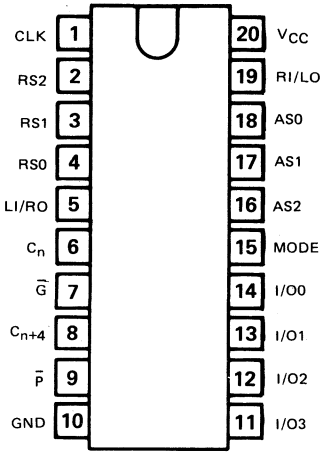
f_{max} ≡ maximum clock frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from low level
t_{PLZ} ≡ Output disable time from high level

TYPES SN54LS681, SN74LS681
4-BIT PARALLEL BINARY ACCUMULATORS

D2422, JANUARY 1981

- Full 4-Bit Binary Accumulator in a Single 20-Pin Package
- Contains Two Synchronous Registers:
  - Word A
  - Word B Shift/Accumulator
- 16 Arithmetic Operations Including B Minus A and A Minus B
- 16 Logic-Mode Operations
- Expandable to Handle N-Bit Words with Full Carry Look-Ahead
- Bus Driving I/O Ports

SN54LS681 . . . J PACKAGE
SN74LS681 . . . J OR N PACKAGE
(TOP VIEW)



description

These low-power Schottky IC's integrate a high-speed arithmetic logic unit (ALU) complete with word A and word B registers on a single chip. The ALU performs 16 arithmetic and 16 logic functions (see Tables 1 and 2). Full carry look-ahead is provided for fast carry of four-bit words. The carry input (C_n) and propagate and generate outputs ($\overline{P}$ and $\overline{G}$) are provided for direct use with SN54S182/SN74S182 carry look-ahead generators for optimum performance with longer words.

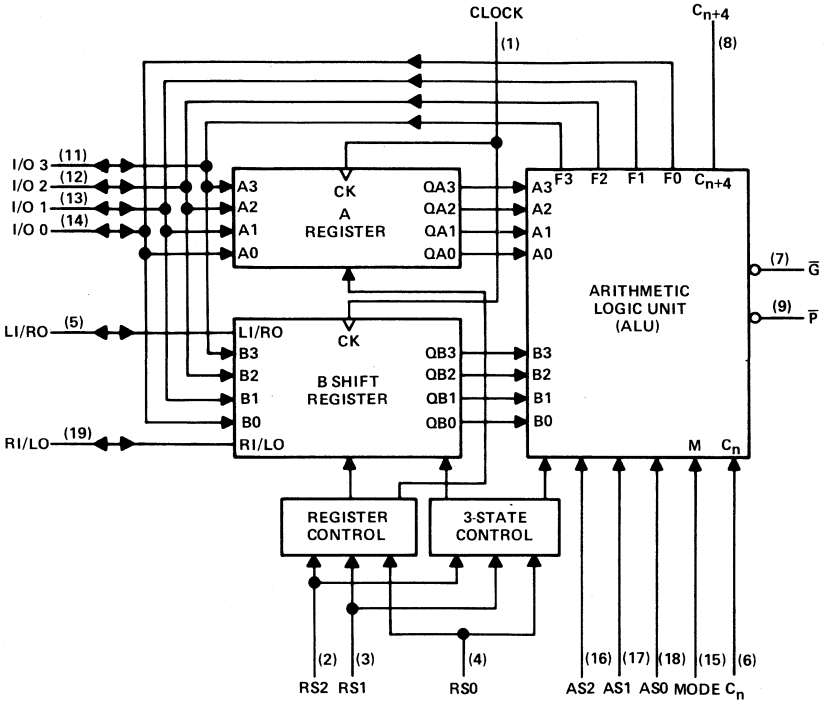
The A and B registers are controlled by three inputs (RS0, RS1, and RS2). These pins define eight distinct register modes (see Table 3). The A register is a simple storage register while the B register is a combination storage/shift/accumulator register. The contents of the A and B registers provide the A and B words for the ALU.

Four I/O ports (I/O 0 thru I/O 3) are provided for parallel loading of word A and/or word B into their respective registers. These same ports also serve as bus driving outputs for the ALU/accumulator results (F_j). Two additional I/O ports (RI/LO and LI/RO) are provided to allow expansion of the accumulator for words greater than four bits in length.

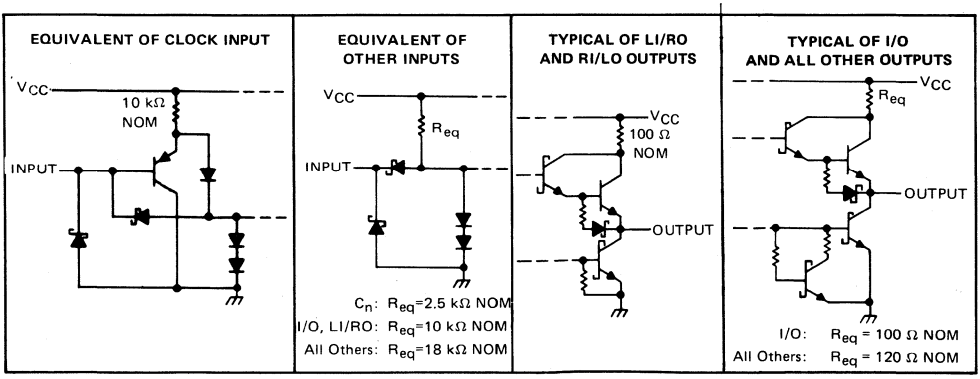
The A or B register can be parallel loaded from the four I/O ports. The B register can also be parallel loaded from the ALU as an accumulator register and in addition, the B register can be serially loaded from either the RI/LO or the LI/RO ports.

The SN54LS681 is characterized for operation over the full military temperature range from −55°C to 125°C. The SN74LS681 is characterized for operation from 0°C to 70°C.

functional block diagram



schematics of inputs and outputs



FUNCTION TABLES

TABLE 1 – ARITHMETIC FUNCTIONS

Mode Control (M) = Low

ALU SELECTION			ACTIVE-HIGH DATA	
AS2	AS1	AS0	C_n = H (with carry)	C_n = L (no carry)
L	L	L	$F_j = L$	$F_j = H$
L	L	H	F = B MINUS A	F = B MINUS A MINUS 1
L	H	L	F = A MINUS B	F = A MINUS B MINUS 1
L	H	H	F = A PLUS B PLUS 1	F = A PLUS B
H	L	L	F = B PLUS 1	$F_j = B_j$
H	L	H	F = $\overline{B}$ PLUS 1	$F_j = \overline{B_j}$
H	H	L	F = A PLUS 1	$F_j = A_j$
H	H	H	F = $\overline{A}$ PLUS 1	$F_j = \overline{A_j}$

TABLE 2 – LOGIC FUNCTIONS

Mode Control (M) = High

ALU SELECTION			ACTIVE-HIGH DATA	
AS2	AS1	AS0	C_n = H (with carry)	C_n = L (no carry)
L	L	L	$F_0 = H, F_1 = F_2 = F_3 = L$	$F_j = L$
L	L	H	$F_j = A_j \oplus B_j$ PLUS 1	$F_j = A_j \oplus B_j$
L	H	L	$F_j = \overline{A_j \oplus B_j}$ PLUS 1	$F_j = \overline{A_j \oplus B_j}$
L	H	H	$F_j = L$	$F_j = H$
H	L	L	$F_j = A_j B_j$ PLUS 1	$F_j = A_j B_j$
H	L	H	$F_j = \overline{A_j + B_j}$ PLUS 1	$F_j = \overline{A_j + B_j}$
H	H	L	$F_j = \overline{A_j B_j}$ PLUS 1	$F_j = \overline{A_j B_j}$
H	H	H	$F_j = A_j + B_j$ PLUS 1	$F_j = A_j + B_j$

TABLE 3 – REGISTER FUNCTIONS

FUNCTION	INPUTS BEFORE L TO H CLOCK TRANSITION									INTERNAL OUTPUTS AFTER L TO H CLOCK TRANSITION												
	REGISTER SELECTION			DATA INPUTS						A REGISTER				B SHIFT REGISTER						ALU			
	RS2	RS1	RS0	LI/RO	I/O 3	I/O 2	I/O 1	I/O 0	RI/LO	QA3	QA2	QA1	QA0	LI/RO	QB3	QB2	QB1	QB0	RI/LO	F3	F2	F1	F0
ACCUM	L	L	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$F3_n$	$F2_n$	$F1_n$	$F0_n$	Z	F3	F2	F1	F0
LOAD B	L	L	H	Z	b3	b2	b1	b0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	b3	b2	b1	b0	Z	Z	Z	Z	Z
LEFT SHIFT LOGICAL	L	H	L	li	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	li	li	$QB3_n$	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
LEFT SHIFT ARITH	L	H	H	li	F3	F2	F1	F0	QB0	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	li	$QB3_n$	li	$QB2_n$	$QB1_n$	$QB1_n$	F3	F2	F1	F0
RIGHT SHIFT LOGICAL	H	L	L	QB3	F3	F2	F1	F0	ri	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB2_n$	$QB2_n$	$QB1_n$	$QB0_n$	ri	ri	F3	F2	F1	F0
RIGHT SHIFT ARITH	H	L	H	QB2	F3	F2	F1	F0	ri	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	$QB1_n$	$QB3_n$	$QB1_n$	$QB0_n$	ri	ri	F3	F2	F1	F0
HOLD	H	H	L	Z	F3	F2	F1	F0	Z	$QA3_0$	$QA2_0$	$QA1_0$	$QA0_0$	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	$F3_0$	$F2_0$	$F1_0$	$F0_0$
LOAD A	H	H	H	Z	a3	a2	a1	a0	Z	a3	a2	a1	a0	Z	$QB3_0$	$QB2_0$	$QB1_0$	$QB0_0$	Z	Z	Z	Z	Z

H = high level (steady state)

L = low level (steady state)

Z = high impedance (output off)

a0 . . . a3, b0 . . . b3 = the level of steady - state condition at I/O 0 thru I/O 3, respectively and intended as A or B input data

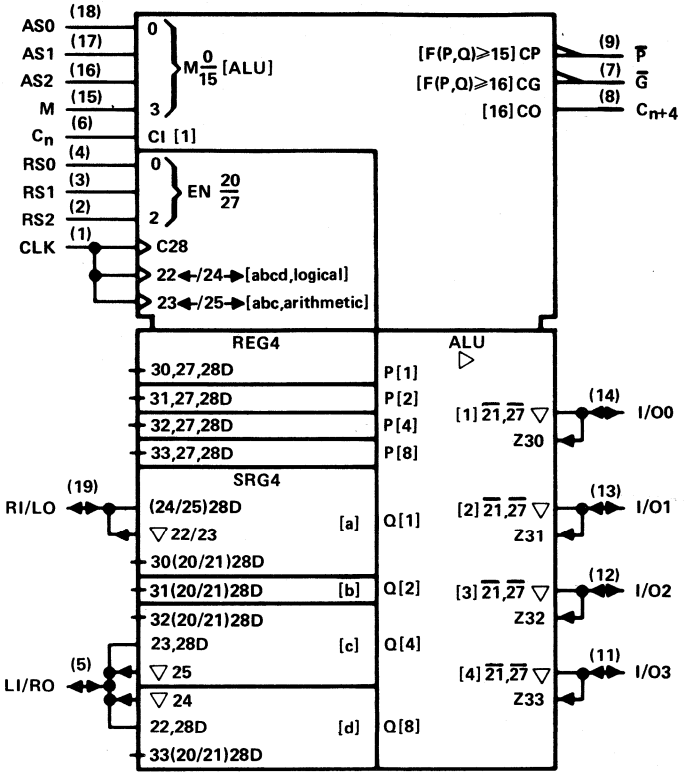
F0 . . . F3 = internal ALU results

$QA0_0 \ldots QB0_0$, $F0_0 \ldots F3_0$ = the level of QA0 thru QB3 and F0 thru F3, respectively, before the indicated steady-state input conditions were established

$QA0_n \ldots QB3_n$ = the level of QA0 thru QB3 before the most recent ↑ transition of the clock

ri, li = the level of steady-state conditions at RI/LO or LI/RO, respectively

logic symbol



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS681 . . . . . −55°C to 125°C
SN74LS681 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS681			SN74LS681			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	LI/RO, I/O, RI/LO			−1			−2.6	mA
	$\overline{P}$, $\overline{G}$, C_{n+4}			−400			−400	μA
Low-level output current, I_{OL}	I/O			12			24	mA
	C_{n+4}, LI/RO, RI/LO			4			8	
	$\overline{P}$			8			8	
	$\overline{G}$			16			16	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Setup time, t_{su}	RS0-RS2 to CLK↑	30			30			ns
	Data I/O to CLK↑	25			25			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS681			SN74LS681			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage	C_n					0.7			0.7	V
		All others					0.7			0.8	
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	All I/O	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max, I_{OH}=MAX		2.4	3.1		2.4	3.2		V
		$\overline{P}$, $\overline{G}$, C_{n+4}			2.5	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	I/O	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
				I_{OL}=24 mA					0.35	0.5	
		LI/RO, RI/LO, C_{n+4}		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
				I_{OL}=8 mA					0.35	0.5	
		$\overline{P}$		I_{OL}=8 mA		0.35	0.5		0.35	0.5	
		$\overline{G}$		I_{OL}=16 mA		0.35	0.5		0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	I/O, LI/RO, RI/LO	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=2.7 V				40			40	μA
I_{OZL}	Off-state output current, low-level voltage applied	I/O, LI/RO	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=0.4 V				−800			−800	μA
		RI/LO					−400			−400	
I_I	Input current at maximim input voltage	All I/O	V_{CC}=MAX	V_I=5.5 V			0.1			0.1	mA
		C_n		V_I=7 V			0.5			0.5	
		All others					0.1			0.1	
I_{IH}	High-level input current	C_n	V_{CC}=MAX, V_I=2.7 V				100			100	μA
		All I/O					40			40	
		All others					20			20	
I_{IL}	Low-level input current	C_n	V_{CC}=MAX, V_I=0.4 V				−4			−4	mA
		I/O, LI/RO					−0.8			−0.8	
		CLK					−0.2			−0.2	
		All others					−0.4			−0.4	
I_{OS}	Short-circuit output current§	I/O	V_{CC}=MAX		−30		−130	−30		−130	mA
		LI/RO, RI/LO, $\overline{P}$, $\overline{G}$, C_{n+4}			−20		−100	−20		−100	
I_{CC}	Supply current		V_{CC}=MAX, RS0 at 4.5 V, All other I/O at 0 V			100			100	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operations.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	CLOCK↑	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		25	40	ns
t_{PHL}						30	45	
t_{PLH}		$\overline{G}$				26	40	ns
t_{PHL}						27	40	
t_{PLH}		I/O				27	40	ns
t_{PHL}						29	40	
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		36	55	ns
t_{PHL}						34	50	
t_{PLH}		LI/RO				25	40	ns
t_{PHL}						23	35	
t_{PLH}		RI/LO				19	30	ns
t_{PHL}						17	30	
t_{PLH}	AS0-AS2	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		30	45	ns
t_{PHL}						30	45	
t_{PLH}		$\overline{G}$				27	35	ns
t_{PHL}						28	35	
t_{PLH}		I/O				31	45	ns
t_{PHL}						29	45	
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		39	55	ns
t_{PHL}						34	50	
t_{PLH}	C_n	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		9	25	ns
t_{PHL}						9	20	
t_{PLH}		I/O				17	35	ns
t_{PHL}						13	20	
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		20	30	ns
t_{PHL}						16	25	
t_{PLH}	MODE	$\overline{P}$	R_L = 667 Ω,	C_L = 45 pF		28	40	ns
t_{PHL}						29	40	
t_{PLH}		$\overline{G}$				21	30	ns
t_{PHL}						23	30	
t_{PLH}		I/O				30	45	ns
t_{PHL}						28	40	
t_{PLH}		C_{n+4}	R_L = 2 kΩ,	C_L = 15 pF		40	60	ns
t_{PHL}						37	50	
t_{PZH}	RS0-RS2	I/O	R_L = 667 Ω	C_L = 45 pF		28	45	ns
t_{PZL}						28	45	
t_{PHZ}				C_L = 5 pF		35	50	ns
t_{PLZ}						39	50	
t_{PZH}		LI/RO	R_L = 2 kΩ	C_L = 15 pF		25	40	ns
t_{PZL}						22	40	
t_{PHZ}				C_L = 5 pF		21	30	ns
t_{PLZ}						34	50	
t_{PZH}		RI/LO	R_L = 2 kΩ	C_L = 15 pF		22	40	ns
t_{PZL}						24	40	
t_{PZH}				C_L = 5 pF		11	30	ns
t_{PZL}						16	40	

NOTE 2: For load circuit and voltage waveforms see page 3-11

t_{PLH} ≡ Propagation delay time, low-to-high-level input
t_{PHL} ≡ Propagation delay time, high-to-low-level input
t_{PZL} ≡ Output enable time to low level
t_{PZH} ≡ Output enable time to high level
t_{PLZ} ≡ Output disable time from low level
t_{PHZ} ≡ Output disable time from high level

TYPES SN54LS682 THRU SN54LS689, SN74LS682 THRU SN74LS689 8-BIT MAGNITUDE COMPARATORS

REVISED MARCH 1984

- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 and 'LS683 have 20-kΩ Pullup Resistors on the Q Inputs
- 'LS686 and 'LS687 . . . New JT and NT 24-Pin, 300-Mil Packages
- 'LS682 is equivalent to 25LS2821
- 'LS688 is equivalent to 25LS2521

TYPE	$\overline{P=Q}$	$\overline{P>Q}$	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS683	yes	yes	no	open-collector	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
'LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no
'LS689	yes	no	yes	open-collector	no

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P=Q}$ outputs and the 'LS682 thru 'LS687 provide $\overline{P>Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS683, 'LS685, 'LS687, and 'LS689 have open-collector outputs. The 'LS682 and 'LS683 feature 20-kΩ pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

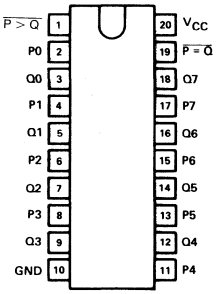
INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{G1}$	$\overline{G2}$	$\overline{P=Q}$	$\overline{P>Q}$
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = high level, L = low level, X = irrelevant

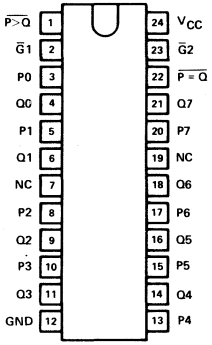
NOTES: 1. The last line of function table applies only to those devices having enable inputs, i.e., 'LS686 thru 'LS689.

2. The $\overline{P<Q}$ function can be generated by applying the $\overline{P=Q}$ and $\overline{P>Q}$ outputs to a 2-input NAND gate.

SN54LS682 THRU SN54LS685 . . . J PACKAGE
SN74LS682 THRU SN74LS685 . . . J OR N PACKAGE
(TOP VIEW)

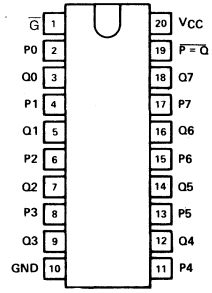


SN54LS686, SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . JT OR NT PACKAGE
(TOP VIEW)



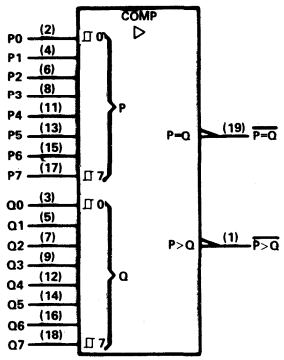
NC = no connection

SN54LS688, SN54LS689 . . . J PACKAGE
SN74LS688, SN74LS689 . . . J OR N PACKAGE
(TOP VIEW)

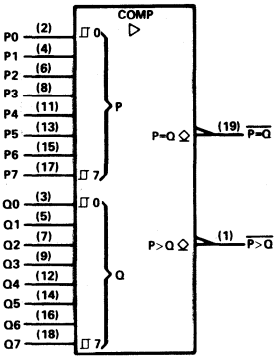


logic symbols

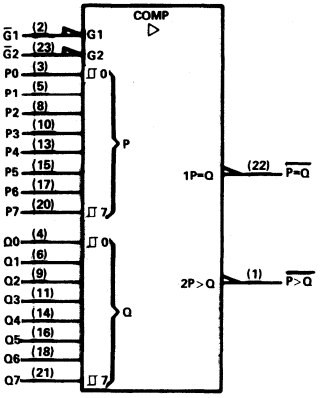
'LS682, 'LS684



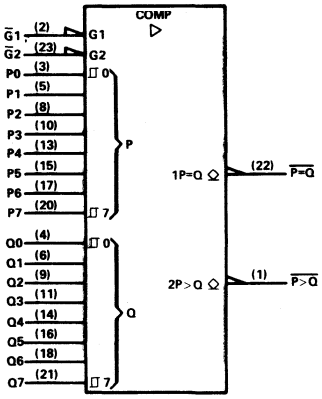
'LS683, 'LS685



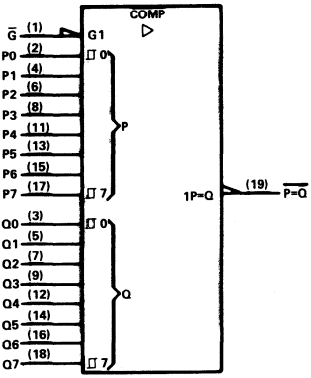
'LS686



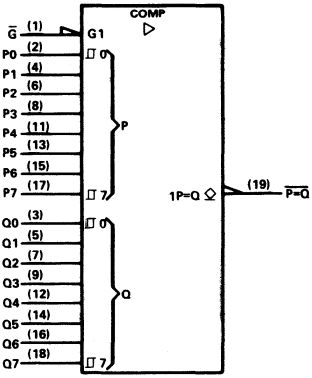
'LS687



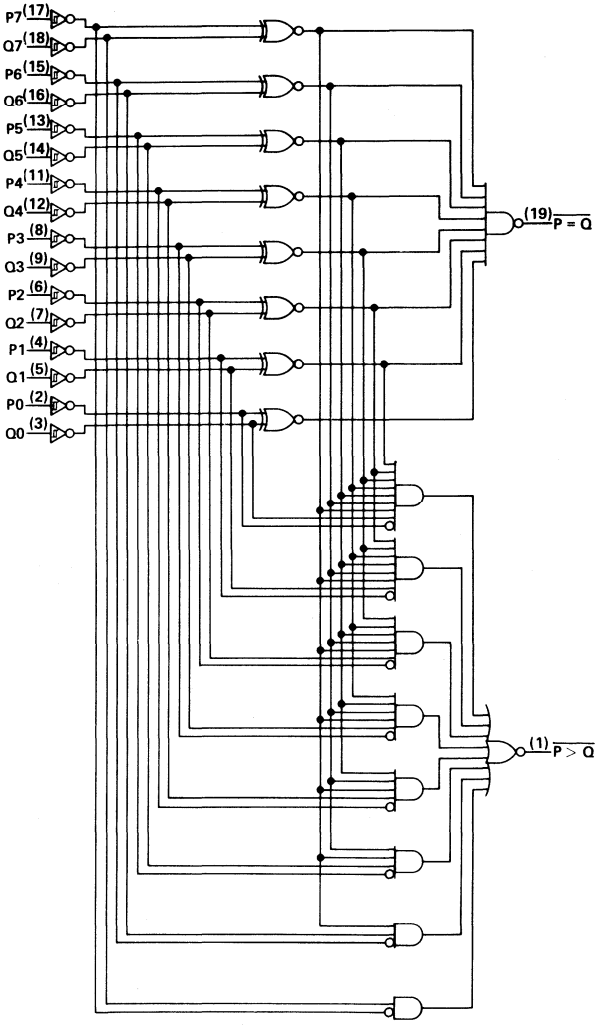
'LS688



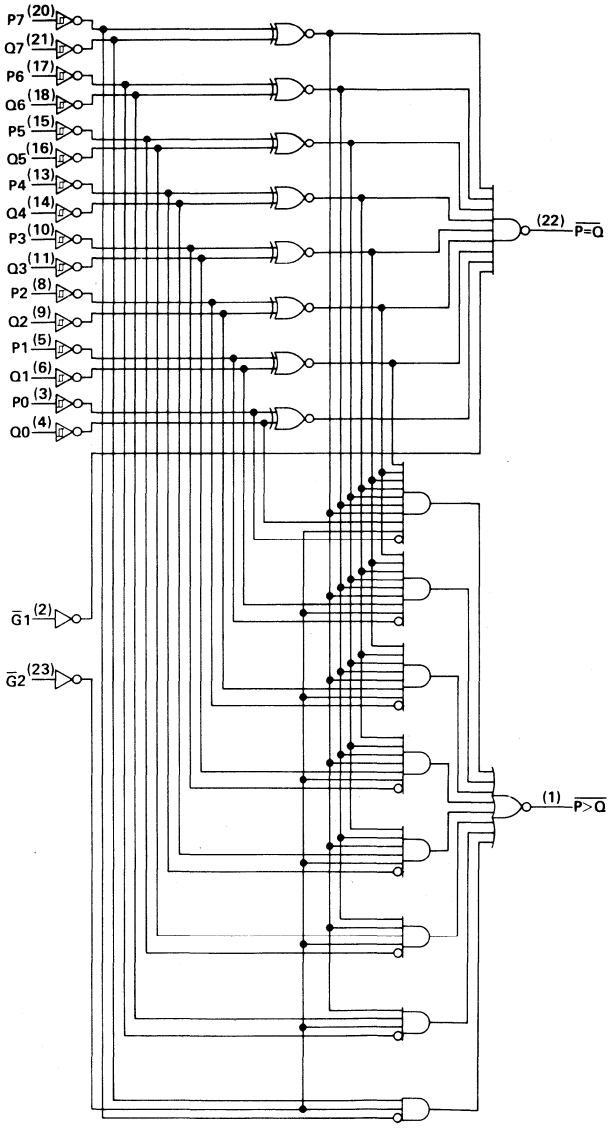
'LS689



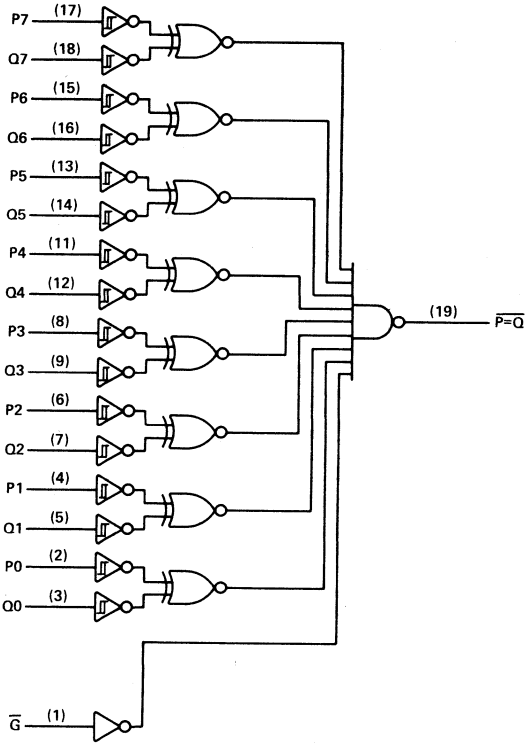
'LS682 thru 'LS685 functional block diagram (positive logic)



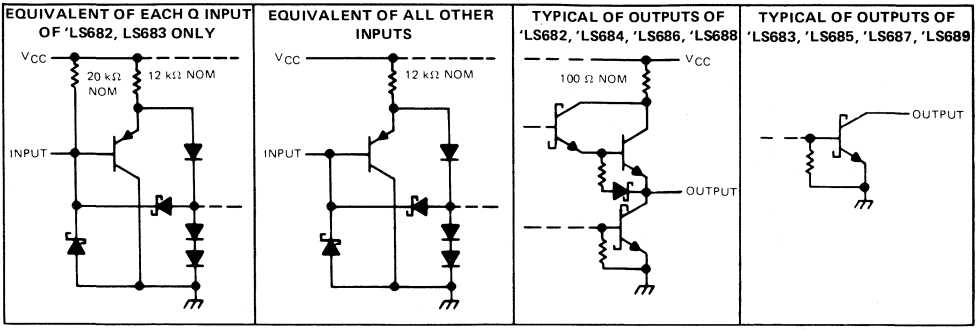
'LS686, 'LS687 functional block diagram (positive logic)



'LS688, 'LS689 functional block diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage: Q inputs of 'LS682 and 'LS683	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS683, 'LS685, 'LS687, 'LS689	5.5 V
Operating free-air temperature range: SN54LS682 thru SN54LS689	−55°C to 125°C
SN74LS682 thru SN74LS689	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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'LS682, 'LS684, 'LS686, 'LS688

recommended operating conditions

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{OS}	Short-circuit output current¶		V_{CC} = MAX,	V_O = 0	−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS682	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS684				40	65		40	65	
		'LS686				44	75		44	75	
		'LS688				40	65		40	65	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		13	25		15	25		13	25		12	18	ns
t_{PHL}					15	25		17	25		20	30		17	23	
t_{PLH}	Q	$\overline{P=Q}$			14	25		16	25		13	25		12	18	ns
t_{PHL}					15	25		15	25		21	30		17	23	
t_{PLH}	$\overline{G}$, $\overline{G1}$	$\overline{P=Q}$									11	20		12	18	ns
t_{PHL}											19	30		13	20	
t_{PLH}	P	$\overline{P>Q}$			20	30		22	30		19	30				ns
t_{PHL}					15	30		17	30		15	30				
t_{PLH}	Q	$\overline{P>Q}$			21	30		24	30		18	30				ns
t_{PHL}					19	30		20	30		19	30				
t_{PLH}	$\overline{G2}$	$\overline{P>Q}$									21	30				ns
t_{PHL}											16	25				

#t_{PLH} ≡ propagation delay time, low-to-high-level outputs; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 3: Load circuit and waveforms are shown on page 3-11

recommended operating conditions 'LS683, 'LS685, 'LS687, 'LS689

PARAMETER	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			100	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{CC}	Supply current	'LS683	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS685				40	65		40	65	
		'LS687				44	75		44	75	
		'LS689				40	65		40	65	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with any G inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS683			'LS685			'LS687			'LS689			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P=Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		30	45		30	45		24	35		24	40	ns
t_{PHL}					20	30		19	35		20	30		22	35	
t_{PLH}	Q	$\overline{P=Q}$			24	35		24	45		24	35		24	40	ns
t_{PHL}					23	35		23	35		20	30		22	35	
t_{PLH}	$\overline{G}$, $\overline{G1}$	$\overline{P=Q}$									21	35		22	35	ns
t_{PHL}											18	30		19	30	
t_{PLH}	P	$\overline{P>Q}$			31	45		32	45		24	35				ns
t_{PHL}					17	30		16	35		16	30				
t_{PLH}	Q	$\overline{P>Q}$			30	45		30	45		24	35				ns
t_{PHL}					21	30		20	35		16	30				
t_{PLH}	$\overline{G2}$	$\overline{P>Q}$									24	35				ns
t_{PHL}											15	30				

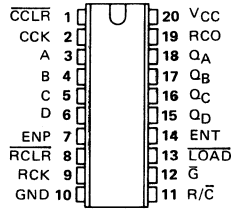
¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 3: Load circuit and waveforms are shown on page 3-11

TYPES SN54LS690 THRU SN54LS693, SN74LS690 THRU SN74LS693
SYNCHRONOUS COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2423, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Stored Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS690 . . Decade Counter, Direct Clear
  'LS691 . . Binary Counter, Direct Clear
  'LS692 . . Decade Counter, Synchronous Clear
  'LS693 . . Binary Counter, Synchronous Clear

SN54LS690 THRU SN54LS693 . . . J PACKAGE
SN74LS690 THRU SN74LS693 . . . J OR N PACKAGE
(TOP VIEW)



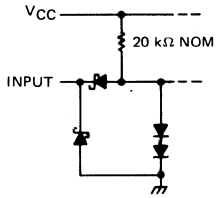
description

These low-power Schottky LSI devices incorporate synchronous counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The counters can be programmed from the data inputs and have enable P and enable T inputs and a ripple-carry output for easy expansion. The register/counter select input, R/$\overline{C}$, selects the counter when low or the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus-driving performance.

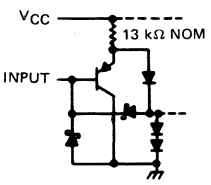
Individual clock and clear inputs are provided for both the counter and the register. Both clock inputs are positive-edge triggered. The clear line is active low and is asynchronous on the 'LS690 and 'LS691, synchronous on the 'LS692 and 'LS693.

schematics of inputs and outputs

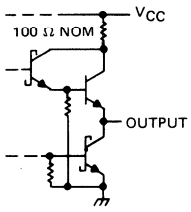
EQUIVALENT OF A, B, C, D INPUTS



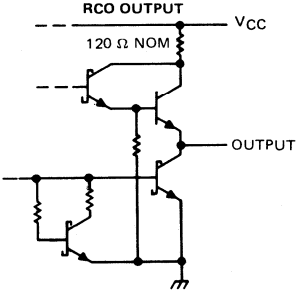
EQUIVALENT OF ALL OTHER INPUTS



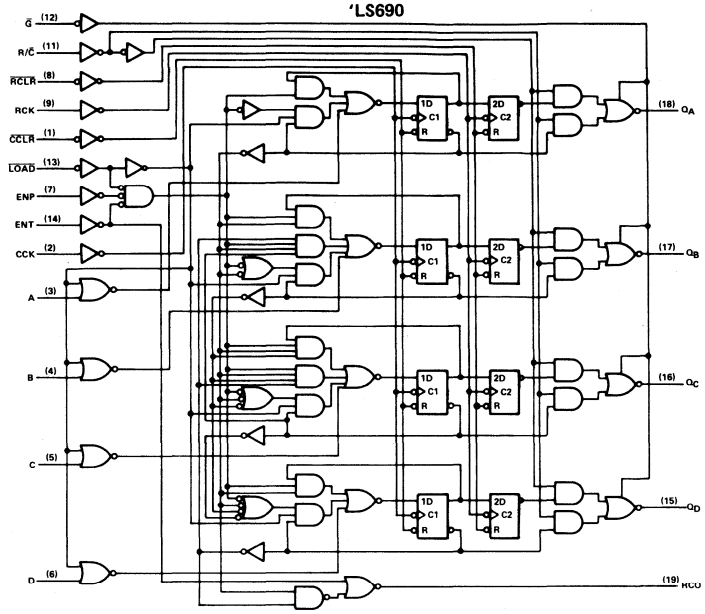
TYPICAL OF ALL Q OUTPUTS



RCO OUTPUT



'LS690



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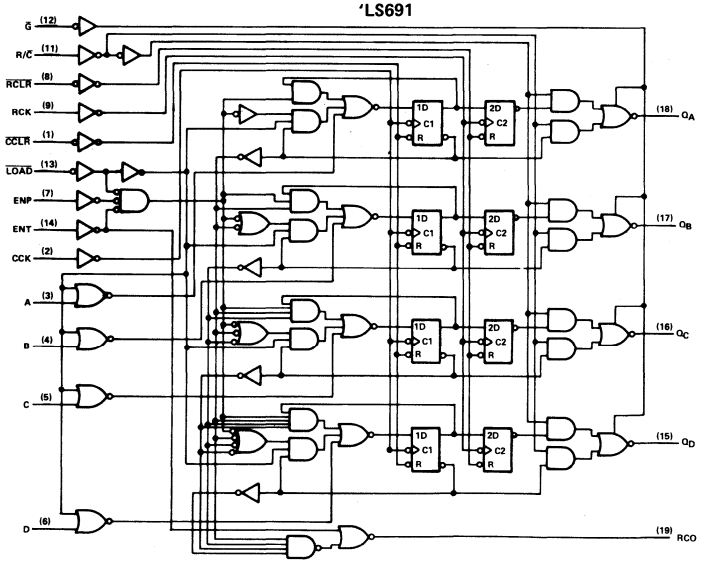

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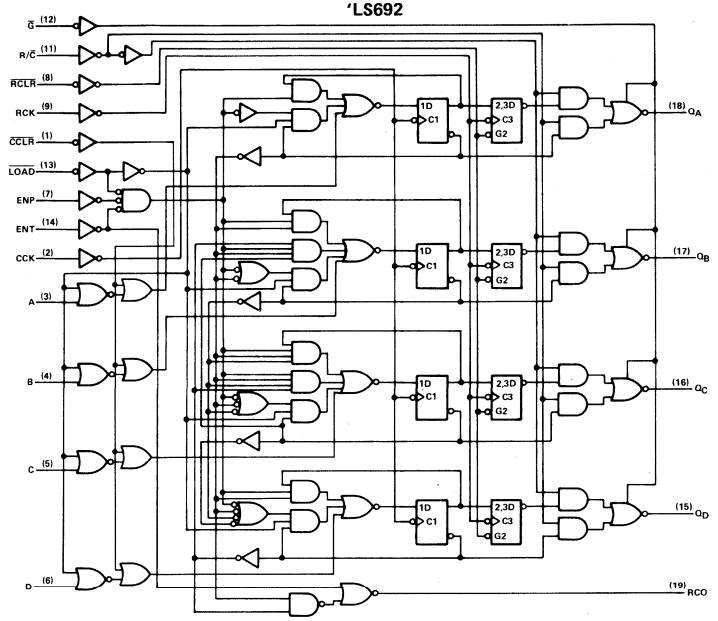
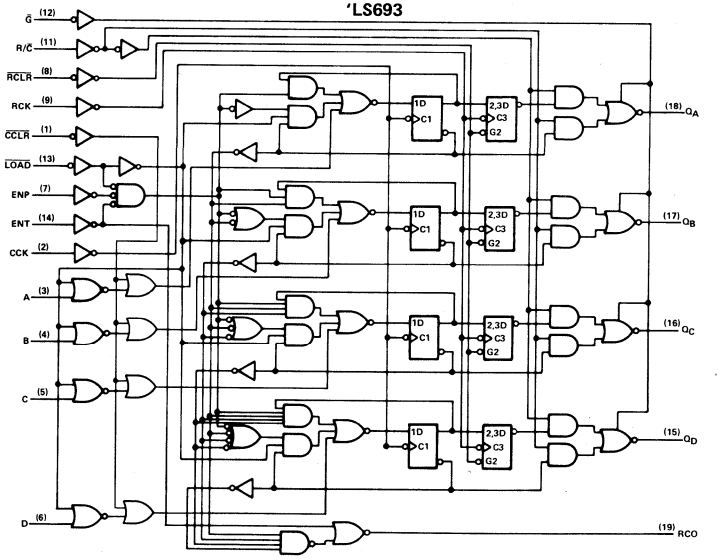
'LS692

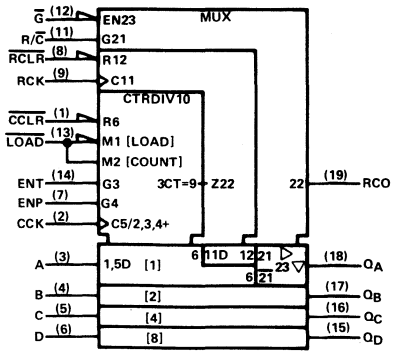

G (12)
R/C (11)
RCLR (8)
RCK (9)
CCLR (1)
LOAD (13)
ENP (7)
ENT (14)
CCK (2)
A (3)
B (4)
C (5)
D (6)
1D
C1
2,3D
C3
G2
(18) QA
(17) QB
(16) QC
(15) QD
(19) RCO

'LS693


G (12)
R/C (11)
RCLR (8)
RCK (9)
CCLR (1)
LOAD (13)
ENP (7)
ENT (14)
CCK (2)
A (3)
B (4)
C (5)
D (6)
1D
C1
2,3D
C3
G2
(18) QA
(17) QB
(16) QC
(15) QD
(19) RCO

logic symbols

'LS690



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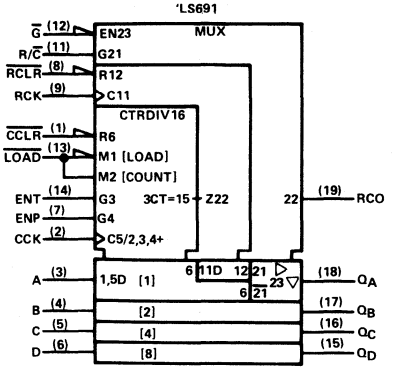
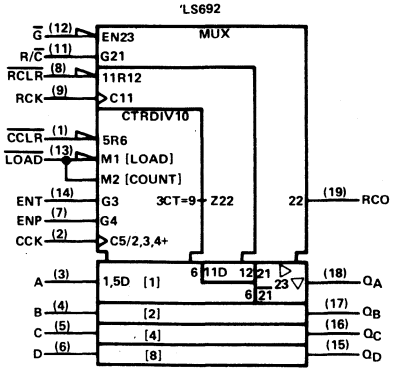


'LS692



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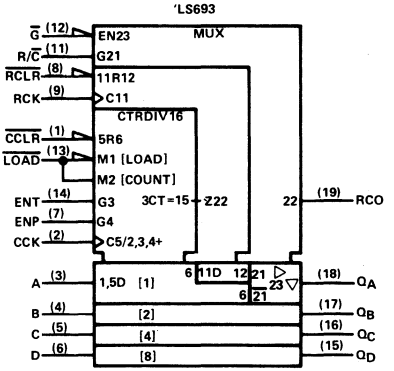


absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS690 thru SN54LS693 . . . . . −55°C to 125°C
SN74LS690 thru SN74LS693 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}		Q			−1			−2.6	mA
		RCO			−400			−400	μA
Low-level output current, I_{OL}		Q			12			24	mA
		RCO			4			8	mA
Clock frequency, f_{clock}		CCK	0		20	0		20	MHz
		RCK	0		20	0		20	MHz
Width of clock pulse, t_w (high or low)		CCK	25			25			ns
		RCK	25			25			ns
Setup time, t_{su}		A-D to CCK↑	30			30			ns
		Enable P or T to CCK↑	30			30			ns
	'LS692, 'LS693 only	$\overline{CCLR}$↓ to CCK↑	20			20			ns
	'LS692, 'LS693 only	$\overline{RCLR}$↓ to RCK↑	20			20			ns
Hold time, t_h	Any input from CCK↑ or RCK↑		0			0			ns
Operating free-air temperature, T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		RCO		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		RCO		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		RCO		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, V_{IH}=2 V, V_{IL}=V_{IL} max, V_O=0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		RCO			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 2		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 3		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 4		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

NOTES: 2. I_{CCH} is measured after two 4.5-V to 0-V to 4.5-V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.

3. I_{CCL} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while all other inputs are grounded.

4. I_{CCZ} is measured after two 0-V to 4.5-V to 0-V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS690, 'LS691			'LS692, 'LS693			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CCK↑	RCO	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	
t_{PLH}	ENT	RCO			13	20		13	20	ns
t_{PHL}					13	20		13	20	
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	$\overline{RCLR}$↓	Q			20	30				ns
t_{PHL}	CCK↑	Q (CLEAR)						23	40	ns
t_{PHL}	RCK↑	Q (CLEAR)						20	30	ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	

NOTE 5: Load circuit and voltage waveforms are shown on page 3-11

t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

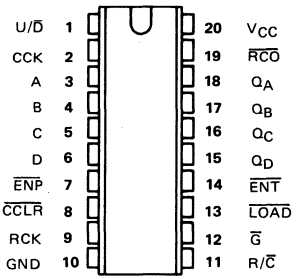
7

TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2424, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Stored Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . Decade Counter, Direct Clear
  'LS697 . . Binary Counter, Direct Clear
  'LS698 . . Decade Counter, Synchronous Clear
  'LS699 . . Binary Counter, Synchronous Clear

SN54LS696 THRU SN54LS699 . . J PACKAGE
SN74LS696 THRU SN74LS699 . . J OR N PACKAGE
(TOP VIEW)

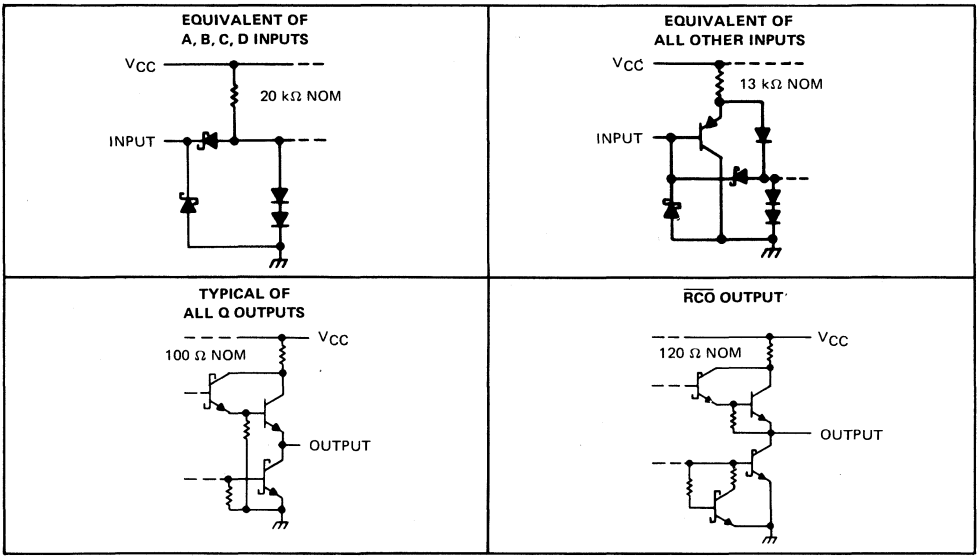


description

These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable $\overline{P}$ and enable $\overline{T}$ and a ripple-carry output for easy expansion. The register/counter select input R/$\overline{C}$, selects the counter when low and the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

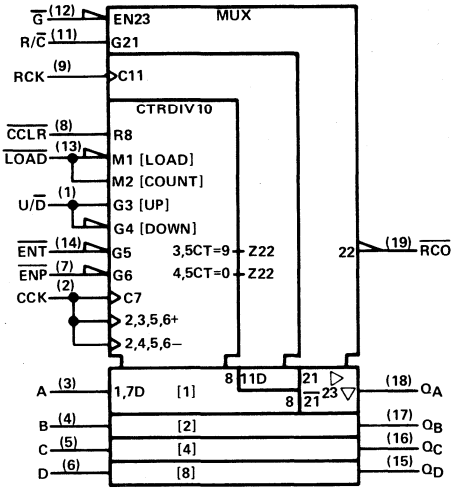
Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear $\overline{CCLR}$ is active low and is asynchronous on the 'LS696 and 'LS697, synchronous on the 'LS698 and 'LS699.

schematics of inputs and outputs

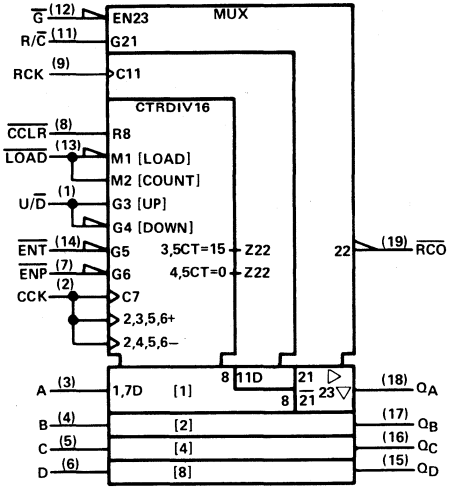


logic symbols

'LS696



'LS697



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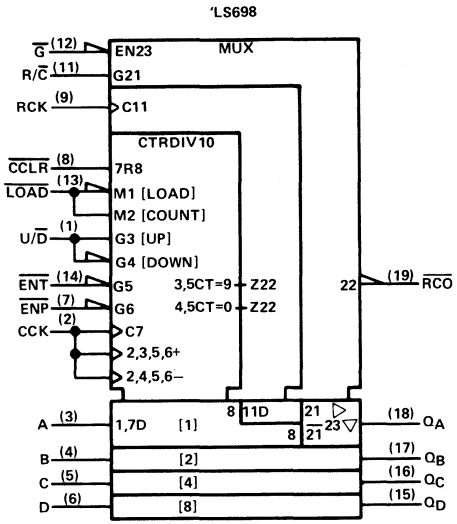

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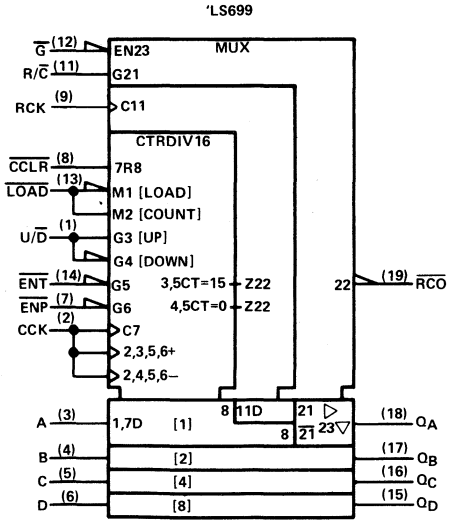
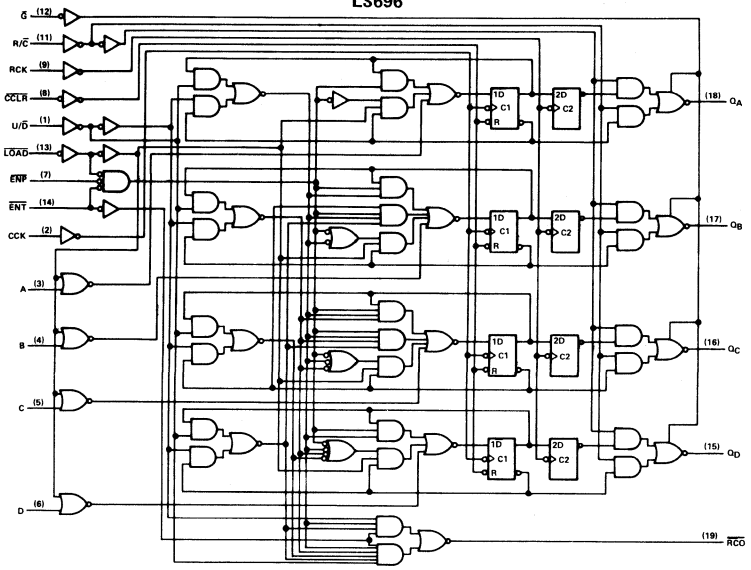


7

functional block diagrams

'LS696



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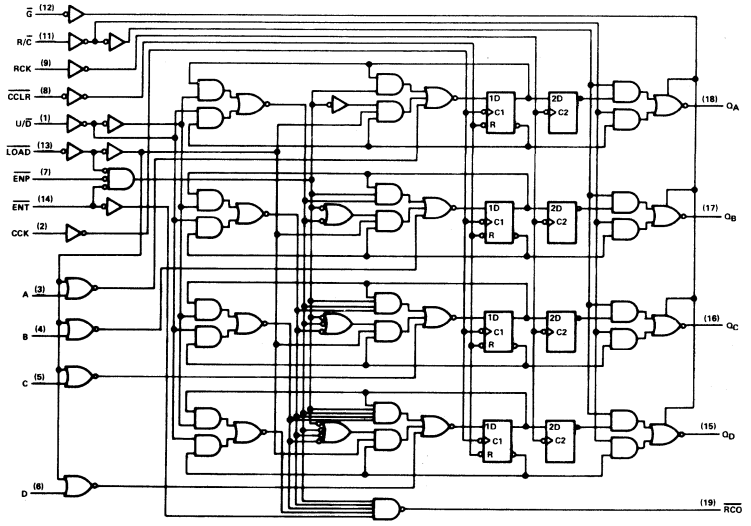
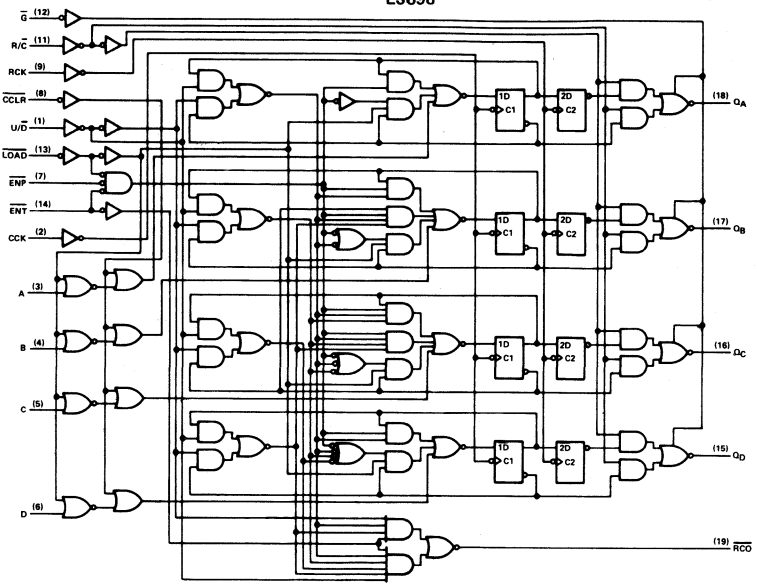
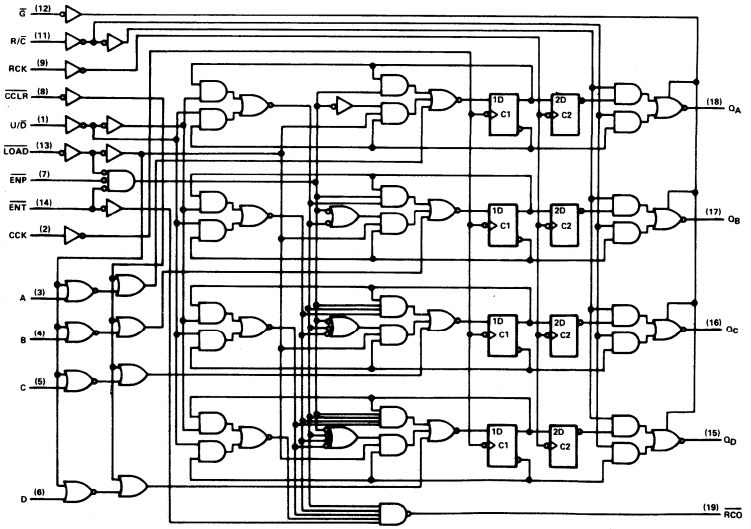


functional block diagrams

'LS698



'LS699



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS696 thru SN54LS699 . . . . . −55°C to 125°C
SN74LS696 thru SN74LS699 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q			−1			−2.6	mA
	$\overline{RCO}$			−400			−400	μA
Low-level output current, I_{OL}	Q			12			24	mA
	$\overline{RCO}$			4			8	
Clock frequency, f_{clock}	CCK	0		20	0		20	MHz
	RCK	0		20	0		20	
Width of clock pulse, t_w (high or low)	CCK	25			25			ns
	RCK	25			25			
Setup time, t_{su}	A-D to CCK↑	30			30			ns
	Enable $\overline{P}$ or $\overline{T}$ to CCK↑	30			30			
	U/$\overline{D}$ to CCK↑	35			35			
	'LS698, 'LS699, $\overline{CCLR}$ to CCK↑	20			20			
Hold time, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC}=MIN, I_I=−18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OH}=−1 mA	2.4	3.1					V
		Any Q		I_{OH}=−2.6 mA				2.4	3.1		
		$\overline{RCO}$		I_{OH}=−400 μA	2.5	3.2		2.7	3.2		
V_{OL}	Low-level output voltage	Any Q	V_{CC}=MIN, V_{IH}=2 V, V_{IL}=V_{IL} max	I_{OL}=12 mA		0.25	0.4		0.25	0.4	V
		Any Q		I_{OL}=24 mA					0.35	0.5	
		$\overline{RCO}$		I_{OL}=4 mA		0.25	0.4		0.25	0.4	
		$\overline{RCO}$		I_{OL}=8 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V, V_O=2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	Any Q	V_{CC}=MAX, $\overline{G}$ at 2 V, V_O=0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage		V_{CC}=MAX, V_I=7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC}=MAX, V_I=2.7 V				20			20	μA
I_{IL}	Low-level input current	A thru D	V_{CC}=MAX, V_I=0.4 V				−0.4			−0.4	mA
		All others					−0.2			−0.2	
I_{OS}	Short-circuit output current§	Any Q	V_{CC}=MAX, V_O=0 V		−30		−130	−30		−130	mA
		$\overline{RCO}$			−20		−100	−20		−100	
I_{CCH}	Supply current, outputs high		V_{CC}=MAX, All outputs open	See Note 2		46	65		46	65	mA
I_{CCL}	Supply current, outputs low			See Note 3		48	70		48	70	
I_{CCZ}	Supply current, outputs off			See Note 4		48	70		48	70	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 2. I_{CCH} is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while $\overline{G}$ is grounded and all other inputs are at 4.5 V.

3. I_{CCL} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.

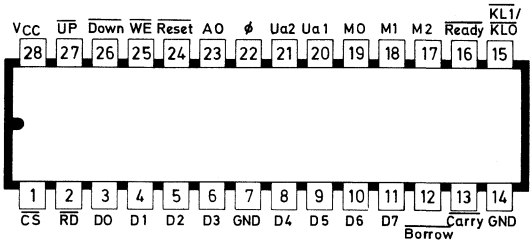
4. I_{CCZ} is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while $\overline{G}$ is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697 MIN	'LS696, 'LS697 TYP	'LS696, 'LS697 MAX	'LS698, 'LS699 MIN	'LS698, 'LS699 TYP	'LS698, 'LS699 MAX	UNIT
t_{PLH}	CCK↑	$\overline{RCO}$	R_L = 2 kΩ, C_L = 15 pF		23	40		23	40	ns
t_{PHL}					23	40		23	40	ns
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$			13	20		13	20	ns
t_{PHL}					13	20		13	20	ns
t_{PLH}	CCK↑	Q	R_L = 667 Ω, C_L = 45 pF		12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PLH}	RCK↑	Q			12	20		12	20	ns
t_{PHL}					17	25		17	25	ns
t_{PHL}	$\overline{CCLR}$↓	Q			23	40				ns
t_{PHL}	CCK↑	Q (CLEAR)						17	25	ns
t_{PLH}	R/$\overline{C}$	Q			16	25		16	25	ns
t_{PHL}					16	25		16	25	ns
t_{PZH}	$\overline{G}$↓	Q			19	30		19	30	ns
t_{PZL}					19	30		19	30	ns
t_{PHZ}	$\overline{G}$↑	Q	R_L = 667 Ω, C_L = 5 pF		17	30		17	30	ns
t_{PLZ}					17	30		17	30	ns

TYPE SN74LS2000
(DIRECTION DISCRIMINATOR)

J OR N PACKAGE



Features

- **Direction Discriminator to identify forward/backward direction.**
- **Separate 16 BIT cascadable up/down counter.**
- **Pulse-width measurement with either forward or backward counting.**
- **Frequency measurement.**
- **8-Bit parallel tri-state data bus.**
- **Simple write and read procedure.**
- **All inputs and outputs TTL compatible.**
- **Single +5 Volt supply.**

INTRODUCTION

The SN74LS2000N DIRECTION DISCRIMINATOR is a device designed for use with TEXAS INSTRUMENTS or other microprocessors in all kinds of applications where it is required to evaluate the output signals, received from an incremental length measurement system or any other incremental transducer. (like robots, automatic turning lathe, etc. . . .).

Additional features allow it to be used also in microprocessor-systems where automatically pulse-width, frequency measurement or up/down counting is required.

The SN74LS2000N is a 28 Pin, single supply (+5 V_{CC}), low power schottky array technology device, with all inputs and outputs – TTL compatible.

SPECIFICATION AND FUNCTIONAL DESCRIPTION

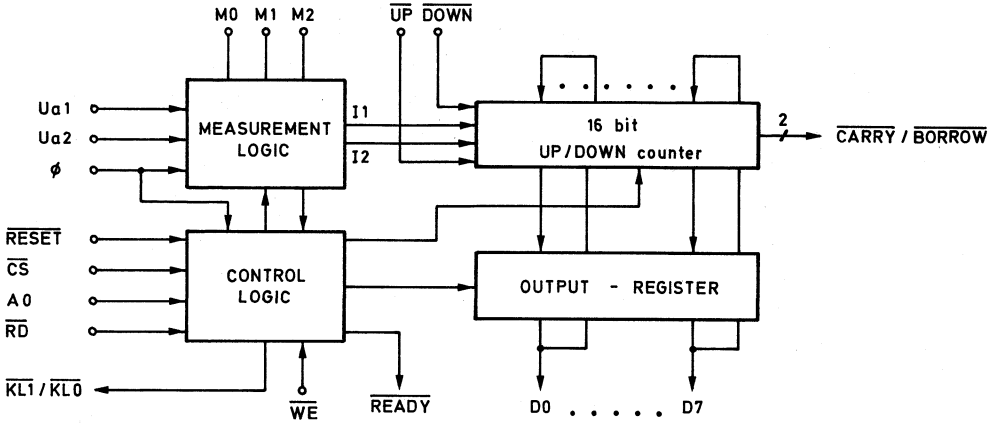
Architecture

Figure 2-1 shows the functional block-diagram of the SN74LS2000N. The direction discriminator consists of the measurement-logic, control-logic, 16 BIT up/down counter and output-register. The measurement-logic generates, depending on the input signals Ua1, Ua2 and the mode state, the internal I1/I2 pulses for the up/down count.

The control-logic circuitry is the interface between controlsignals of the processor and the SN74LS2000N. This logic generates internal control signals to prevent faultless behavior of the device.

The output-register, which operates as a one word memory for the 16 BIT evaluated information, prevents wrong information to be read in consequence of the 2 Byte reading operation. In both the pulse-width and the frequency measurement mode it enables the measurement circuitry to make a new sample.

Figure 2-1



Mode Selection

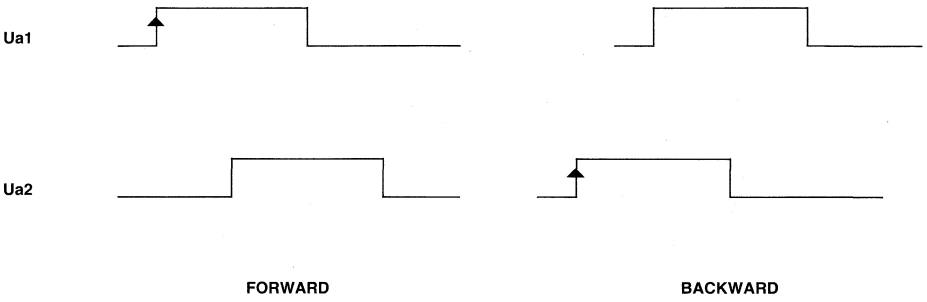
Table 2-1 shows the different mode functions of the SN74LS2000N. (see also fig. 2-2)

Table 2-1

M2	M1	M0	MODE DESCRIPTION
			Direction Discriminator
0	0	0	direction discriminator inhibit
0	0	1	single count pulse, synchronous with Ua1
0	1	0	single count pulse, synchronous with Ua2
0	1	1	double count pulse, synchronous with Ua1
1	0	0	double count pulse, synchronous with Ua2
1	0	1	quadruple counting
1	1	0	**Pulse width measurement** 1. Ua1 = gate signal Ua2 'H' = up counting 2. Ua1 = gate signal Ua2 'L' = down counting
1	1	1	**Frequency measurement** Ua1 = frequency to be measured Ua2 = start/stop gate

Direction Discriminator Mode

For each of the various direction discriminator modes (see table 2-1) the direction counting is identified by the low to high transition of the input signals Ua1, Ua2. Ua1 leading/lagging Ua2 means up/down counting.



The positive transition of the input signal Ua1 is stored in the first of 2 consecutive flip-flops and is transferred to the second flip-flop with the next edge of the clock pulse. The same principle applies for Ua2. From the state of these 4 flip-flops it is possible (out of the 8 relevant cases) to identify the direction and generate the up/down count pulses. The pulse diagram of fig. 2-2 shows the various signals of the direction discriminator. Each edge of the signals Ua1 and Ua2, depending on the mode, will result in a I1 (up) and I2 (down) count pulse.

The control-logic generates from the input signal $\overline{CS}$ (chip-select) and AO (byte-select) a load pulse for the output-register. An internal cirucuitry decides, if the least-significant-byte (AO high level) or the most-significant-byte (AO low level) should generate the load pulse; therefore all different kinds of microprocessor can be used.

During the load process the content of the counter is not affected. The load procedure can also be controlled from the I/O $\overline{KLI/KLO}$ pin (cascade-load-input/cascade-load-output). The same pin is used for both functions. After $\overline{RESET}$ being active, KLO is available upon first time $\overline{CS}$ and AO being active and remains so. If $\overline{KLI}$ becomes active after $\overline{RESET}$, the load procedure via $\overline{CS}$ and AO is not affected (see fig. 2-3).

Those functions are necessary where more than 16 BIT accuracy is needed and the store process should be performed in one movement. (see system application).

Loading the counter is possible at any value by activating $\overline{CS}$, WRITE ENABLE ($\overline{WE}$) and AO.
Reading the content of the counter is possible by activating $\overline{CS}$, READ ($\overline{RD}$) and AO.

figure 2-2

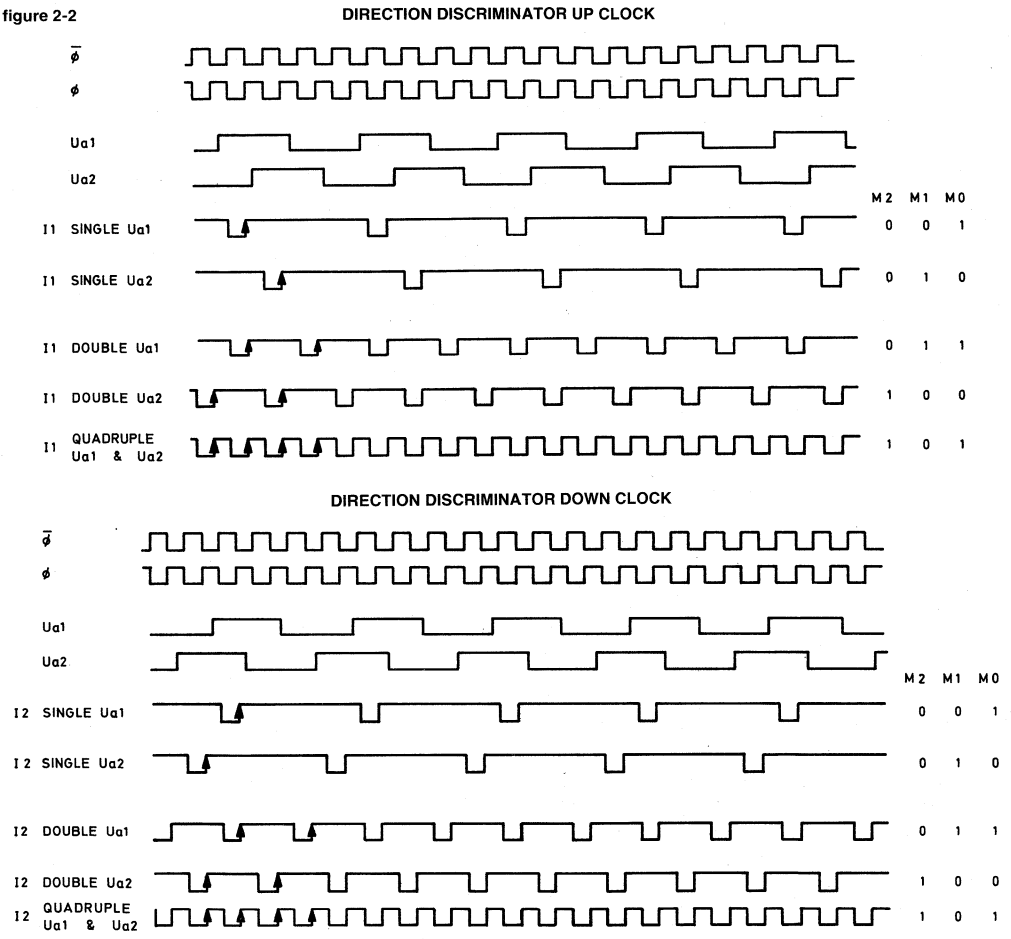
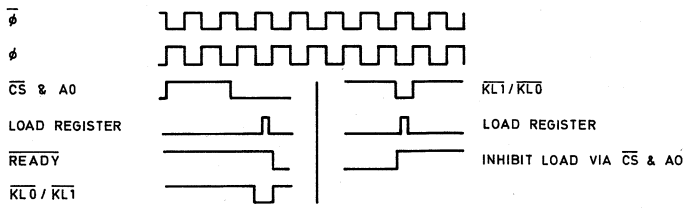


figure 2-3



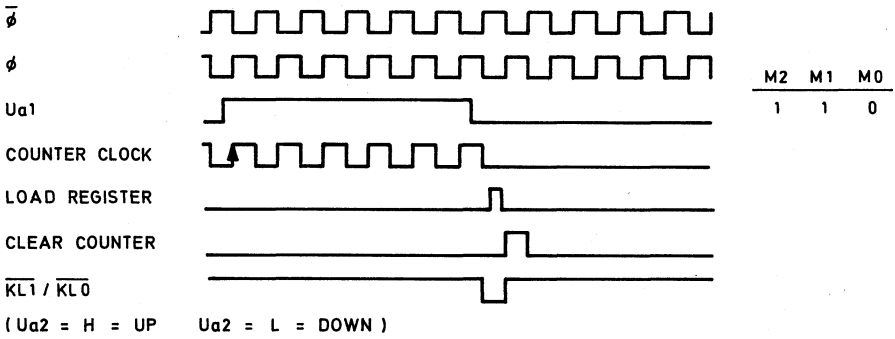
Pulse Width/Time Measurement Mode

In this mode the pulse width is measured (see fig. 2-4) when Ua1 (input for pulse width measurement) changes from low to high and depending on the input level at Ua2 being high/low, the 16 BIT counter will count up/down. Changing the input signal Ua1 from high to low will result in loading the content of the counter into the output-register and it also clears the counter.

The data from the output-register can be read at any time by activating $\overline{CS}$, $\overline{RD}$ and AO.

Loading the counter is possible by having $\overline{CS}$, $\overline{WE}$ and AO active. To prevent wrong measurement, it is necessary to load the counter during a low level input signal at Ua1. Reading the register should take place before the next load input. This can easily be solved with a processor in interrupt mode ($\overline{KLO}$ will be used as the interrupt signal).

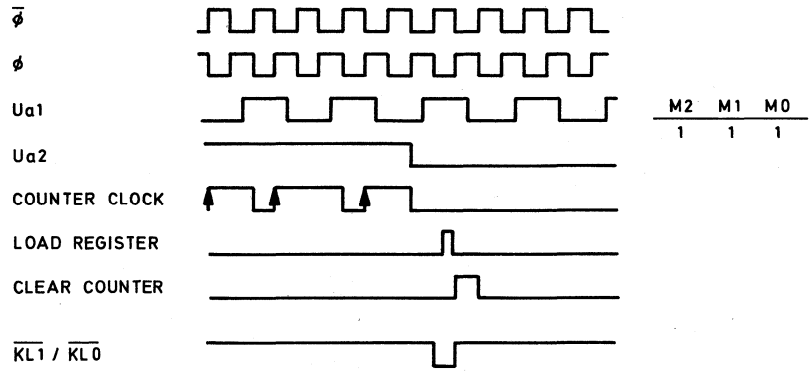
figure 2-4



Frequency Mesurement Mode

In this mode the input pin Ua1 is used as frequency signal input and the input Ua2 as the gate. When Ua2 is high, the input signal at Ua1 is counted. The information in the counter is transferred to the output-register with the trailing edge of the input signal on Ua2 and the counter is reset (see pulse diagram 2-5).
Read or write of data uses the same procedure as described for direction discriminator mode.

diagram 2-5



Up/Down Counter Mode

The SN74LS2000N can also be used as a fast 16 BIT up/down counter with cascade capability. Loading is as described for direction discriminator or frequency measurement modes. In this mode the Ø Clock) should be connected either to the $\overline{UP}$ or $\overline{DOWN}$ input.

Pin Description

Table 2-2 defines the SN74LS2000N pin assignment and describes each pin.

Table 2-2

SIGNATURE	PIN	I/O	DESCRIPTION
V_{CC}	28		Supply voltage. 5 V DC ± 5 %
GND	7. 14		Ground. Reference
$\overline{RESET}$	24	IN	DEVICE RESET. When $\overline{RESET}$ is active (low). the control-logic is reset to a known state and the counter will be cleared.
MO-M2	19–17	IN	Mode inputs
Ua1 – Ua2	20. 21	IN	Measuring input signals
$\overline{UP}$	27	IN	Cascade input for count up.
$\overline{DOWN}$	26	IN	Cascade input for count down.
$\overline{CARRY}$	13	OUT	Overflow signal.
$\overline{BORROW}$	12	OUT	Underflow signal.
$\overline{CS}$	1	IN	CHIP-SELECT. When CS is inactive (high). the data bus is at HI-$\overline{Z}$ level. In the direction discriminator modes this signal together with AO generates the load pulse.
D0 – D7	3–6. 8–11	IN/OUT	Register I/O lines.
$\overline{RD}$	2	IN	READ. When $\overline{RD}$ is active (low). the data from the OUTPUT-REGISTER will be present on the data bus.
$\overline{WE}$	25	IN	WRITE-ENABLE. When $\overline{WE}$ is an active low signal. that performs the function of storing write data from the data-bus.
	22	IN	CLOCK. This input is used for internal synchronisation and controls timing.
$\overline{READY}$	16	OUT	READY. $\overline{READY}$ is an output signal which. when active (low). indicates to the processor that it can complete its read or write operation. $\overline{READY}$ is synchronous to the Ø clock.
$\overline{KLI}/\overline{KLO}$	15	IN/OUT	CASCADE-LOAD-INPUT/CASCADE-LOAD-OUTPUT.
AO	23	IN	BYTE SELECT. AO high selects the least significant byte. AO low the most significant.

Timing/Frequency Limits

Ø-Input

The maximum allowable signal frequency at Ø is 20 MHz.

Ua1, Ua2 Inputs (Direction Discriminator Mode)

Frequency of the input signals Ua1 and Ua2 in the direction discriminator modes is calculated as follows:

$$F = \frac{\text{SHAFTSPEED}}{\text{RESOLUTION OF TRANSDUCER}}$$

EXAMPLE:

$$F = \frac{30\ m/min}{4\ \mu m} = 125\ KHz \qquad T = 8\ \mu S$$

It is recommended to use a frequency of the clock input Ø which is at least 4 times higher than the frequency of the signals at inputs Ua1 and Ua2. This will prevent problems occuring from jitter of the transducer signal and also gives the opportunity to work in the quadruple counting mode.

Pulse Width Measurement Timing

In the pulse width mode the minimum time that can be measured is:

$$T_{min} = 2 \times T\emptyset$$

with the resolution:

$$T_a = T\emptyset \pm LSB$$

accuracy ± LSB.

Frequency Measurement Time (Ua2)

The maximum frequency that can be measured is:

$$F_{max} = \frac{F\emptyset}{2}$$

The minimum gate time (Ua2):

$$T_g = 2 \times T\emptyset$$

accuracy ± LSB.

Inputs and Outputs

All inputs and outputs are TTL compatible.
D0 – D7: Bidirectional bus transceiver with tri-state outputs.

ELECTRICAL CHARACTERISTICS

absolute maximum ratings over operating free-air temperature range (uzless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.3 to 7 V
All input voltages . . . . . −0.3 to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNITS
Supply voltage, V_{CC}	4.75	5	5.25	V
High level output current, I_{OH} (all outputs)			−400	μA
Low level output current, I_{OL} (all outputs)			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operation free-air temperature range (unless otherwise noted)

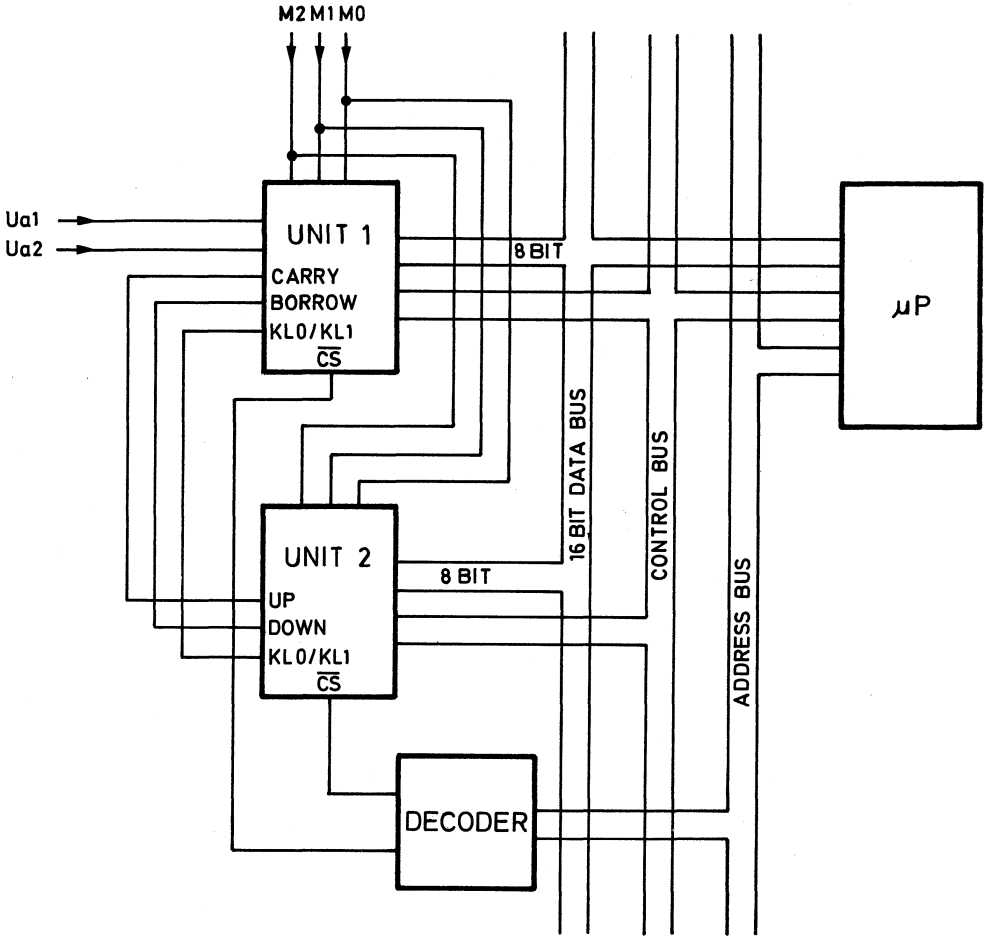
PARAMETER		TEST CONDITIONS		MIN	TYP*	MAX	UNITS
V_{IH}	High level input voltage			2			V
V_{IL}	Low level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5	V
V_{OH}	High level output voltage D0 – D7, $\overline{CARRY}$, $\overline{BORROW}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.1		V
V_{OH}	High level output voltage KLI/KLO, $\overline{READY}$	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.1			V
V_{OL}	Low level output voltage	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 8 mA		0.25	0.4	V
		V_{IL} = V_{IL}max	I_{OL} = 16 mA		0.35	0.5	
I_{OZ}	Off state (high impedance state) output current D0 – D7	V_{CC} = MAX	V_O = 2.7 V			20	μA
		V_{IH} = 2 V	V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1	mA
I_{IH}	High level input current	V_{CC} = MAX, V_{IH} = 2.7 V				20	μA
I_{IL}	Low level input current	V_{CC} = MAX, V_I = 0.4 V				−0.2	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		−40		−120	mA
I_{CC}	Supply current	V_{CC} = MAX			150	190	mA

* All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
F max, for 0, U_{a1}, U_{a2}, UP, DOWN	CL = 15 pF, RL = 2 kΩ	5	20		MHz
T_{WL1} Input frequency width low for 0, U_{a1}, U_{a2}, UP, DOWN		100			ns
T_W Reset Pulse width, $\overline{RESET}$, Input Low			70		ns
T_W $\overline{KLI/KLO}$, Pulse width, $\overline{KLI/KLO}$, Input Low			30		ns
T_D $\overline{RO}$/DATA Delay time, $\overline{RD}$ to Data valid			30		ns
T_H $\overline{WE}$/DATA Hold time, Data after ↑ $\overline{WE}$			TBD		ns
T_D $\overline{READY}$ Delay time, $\overline{READY}$ low after ↓ 0			27		ns
T_{WL2} Pulse width low for gate input U_{a2} (Pulse width mode), U_{a1} (Frequency mode)			TBD		ns

SYSTEM APPLICATION



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